ICX205AK

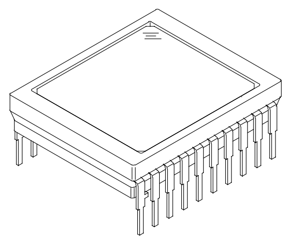
Diagonal 8mm (Type 1/2) Progressive Scan CCD Image Sensor with Square Pixel for Color Cameras

Description

The ICX205AK is a diagonal 8mm (Type 1/2) interline CCD solid-state image sensor with a square pixel array and 1.45M effective pixels. Progressive scan allows all pixels' signals to be output independently within approximately 1/7.5 second. Also, the adoption of high frame rate readout mode supports 30 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High resolution and high color reproductivity are achieved through the use of R, G, B primary color mosaic filters. Further, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

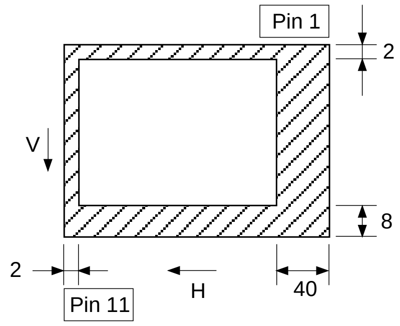
This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

20 pin DIP (Cer-DIP)



Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approx. 800TV-lines) still image without a mechanical shutter.
- Supports high frame rate readout mode (effective 256 lines output, 30 frame/s)
- Square pixel
- Horizontal drive frequency: 14.318MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- R, G, B primary color mosaic filters on chip
- High resolution, high color reproductivity, high sensitivity, low dark current
- Low smear, excellent antiblooming characteristics
- Continuous variable-speed shutter



Optical black position (Top View)

Device Structure

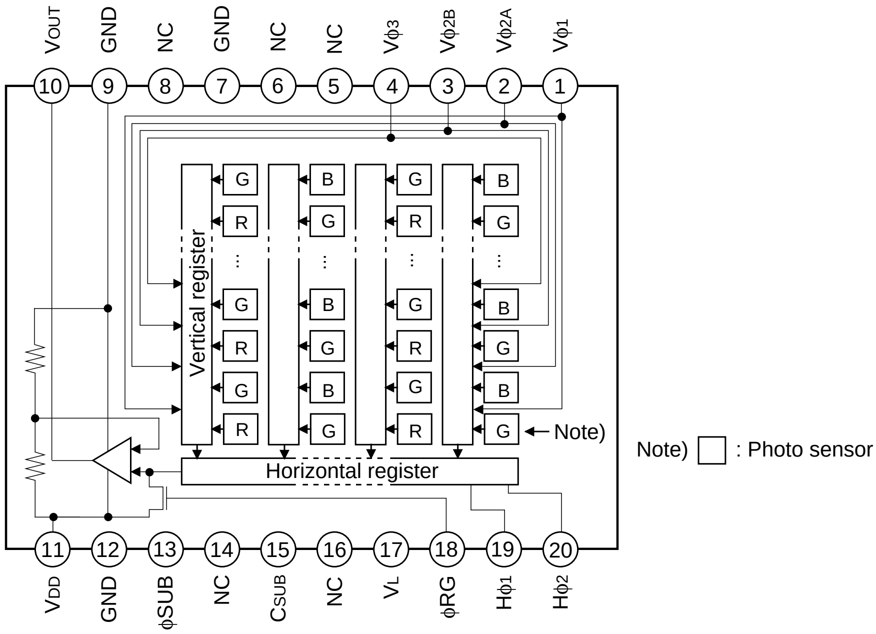
- Interline CCD image sensor
- Image size: Diagonal 8mm (Type 1/2)
- Total number of pixels: 1434 (H) × 1050 (V) approx. 1.50M pixels
- Number of effective pixels: 1392 (H) × 1040 (V) approx. 1.45M pixels
- Number of active pixels: 1360 (H) × 1024 (V) approx. 1.40M pixels (7.959mm diagonal)
- Chip size: 7.60mm (H) × 6.20mm (V)
- Unit cell size: 4.65µm (H) × 4.65µm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
  Vertical 3
- Substrate material: Silicon

WfineCCD®

* Wfine CCD is a registered trademark of Sony Corporation.
Represents a CCD adopting progressive scan, primary color filter and square pixel.

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_1$	Vertical register transfer clock	11	V_{DD}	Supply voltage
2	$V\phi_{2A}$	Vertical register transfer clock	12	GND	GND
3	$V\phi_{2B}$	Vertical register transfer clock	13	φSUB	Substrate clock
4	$V\phi_3$	Vertical register transfer clock	14	NC	
5	NC		15	C_{SUB}	Substrate bias*1
6	NC		16	NC	
7	GND	GND	17	V_L	Protective transistor bias
8	NC		18	φRG	Reset gate clock
9	GND	GND	19	$H\phi_1$	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	$H\phi_2$	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +10	V	
	$V\phi_{2A}$, $V\phi_{2B}$ – φSUB	–50 to +15	V	
	$V\phi_1$, $V\phi_3$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +18	V	
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +15	V	
Against V_L	$V\phi_{2A}$, $V\phi_{2B}$ – V_L	–0.3 to +28	V	
	$V\phi_1$, $V\phi_3$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–16 to +16	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_3$	–16 to +16	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L		*1			
Substrate clock	φSUB		*2			
Reset gate clock	φRG		*2			

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

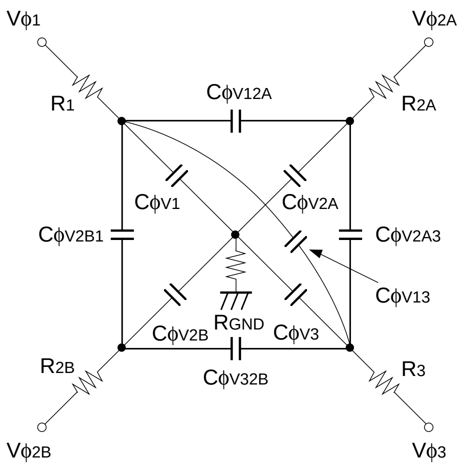
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		5.5		mA	

Clock Voltage Conditions

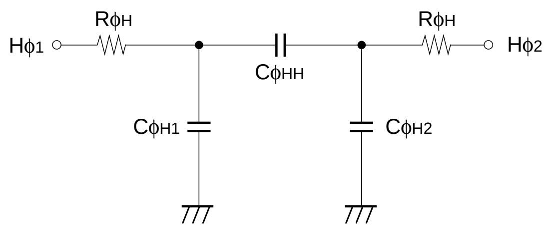
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02A}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02A}$
	V_{VH1}, V_{VH2A}, V_{VH2B}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2A}, V_{VL2B}, V_{VL3}	–8.4	–8.0	–7.6	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$
	$V_{\phi 1}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3}$	7.6	8.0	8.4	V	2	
	$\| V_{VL1} - V_{VL3} \|$			0.1	V	2	
	V_{VHH}			0.9	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.0	V	2	Low-level coupling
	V_{VLL}			0.9	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V_{\phi RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	22.15	23.0	23.85	V	5	

Clock Equivalent Circuit Constant

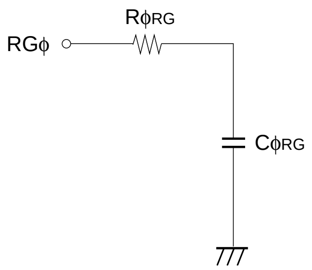
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$		2200		pF	
	$C\phi_{V2A}$		1800		pF	
	$C\phi_{V2B}$		6800		pF	
	$C\phi_{V3}$		3300		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12A}$, $C\phi_{V2B1}$		1200		pF	
	$C\phi_{V2A3}$, $C\phi_{V32B}$		1200		pF	
	$C\phi_{V13}$		2200		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		100		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		680		pF	
Vertical transfer clock series resistor	R_1		36		Ω	
	R_{2A}, R_3		56		Ω	
	R_{2B}		43		Ω	
Vertical transfer clock ground resistor	R_{GND}		30		Ω	
Horizontal transfer clock series resistor	$R\phi_H$		15		Ω	
Reset gate clock series resistor	$R\phi_{RG}$		20		Ω	



Vertical transfer clock equivalent circuit



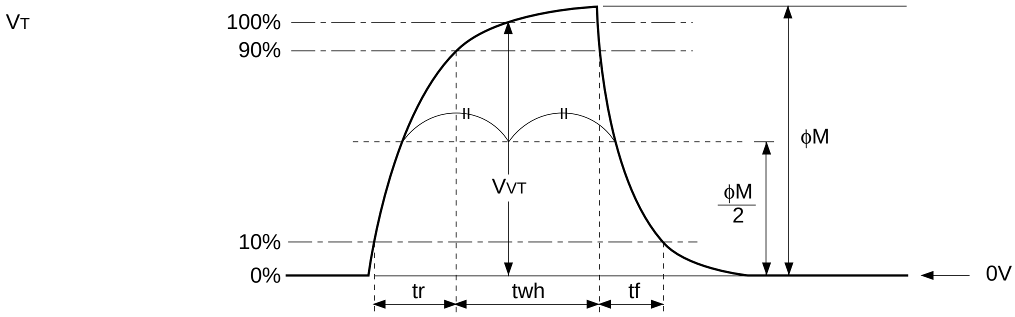
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

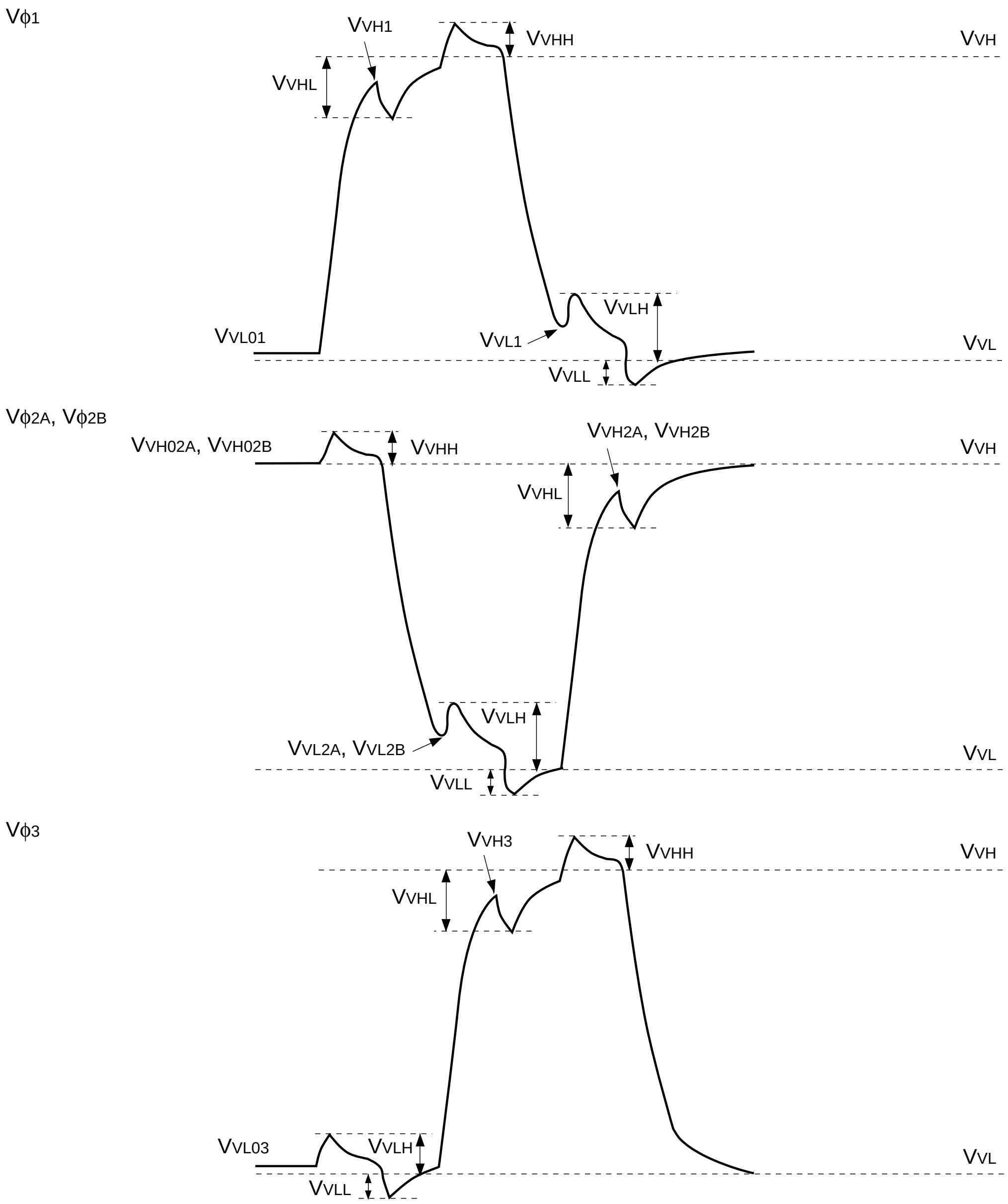
Drive Clock Waveform Conditions

(1) Readout clock waveform



Note) Readout clock is used by composing vertical transfer clocks $V\phi_{2A}$ and $V\phi_{2B}$.

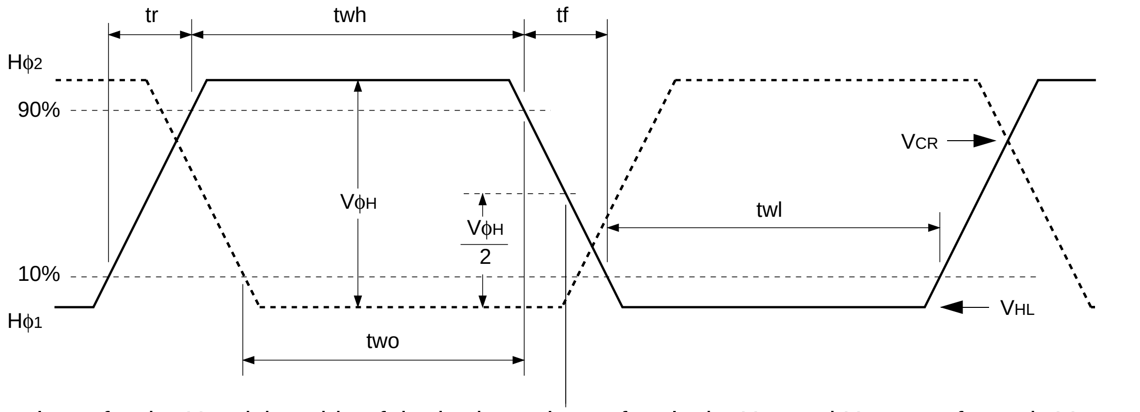
(2) Vertical transfer clock waveform



$V_{VH} = V_{VH02A}$
$V_{VL} = (V_{VL01} + V_{VL03}) / 2$
$V_{VL3} = V_{VL03}$

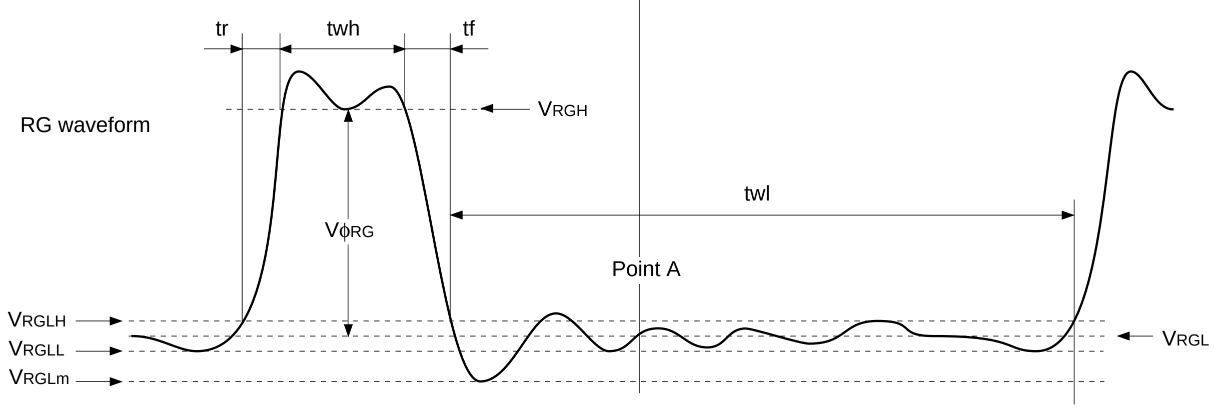
$V_{\phi V1} = V_{VH1} - V_{VL01}$
$V_{\phi V2A} = V_{VH02A} - V_{VL2A}$
$V_{\phi V2B} = V_{VH02B} - V_{VL2B}$
$V_{\phi V3} = V_{VH3} - V_{VL03}$

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hφ1 rising side of the horizontal transfer clocks Hφ1 and Hφ2 waveforms is V_{CR}.
The overlap period for twh and twl of horizontal transfer clocks Hφ1 and Hφ2 is two.

(4) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

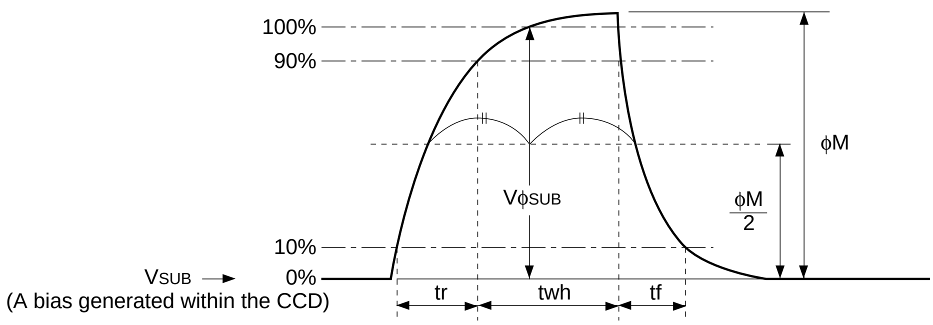
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming V_{RGH} is the minimum value during the interval twh, then:

$V_{\phi RG} = V_{RGH} - V_{RGL}$.

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$										15		450	ns	*1
Horizontal transfer clock — During imaging	$H\phi_1$	20	25		20	25			10	15		10	15	ns	*2
	$H\phi_2$	20	25		20	25			10	15		10	15		
Horizontal transfer clock — During parallel-serial conversion	$H\phi_1$								0.01			0.01		µs	
	$H\phi_2$								0.01			0.01			
Reset gate clock	ϕRG	11	13			51			3			3		ns	
Substrate clock	ϕSUB		2.2							0.5			0.5	µs	During drain charge

*1 When vertical transfer clock driver CXD1267AN × 2 is used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (V_{CR}) for the $H\phi_1$ rising side of the $H\phi_1$ and $H\phi_2$ waveforms must be at least $V\phi_H/2$ [V].

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	16	20		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

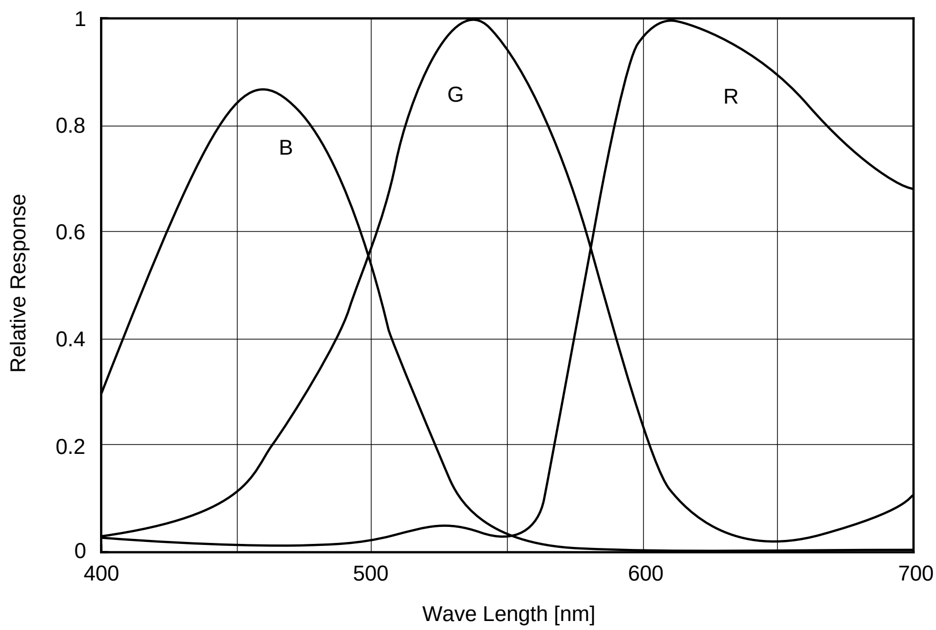
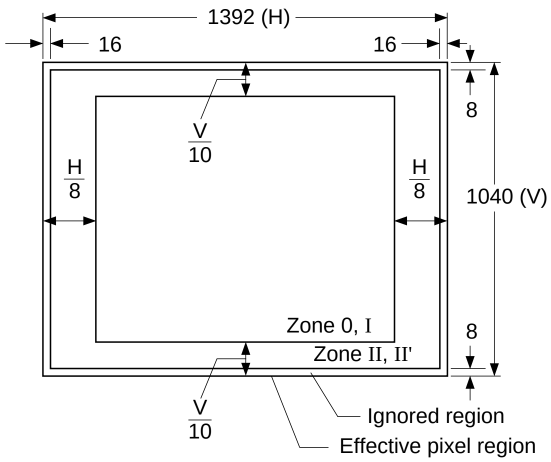


Image Sensor Characteristics

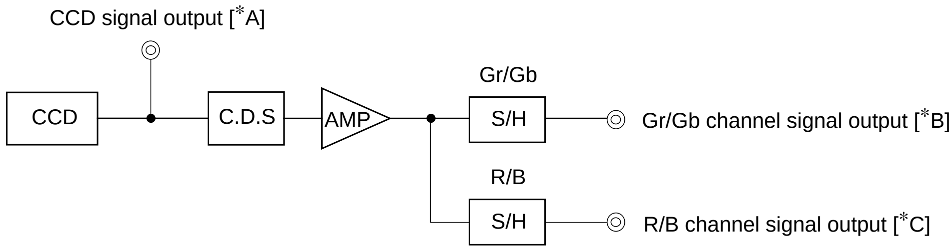
(Ta = 25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	320	400		mV	1	1/30s accumulation
Sensitivity comparison	R	Rr	0.4	0.55	0.7		1	
	B	Rb	0.3	0.45	0.6		1	
Saturation signal		Vsat	450			mV	2	Ta = 60°C
Smear		Sm		0.001	0.0025	%	3	No electronic shutter
Video signal shading		SHg			20	%	4	Zone 0 and I
					25	%	4	Zone 0 to II'
Uniformity between video signal channels		ΔSrg			8	%	5	
		ΔSbg			8	%	5	
Dark signal		Vdt			16	mV	6	Ta = 60°C
Dark signal shading		ΔVdt			4	mV	7	Ta = 60°C
Line crawl G		Lcg			3.8	%	8	
Line crawl R		Lcr			3.8	%	8	
Line crawl B		Lcb			3.8	%	8	
Lag		Lag			0.5	%	9	

Zone Definition of Video Signal Shading



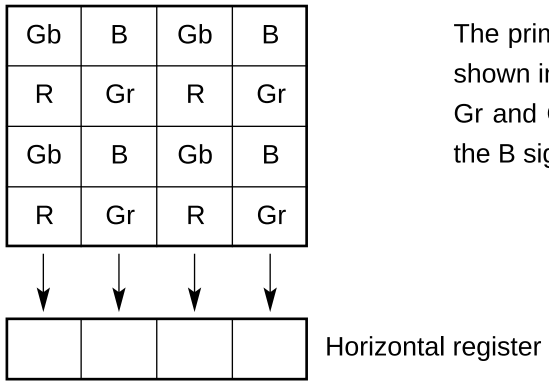
Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

◎ Color coding and readout of this image sensor



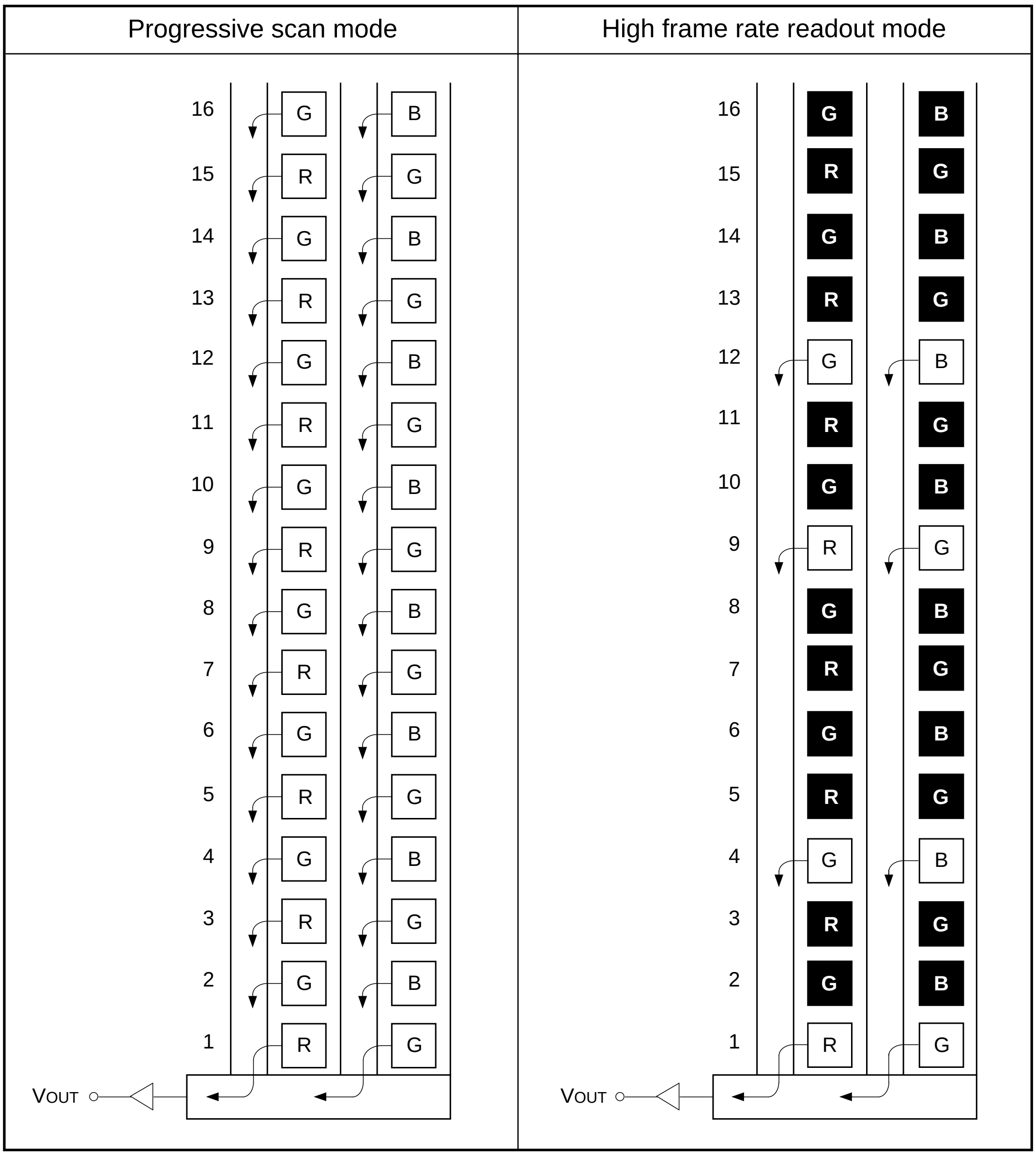
Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

All pixel signals are output successively in a 1/7.5s period.
The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

◎ Readout modes

The diagram below shows the output methods for the following two readout modes.



Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from the line 1 in high frame rate readout mode.

1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/7.5s.
   The vertical resolution is approximately 800TV-lines and all pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   All effective areas are scanned in approximately 1/30s by reading out two out of eight lines (1st and 4th lines, 9th and 12th lines). The vertical resolution is approximately 200TV-lines.
   This readout mode emphasizes processing speed over vertical resolution.

◎ Measurement conditions

1) In the following measurements, the device drive conditions are at the typical values of the progressive scan mode, bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

◎ Definition of standard imaging conditions

1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity comparison
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$V_G = (V_{Gr} + V_{Gb})/2$
$Sg = V_G \times 100/30$ [mV]
$Rr = V_R/V_G$
$Rb = V_B/V_G$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (V_{Sm} [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \times 100\ [\%]$$ (1/10V method conversion value)

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum (Grmax [mV]) and minimum (Grmin [mV]) values of the Gr signal output and substitute the values into the following formula.

$SHg = (Grmax – Grmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
   After measuring 4, measure the maximum (Rmax [mV]) and minimum (Rmin [mV]) values of the R signal and the maximum (Bmax [mV]) and minimum (Bmin [mV]) values of the B signal, and substitute the values into the following formulas.

   $\Delta Srg = (Rmax - Rmin)/150 \times 100$ [%]
   $\Delta Sbg = (Bmax - Bmin)/150 \times 100$ [%]

6. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

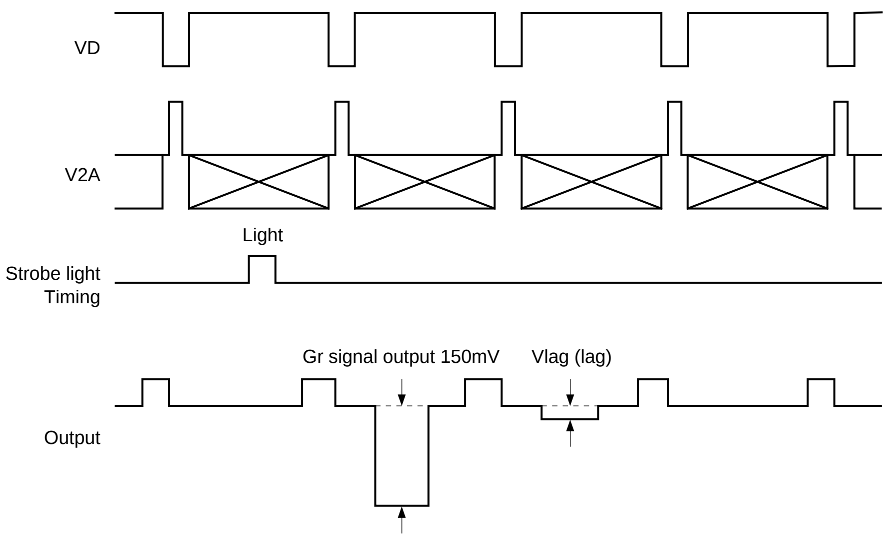
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawl
   Set to standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

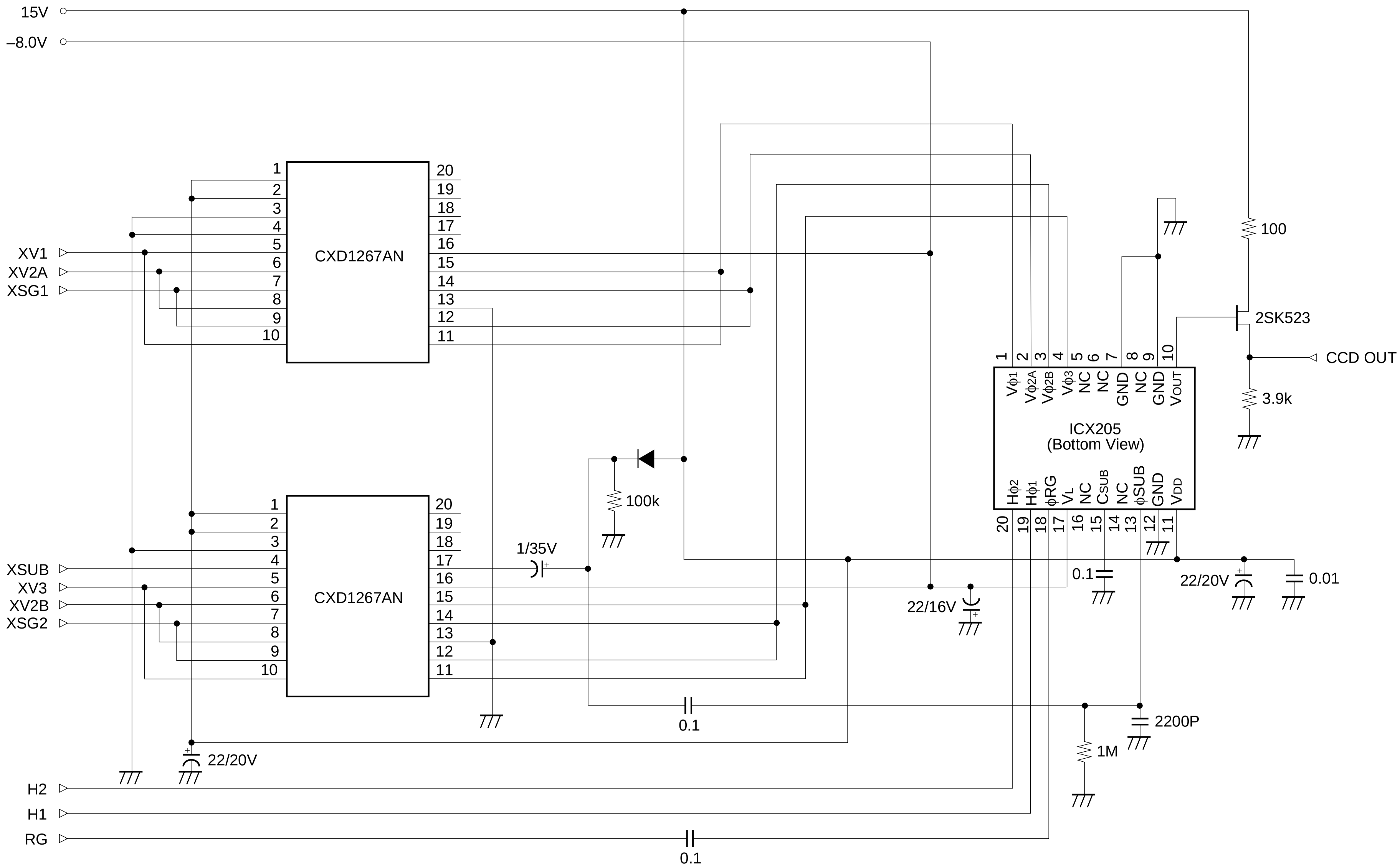
   $Lci = \Delta Gli/Gai \times 100$ [%] (i = r, g, b)

9. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

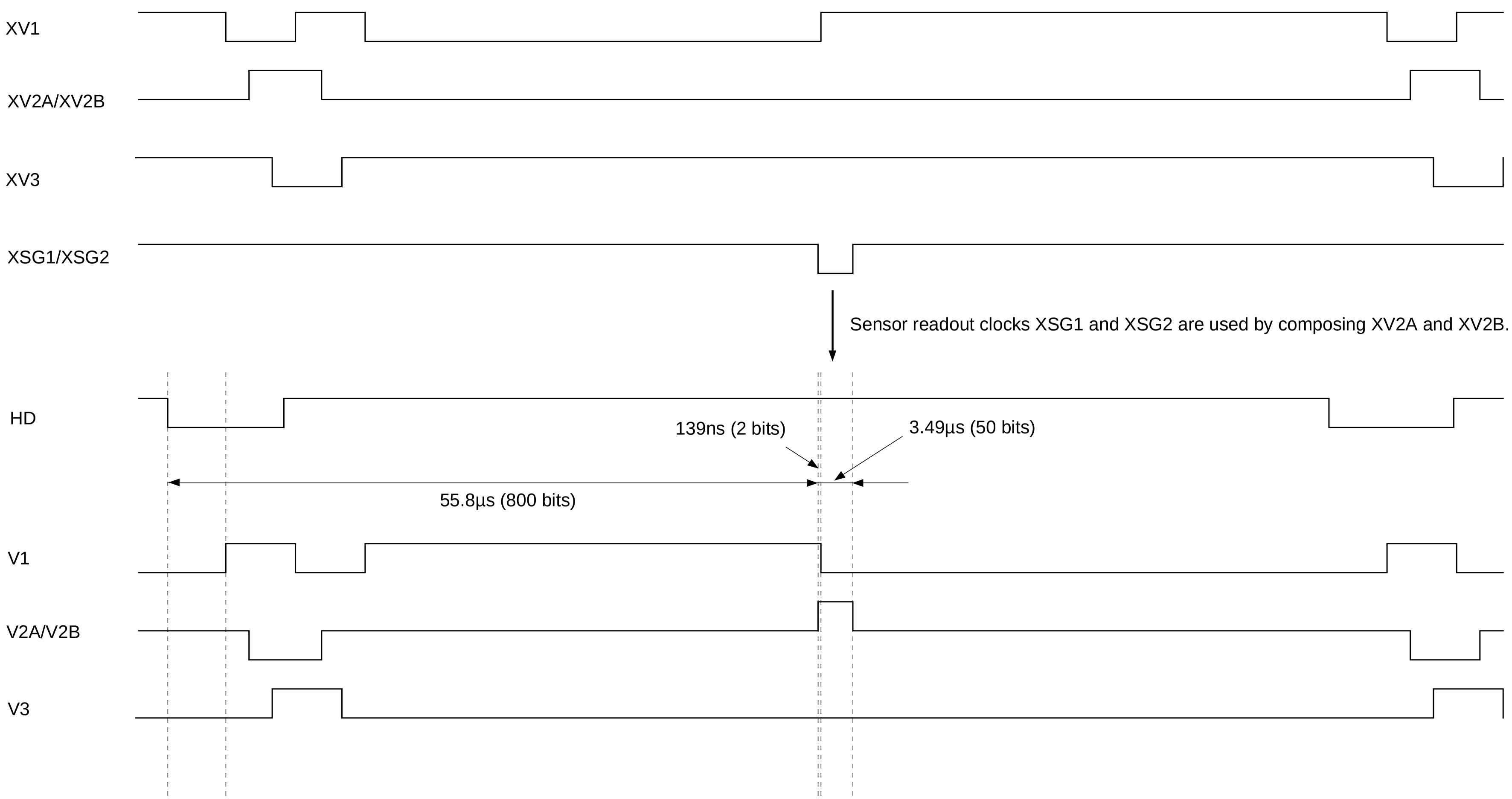
   $Lag = (Vlag/150) \times 100$ [%]



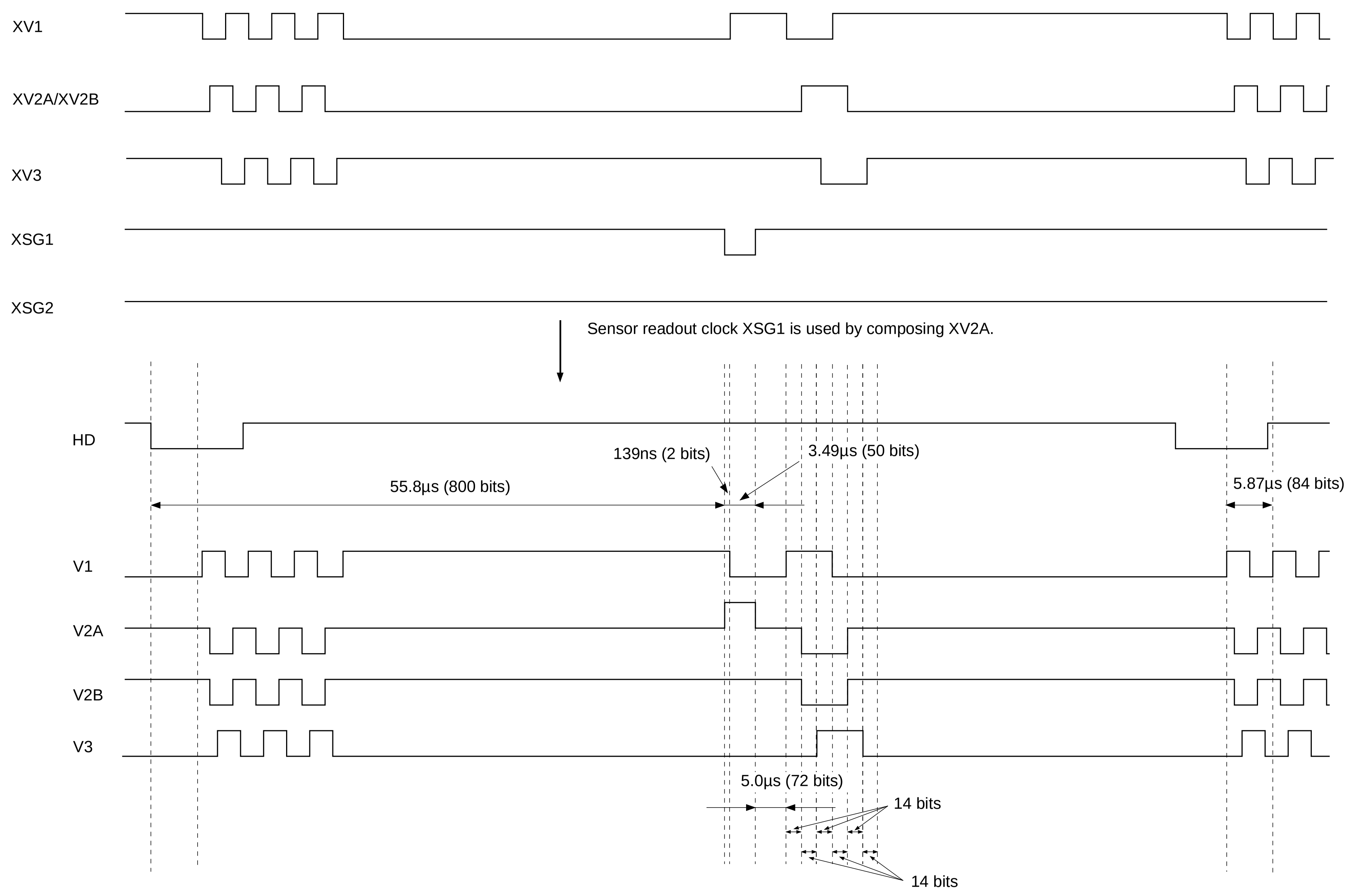
Drive Circuit



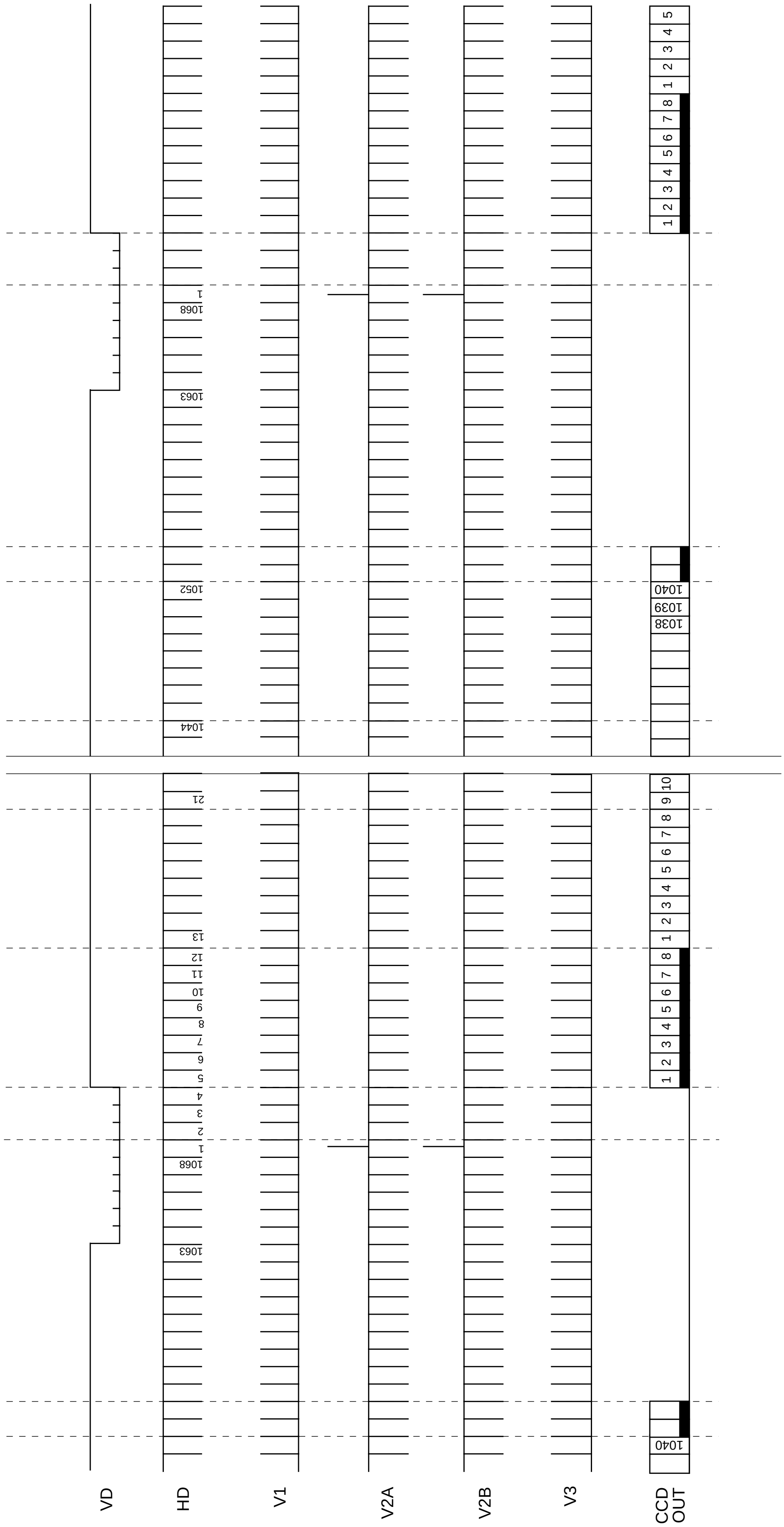
Sensor Readout Clock Timing Chart   Progressive Scan Mode



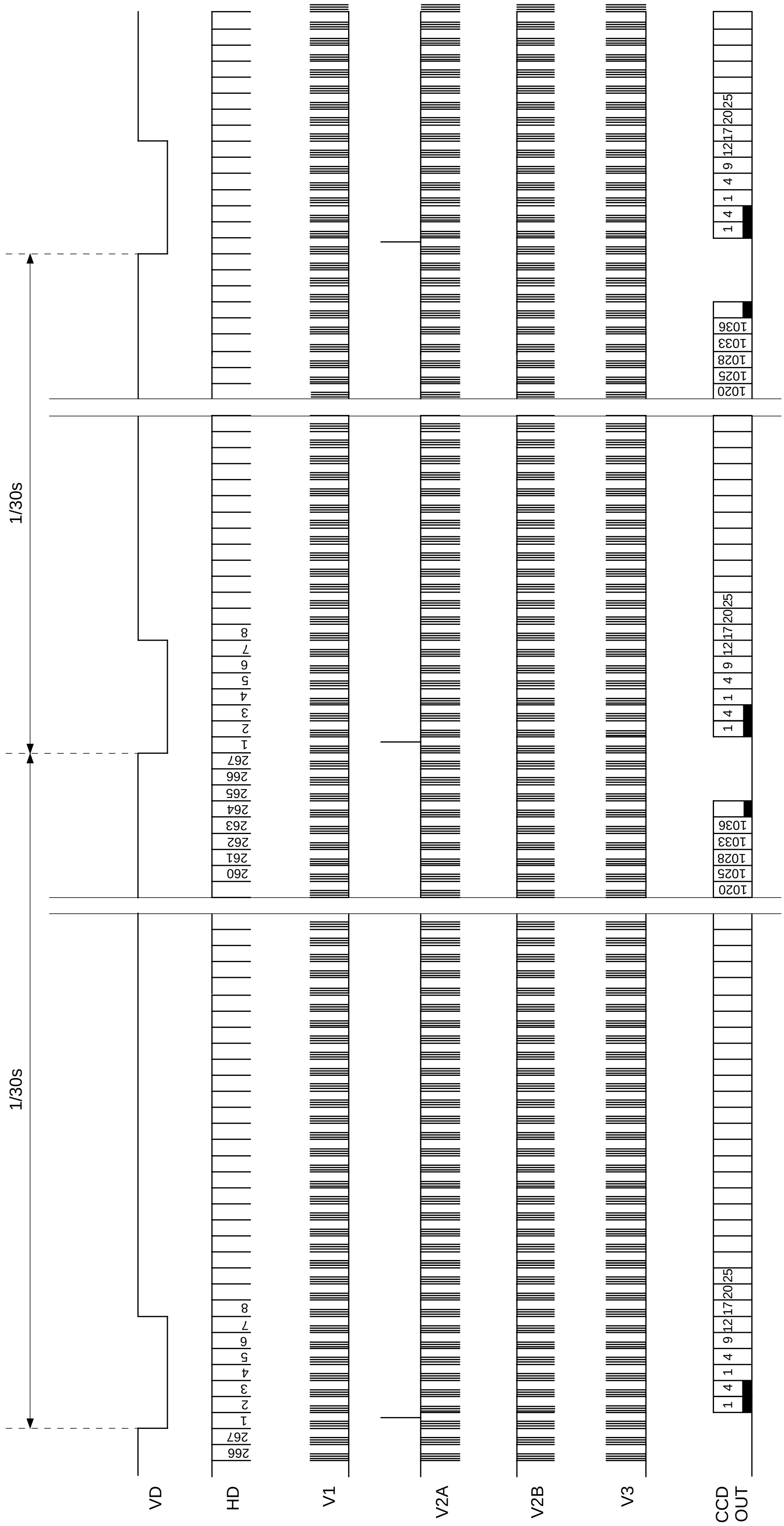
Sensor Readout Clock Timing Chart High Frame Rate Readout Mode



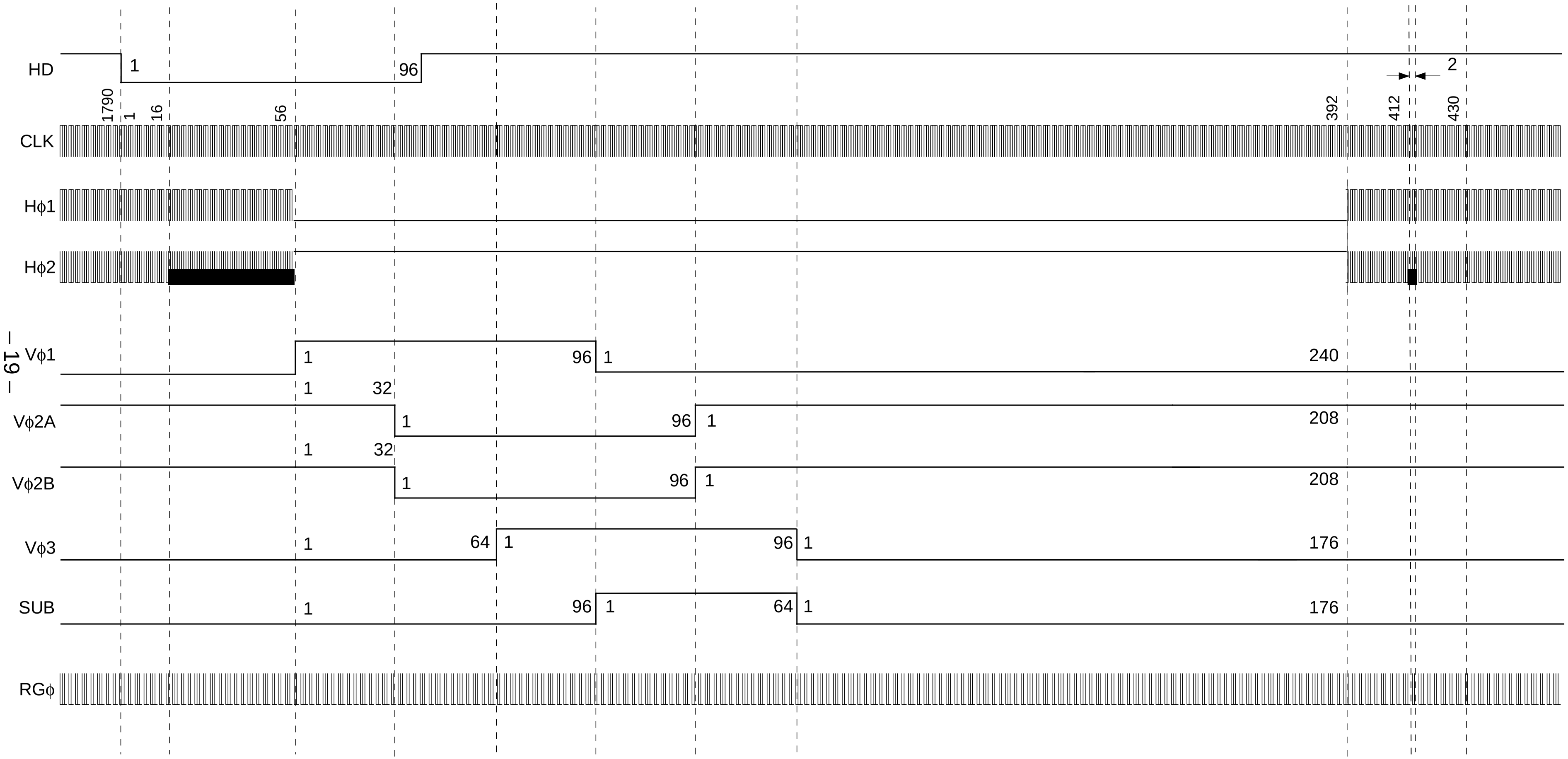
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



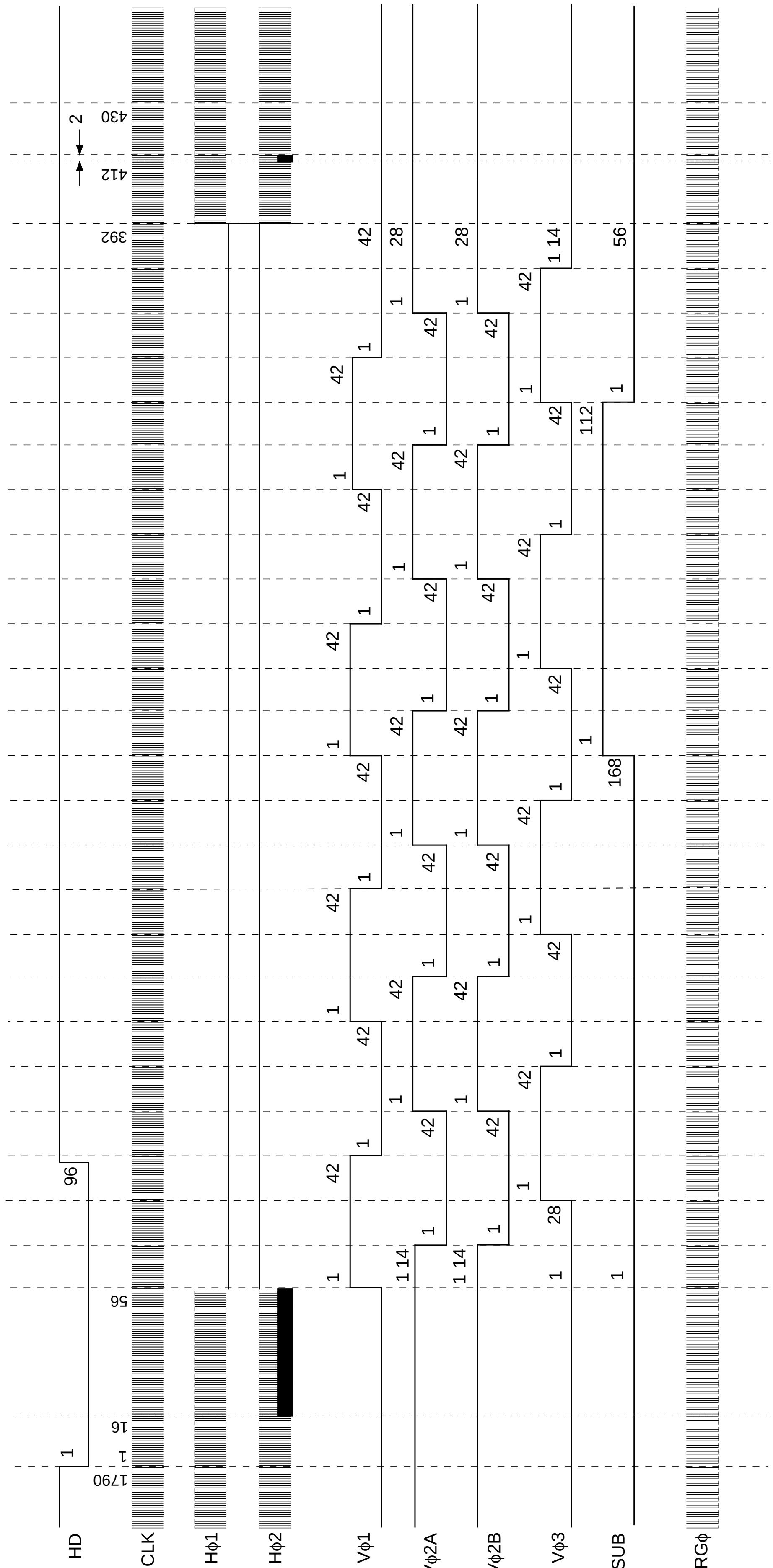
Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode



Drive Timing Chart (Horizontal Sync)   Progressive Scan Mode



Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

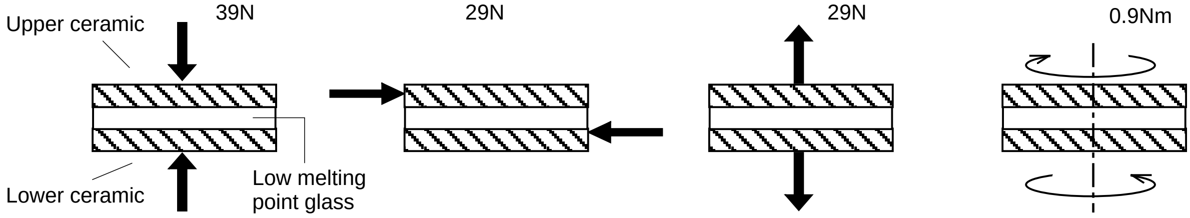
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Shearing strength** **Tensile strength** **Torsional strength**

b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portions. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.

d) The upper and lower ceramic are joined by low melting point glass. Therefore, care should be taken not to perform the following actions as this may cause cracks.
   - Applying repeated bending stress to the outer leads.
   - Heating the outer leads for an extended period with a soldering iron.
   - Rapidly cooling or heating the package.
   - Applying any load or impact to a limited portion of the low melting point glass using tweezers or other sharp tools.
   - Prying at the upper or lower ceramic using the low melting point glass as a fulcrum.

   Note that the same cautions also apply when removing soldered products from boards.

e) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

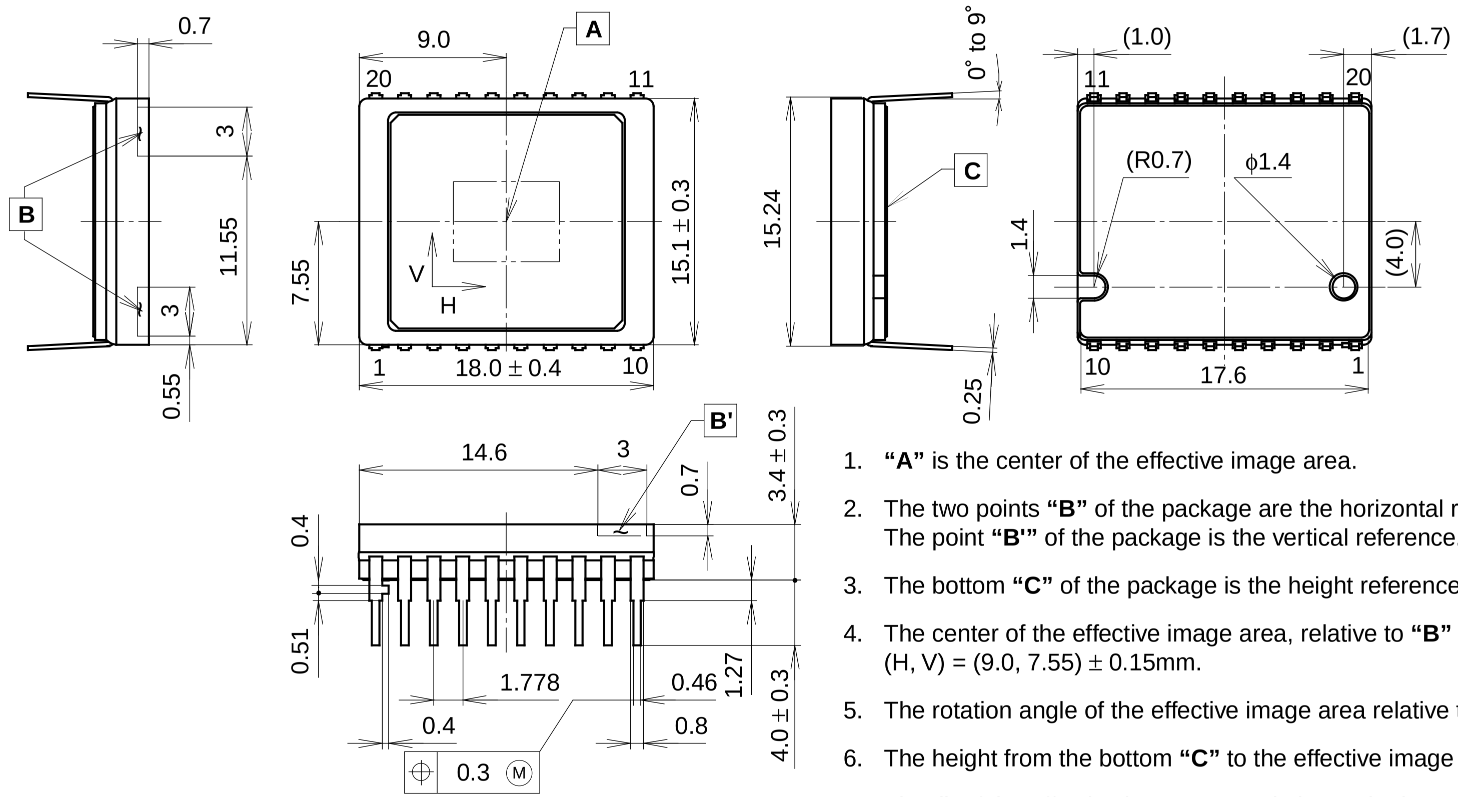
5) Others

a) Do not expose to strong light (sun rays) for long periods, color filters will be discolored. When high luminance objects are imaged with the exposure level control by electronic-iris, the luminance of the image-plane may become excessive and discolor of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

Package Outline Unit: mm

20 pin DIP (600mil)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package is the height reference.
4. The center of the effective image area, relative to **"B"** and **"B'"** is
   (H, V) = (9.0, 7.55) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 60µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch and the hole on the bottom must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.60g
DRAWING NUMBER	AS-B2-02(E)