SONY

Diagonal 11.0 mm (Type 2 / 3) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

IMX421LLJ-C

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Description

The IMX421LLJ-C is a diagonal 11.0 mm (Type 2 / 3, 0.67-inch) CMOS active pixel type solid-state image sensor with a square pixel array and 2.86 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: FA cameras, ITS cameras)

Features

- CMOS active pixel type dots
- Built-in timing adjustment circuit, H/V driver and serial communication circuit
- Global shutter function
- Input frequency
  37.125 MHz / 74.25 MHz / 54 MHz
- Number of recommended recording pixels: 1936 (H) × 1464 (V) approx. 2.83 M pixels

  Readout mode
  All - pixel scan mode
  1080p - Full HD readout mode
  Vertical / Horizontal 1 / 2 Subsampling mode
  2 × 2 Vertical FD binning mode
  ROI mode
  Vertical / Horizontal ‐ Normal / Inverted readout mode
- Readout rate
  Maximum frame rate in

  All - pixel scan mode: 8 bit 409.2 frame/s, 10 bit: 371.8 frame/s, 12 bit: 231.2 frame/s
- Variable-speed shutter function (resolution 1 H units)
- 8-bit / 10-bit / 12-bit A/D converter
- Conversion gain switching (HCG Mode / LCG Mode)
- CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- I/O interface
  SLVS (4 ch / 8 ch switching) output

  SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 lane) output
- Recommended lens F number: 2.8 or more (Close side)
- Recommended exit pupil distance: –100 mm to –∞

Device Structure

- ◆ CMOS image sensor
- ◆ Image size

Diagonal 11.0 mm (Type 2 / 3)	Approx. 2.86 M pixels All - pixel
Diagonal 10.1 mm (Type 1 / 1.58)	Approx. 2.13M pixels 1080p - Full HD

- ◆ Total number of pixels

1944 (H) × 1496 (V)	Approx. 2.90 M pixels

- ◆ Number of effective pixels

1944 (H) × 1472 (V)	Approx. 2.86 M pixels

- ◆ Number of active pixels

1944 (H) × 1472 (V)	Approx. 2.86 M pixels

- ◆ Number of recommended recording pixels

1936 (H) × 1464 (V)	Approx. 2.83 M pixels All - pixel
1920 (H) × 1080 (V)	Approx. 2.07M pixels 1080p - Full HD

- ◆ Unit cell size
  4.5 µm (H) × 4.5 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 24 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Rating			Unit	Remarks
Supply voltage (Analog 3.3 V)	AV_{DD}	–0.3	to	+4.0	V	
Supply voltage (Interface 1.8 V)	OV_{DD}	–0.3	to	+3.3	V	
Supply voltage (Digital 1.2 V)	DV_{DD}	–0.3	to	+2.0	V	
Input voltage	VI	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Output voltage	VO	–0.3	to	OV_{DD} +0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	to	+75	˚C	
Storage temperature	Tstg	-40	to	+85	˚C	
Performance guarantee temperature	Tspec	-10	to	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Analog 3.3 V)	AV_{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (Digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

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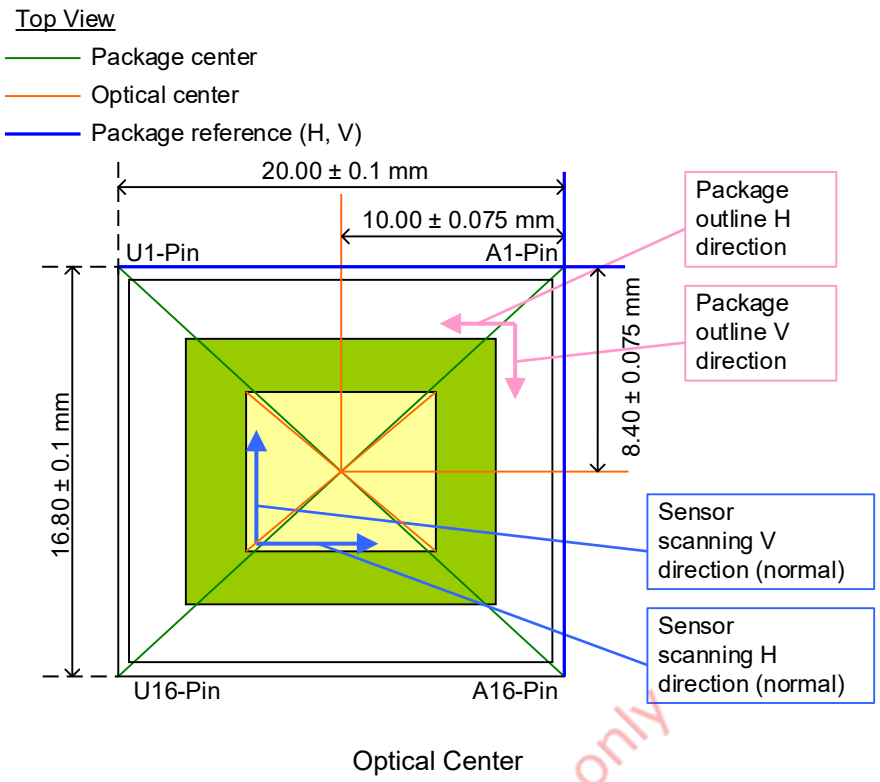
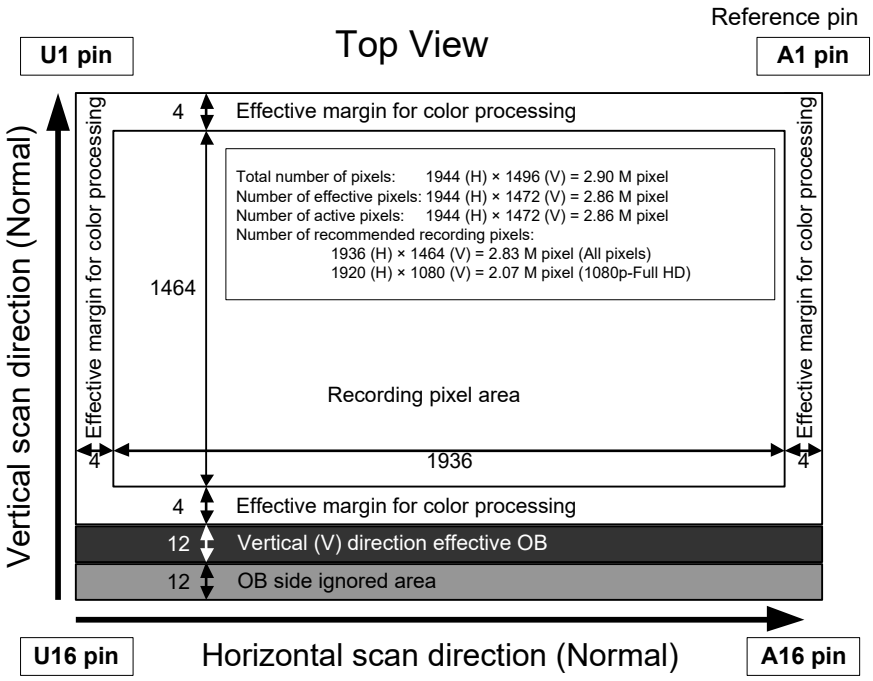
Chip Center and Optical Center



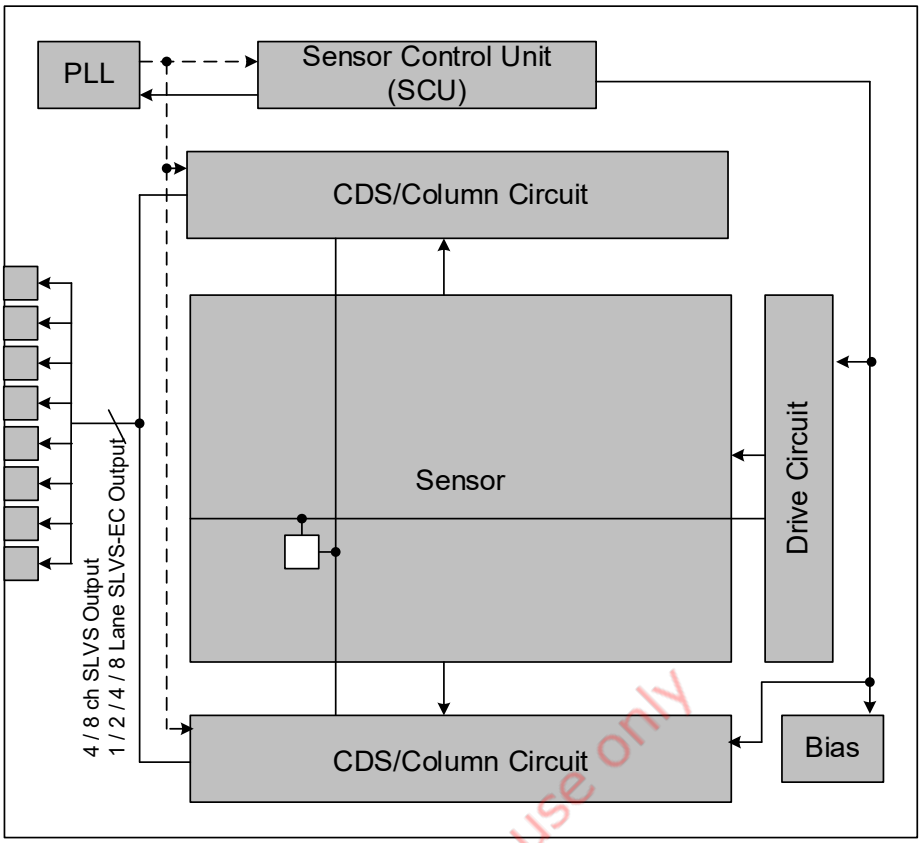
Pixel Arrangement



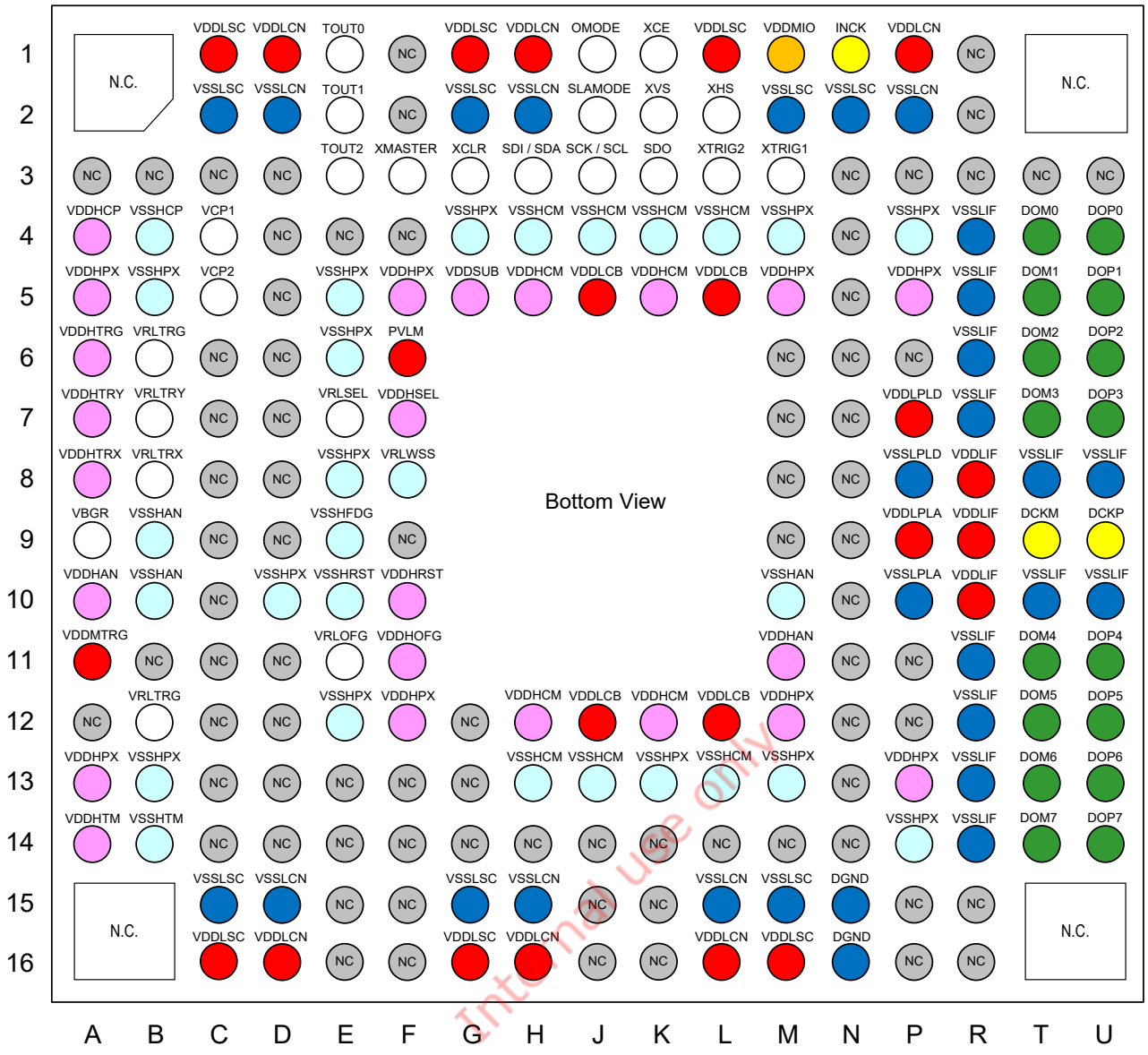
Pixel Arrangement

Block Diagram and Pin Configuration

(Top View)



Block Diagram



Pin Configuration

Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
1	A1	—	—	N.C.	—
2	A3	—	—	N.C.	—
3	A4	Power	A	VDDHCP	3.3 V power supply
4	A5	Power	A	VDDHPX	3.3 V power supply
5	A6	Power	A	VDDHTRG	3.3 V power supply
6	A7	Power	A	VDDHTRY	3.3 V power supply
7	A8	Power	A	VDDHTRX	3.3 V power supply
8	A9	O	A	VBGR	Connect to 0.22 µF to GND
9	A10	Power	A	VDDHAN	3.3 V power supply
10	A11	Power	A	VDDMTRG	1.2 V power supply
11	A12	—	—	N.C.	—
12	A13	Power	A	VDDHPX	3.3 V power supply
13	A14	Power	A	VDDHTM	3.3 V power supply
14	A16	—	—	N.C.	—
15	B3	—	—	N.C.	—
16	B4	GND	A	VSSHCP	3.3 V GND
17	B5	GND	A	VSSHPX	3.3 V GND
18	B6	I	A	VRLTRG	Connect to VCP2
19	B7	I	A	VRLTRY	Connect to VCP1
20	B8	I	A	VRLTRX	Connect to VCP1
21	B9	GND	A	VSSHAN	3.3 V GND
22	B10	GND	A	VSSHAN	3.3 V GND
23	B11	—	—	N.C.	—
24	B12	I	A	VRLTRG	Connect to VCP2
25	B13	GND	A	VSSHPX	3.3 V GND
26	B14	GND	A	VSSHTM	3.3 V GND
27	C1	Power	D	VDDLSC	1.2 V power supply
28	C2	GND	D	VSSLSC	1.2 V GND
29	C3	—	—	N.C.	—
30	C4	O	A	VCP1	Connect to VRLOFG, VRLTRX, VRLSEL, VRLTRY (Connect to 4.7 µF × 4 to GND)
31	C5	O	A	VCP2	Connect to VRLTRG (Connect to 4.7 µF × 4 to GND)
32	C6	—	—	N.C.	—
33	C7	—	—	N.C.	—
34	C8	—	—	N.C.	—
35	C9	—	—	N.C.	—
36	C10	—	—	N.C.	—
37	C11	—	—	N.C.	—
38	C12	—	—	N.C.	—
39	C13	—	—	N.C.	—
40	C14	—	—	N.C.	—
41	C15	GND	D	VSSLSC	1.2 V GND
42	C16	Power	D	VDDLSC	1.2 V power supply
43	D1	Power	D	VDDLCN	1.2 V power supply
44	D2	GND	D	VSSLCN	1.2 V GND
45	D3	—	—	N.C.	—
46	D4	—	—	N.C.	—
47	D5	—	—	N.C.	—
48	D6	—	—	N.C.	—
49	D7	—	—	N.C.	—
50	D8	—	—	N.C.	—
51	D9	—	—	N.C.	—
52	D10	GND	A	VSSHPX	3.3 V GND
53	D11	—	—	N.C.	—
54	D12	—	—	N.C.	—
55	D13	—	—	N.C.	—
56	D14	—	—	N.C.	—
57	D15	GND	D	VSSLCN	1.2 V GND
58	D16	Power	D	VDDLCN	1.2 V power supply
59	E1	O	D	TOUT0	Pulse0 output pin
60	E2	O	D	TOUT1	Pulse1 output pin
61	E3	O	D	TOUT2	Pulse2 output pin
62	E4	—	—	N.C.	—

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
63	E5	GND	A	VSSHPX	3.3 V GND
64	E6	GND	A	VSSHPX	3.3 V GND
65	E7	I	A	VRLSEL	Connect to VCP1
66	E8	GND	A	VSSHPX	3.3 V GND
67	E9	GND	A	VSSHFDG	3.3 V GND
68	E10	GND	A	VSSHRST	3.3 V GND
69	E11	I	A	VRLOFG	Connect to VCP1
70	E12	GND	A	VSSHPX	3.3 V GND
71	E13	—	—	N.C.	—
72	E14	—	—	N.C.	—
73	E15	—	—	N.C.	—
74	E16	—	—	N.C.	—
75	F1	—	—	N.C.	—
76	F2	—	—	N.C.	—
77	F3	I	D	XMASTER	Master / Slave select (Slave Mode: High, Master Mode: Low)
78	F4	—	—	N.C.	—
79	F5	Power	A	VDDHPX	3.3 V power supply
80	F6	Power	A	PVLM	1.2 V power supply
81	F7	Power	A	VDDHSEL	3.3 V power supply
82	F8	GND	A	VRLWSS	3.3 V GND
83	F9	—	—	N.C.	—
84	F10	Power	A	VDDHRST	3.3 V power supply
85	F11	Power	A	VDDHOFG	3.3 V power supply
86	F12	Power	A	VDDHPX	3.3 V power supply
87	F13	—	—	N.C.	—
88	F14	—	—	N.C.	—
89	F15	—	—	N.C.	—
90	F16	—	—	N.C.	—
91	G1	Power	D	VDDLSC	1.2 V power supply
92	G2	GND	D	VSSLSC	1.2 V GND
93	G3	I	D	XCLR	System clear (Normal: High, Clear: Low)
94	G4	GND	A	VSSHPX	3.3 V GND
95	G5	Power	A	VDDSUB	3.3 V power supply
96	G12	—	—	N.C.	—
97	G13	—	—	N.C.	—
98	G14	—	—	N.C.	—
99	G15	GND	D	VSSLSC	1.2 V GND
100	G16	Power	D	VDDLSC	1.2 V power supply
101	H1	Power	D	VDDLCN	1.2 V power supply
102	H2	GND	D	VSSLCN	1.2 V GND
103	H3	I/O	D	SDI / SDA	4-wire: Serial communication I/F SDI pin I^2C: Serial data line
104	H4	GND	A	VSSHCM	3.3 V GND
105	H5	Power	A	VDDHCM	3.3 V power supply
106	H12	Power	A	VDDHCM	3.3 V power supply
107	H13	GND	A	VSSHCM	3.3 V GND
108	H14	—	—	N.C.	—
109	H15	GND	D	VSSLCN	1.2 V GND
110	H16	Power	D	VDDLCN	1.2 V power supply
111	J1	I	D	OMODE	SLVS - EC / SLVS mode select (SLVS - EC: High, SLVS: Low)
112	J2	I	D	SLAMODE	Slave address select (37h: High, 36h: Low, 1Ah: both polarities)
113	J3	I	D	SCK / SCL	4 - wire: Serial communication I/F SCK pin I^2C: Serial clock line
114	J4	GND	A	VSSHCM	3.3 V GND
115	J5	Power	A	VDDLCB	1.2 V power supply
116	J12	Power	A	VDDLCB	1.2 V power supply
117	J13	GND	A	VSSHCM	3.3 V GND
118	J14	—	—	N.C.	—
119	J15	—	—	N.C.	—
120	J16	—	—	N.C.	—
121	K1	I	D	XCE	4 - wire: Serial communication I/F XCE pin I^2C: Fixed to High
122	K2	I/O	D	XVS	Vertical sync signal

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
123	K3	O	D	SDO	4-wire: Serial communication I/F SDO pin I²C: OPEN
124	K4	GND	A	VSSHCM	3.3 V GND
125	K5	Power	A	VDDHCM	3.3 V power supply
126	K12	Power	A	VDDHCM	3.3 V power supply
127	K13	GND	A	VSSHPX	3.3 V GND
128	K14	—	—	N.C.	—
129	K15	—	—	N.C.	—
130	K16	—	—	N.C.	—
131	L1	Power	D	VDDLSC	1.2 V power supply
132	L2	I/O	D	XHS	Horizontal sync signal
133	L3	I	D	XTRIG2	Trigger input 2
134	L4	GND	A	VSSHCM	3.3 V GND
135	L5	Power	A	VDDLCB	1.2 V power supply
136	L12	Power	A	VDDLCB	1.2 V power supply
137	L13	GND	A	VSSHCM	3.3 V GND
138	L14	—	—	N.C.	—
139	L15	GND	D	VSSLCN	1.2 V GND
140	L16	Power	D	VDDLCN	1.2 V power supply
141	M1	Power	D	VDDMIO	1.8 V power supply
142	M2	GND	D	VSSLSC	1.2 V GND
143	M3	I	D	XTRIG1	Trigger input 1
144	M4	GND	A	VSSHPX	3.3 V GND
145	M5	Power	A	VDDHPX	3.3 V power supply
146	M6	—	—	N.C.	—
147	M7	—	—	N.C.	—
148	M8	—	—	N.C.	—
149	M9	—	—	N.C.	—
150	M10	GND	A	VSSHAN	3.3 V GND
151	M11	Power	A	VDDHAN	3.3 V power supply
152	M12	Power	A	VDDHPX	3.3 V power supply
153	M13	GND	A	VSSHPX	3.3 V GND
154	M14	—	—	N.C.	—
155	M15	GND	D	VSSLSC	1.2 V GND
156	M16	Power	D	VDDLSC	1.2 V power supply
157	N1	I	D	INCK	Master clock input
158	N2	GND	D	VSSLSC	1.2 V GND
159	N3	—	—	N.C.	—
160	N4	—	—	N.C.	—
161	N5	—	—	N.C.	—
162	N6	—	—	N.C.	—
163	N7	—	—	N.C.	—
164	N8	—	—	N.C.	—
165	N9	—	—	N.C.	—
166	N10	—	—	N.C.	—
167	N11	—	—	N.C.	—
168	N12	—	—	N.C.	—
169	N13	—	—	N.C.	—
170	N14	—	—	N.C.	—
171	N15	GND	D	DGND	1.2 V GND
172	N16	GND	D	DGND	1.2 V GND
173	P1	Power	D	VDDLCN	1.2 V power supply
174	P2	GND	D	VSSLCN	1.2 V GND
175	P3	—	—	N.C.	—
176	P4	GND	A	VSSHPX	3.3 V GND
177	P5	Power	A	VDDHPX	3.3 V power supply
178	P6	—	—	N.C.	—
179	P7	Power	D	VDDLPLD	1.2 V power supply
180	P8	GND	D	VSSLPLD	1.2 V GND
181	P9	Power	D	VDDLPLA	1.2 V power supply
182	P10	GND	D	VSSLPLA	1.2 V GND
183	P11	—	—	N.C.	—
184	P12	—	—	N.C.	—
185	P13	Power	A	VDDHPX	3.3 V power supply
186	P14	GND	A	VSSHPX	3.3 V GND
187	P15	—	—	N.C.	—
188	P16	—	—	N.C.	—

No.	Pin No.	I/O	Analog / Digital	Symbol	Description
189	R1	—	—	N.C.	—
190	R2	—	—	N.C.	—
191	R3	—	—	N.C.	—
192	R4	GND	D	VSSLIF	1.2 V GND
193	R5	GND	D	VSSLIF	1.2 V GND
194	R6	GND	D	VSSLIF	1.2 V GND
195	R7	GND	D	VSSLIF	1.2 V GND
196	R8	Power	D	VDDLIF	1.2 V power supply
197	R9	Power	D	VDDLIF	1.2 V power supply
198	R10	Power	D	VDDLIF	1.2 V power supply
199	R11	GND	D	VSSLIF	1.2 V GND
200	R12	GND	D	VSSLIF	1.2 V GND
201	R13	GND	D	VSSLIF	1.2 V GND
202	R14	GND	D	VSSLIF	1.2 V GND
203	R15	—	—	N.C.	—
204	R16	—	—	N.C.	—
205	T3	—	—	N.C.	—
206	T4	O	D	DOM0	SLVS / SLVS - EC IF output (Data)
207	T5	O	D	DOM1	SLVS / SLVS - EC IF output (Data)
208	T6	O	D	DOM2	SLVS / SLVS - EC IF output (Data)
209	T7	O	D	DOM3	SLVS / SLVS - EC IF output (Data)
210	T8	GND	D	VSSLIF	1.2 V GND
211	T9	O	D	DCKM	Digital output timing clock (When using SLVS - EC, Hi - Z.)
212	T10	GND	D	VSSLIF	1.2 V GND
213	T11	O	D	DOM4	SLVS / SLVS - EC IF output (Data)
214	T12	O	D	DOM5	SLVS / SLVS - EC IF output (Data)
215	T13	O	D	DOM6	SLVS / SLVS - EC IF output (Data)
216	T14	O	D	DOM7	SLVS / SLVS - EC IF output (Data)
217	U1	—	—	N.C.	—
218	U3	—	—	N.C.	—
219	U4	O	D	DOP0	SLVS / SLVS - EC IF output (Data)
220	U5	O	D	DOP1	SLVS / SLVS - EC IF output (Data)
221	U6	O	D	DOP2	SLVS / SLVS - EC IF output (Data)
222	U7	O	D	DOP3	SLVS / SLVS - EC IF output (Data)
223	U8	GND	D	VSSLIF	1.2 V GND
224	U9	O	D	DCKP	Digital output timing clock (When using SLVS - EC, Hi - Z.)
225	U10	GND	D	VSSLIF	1.2 V GND
226	U11	O	D	DOP4	SLVS / SLVS - EC IF output (Data)
227	U12	O	D	DOP5	SLVS / SLVS - EC IF output (Data)
228	U13	O	D	DOP6	SLVS / SLVS - EC IF output (Data)
229	U14	O	D	DOP7	SLVS / SLVS - EC IF output (Data)
230	U16	—	—	N.C.	—

* N.C. pins in the table above should be left open on the board.

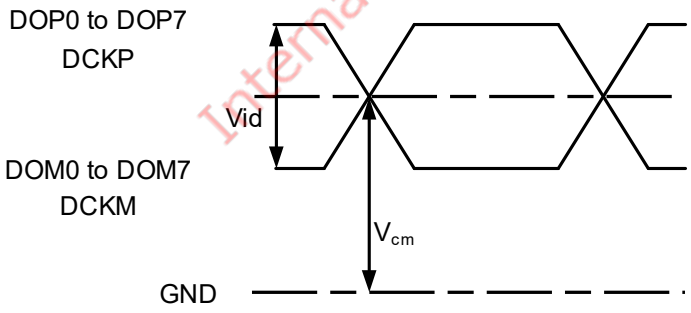
Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}Hx	AV_{DD}	—	3.15	3.30	3.45	V
	Interface	V_{DD}Mx	OV_{DD}	—	1.70	1.80	1.90	V
	Digital	V_{DD}Lx	DV_{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE SCK SDI XCE XTRIG1 XTRIG2 OMODE	VIH	XVS / XHS in Slave mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS SDO TOUT0 TOUT1 TOUT2	VOH	XVS / XHS in Master mode	OV_{DD} -0.4	—	—	V
			VOL		—	—	0.4	V

SLVS Output DC Characteristics

Single end output



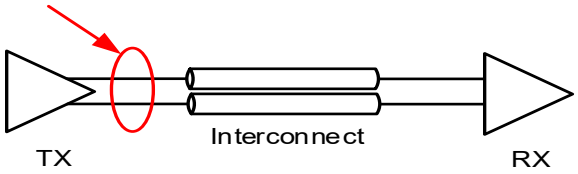
Definition of the characteristics of SLVS (Single end output)

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
Ro	Sensor output impedance	30	—	60	Ω	—
Vcm	Voltage center	150	—	250	mV	*1
|Vid|	Differential voltage	140	—	300	mV	*1

*1 Rin = 100Ω.

SLVS - EC Output DC Characteristics

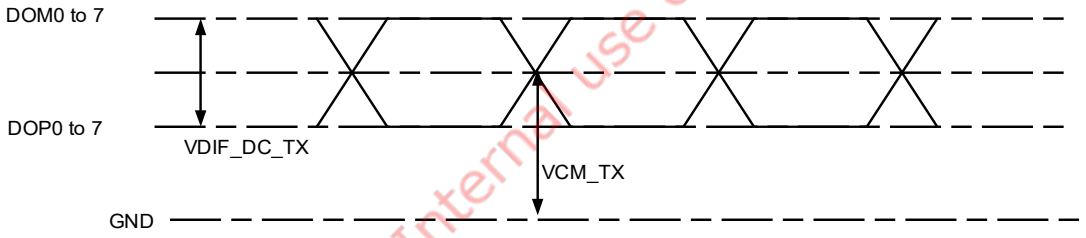
The characteristics of the TX of SLVS - EC are defined in the characteristic at the output pin of the package as shown in figure below.



Definition of the characteristics of SLVS - EC

Refer to “SLVS - EC Specification Version 1.2” for detail.
(Note: Data rate and CLK frequency are different from SLVS - EC Specification.)

Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit
Digital output voltage	DOP0 to DOP7, DOM0 to DOM7	Differential DC Voltage	VDIF_DC_TX	160	—	280	mV
		Common Mode Voltage	VCM_TX	160	—	260	mV
		Single-ended Output Resistance	RSED_TX	30	—	60	Ω



DC output of TX of SLVS - EC

Power Consumption

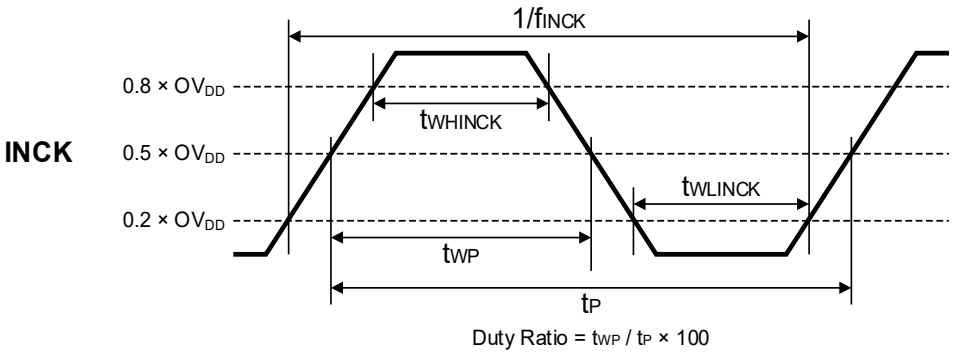
Item	Pins	Symbol	Typ.	Max.	Unit
Operating current SLVS 8 ch 12 bit 121 frame/s	$V_{DD}H$	IAV_{DD}	215	300	mA
	$V_{DD}M$	IOV_{DD}	1	2	mA
	$V_{DD}L$	IDV_{DD}	335	490	mA
Operating current SLVS - EC 8 Lane 12 bit 231 frame/s	$V_{DD}H$	IAV_{DD}	215	300	mA
	$V_{DD}M$	IOV_{DD}	1	2	mA
	$V_{DD}L$	IDV_{DD}	440	620	mA
Standby current	$V_{DD}H$	IAV_{DD}_STB	—	0.5	mA
	$V_{DD}M$	IOV_{DD}_STB	—	0.1	mA
	$V_{DD}L$	IDV_{DD}_STB	—	40	mA

Operating current:
(Typical value condition) : Supply voltage: 3.30 V / 1.80 V / 1.20 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

AC Characteristics

Master Clock (INCK) Waveform Diagram



Duty Ratio = t_{WP} / t_P × 100

When using SLVS

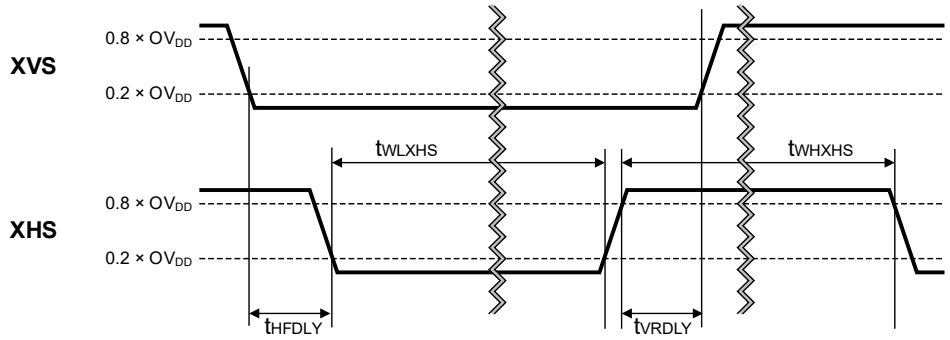
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	40.0	50.0	60.0	%	Define with 0.5 × OV_{DD}

When using SLVS - EC

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz, 54 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	40.0	50.0	60.0	%	Define with 0.5 × OV_{DD}
Clock frequency error	FERR	-300	—	300	ppm	
Phase noise (100 kHz)	PN100K	—	—	-135	dBc/Hz	
Phase noise (1 MHz)	PN1M	—	—	-140	dBc/Hz	

* The INCK fluctuation affects the frame rate.
* About SLVS - EC of this sensor, Data rate and CLK frequency are different from SLVS - EC Specification.

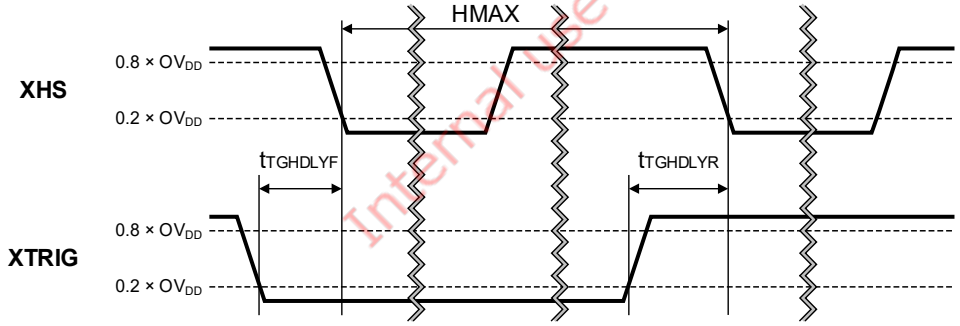
XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)



Item	Symbol	Min.	Typ.	Max.	Unit
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns
XVS - XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns
XHS - XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

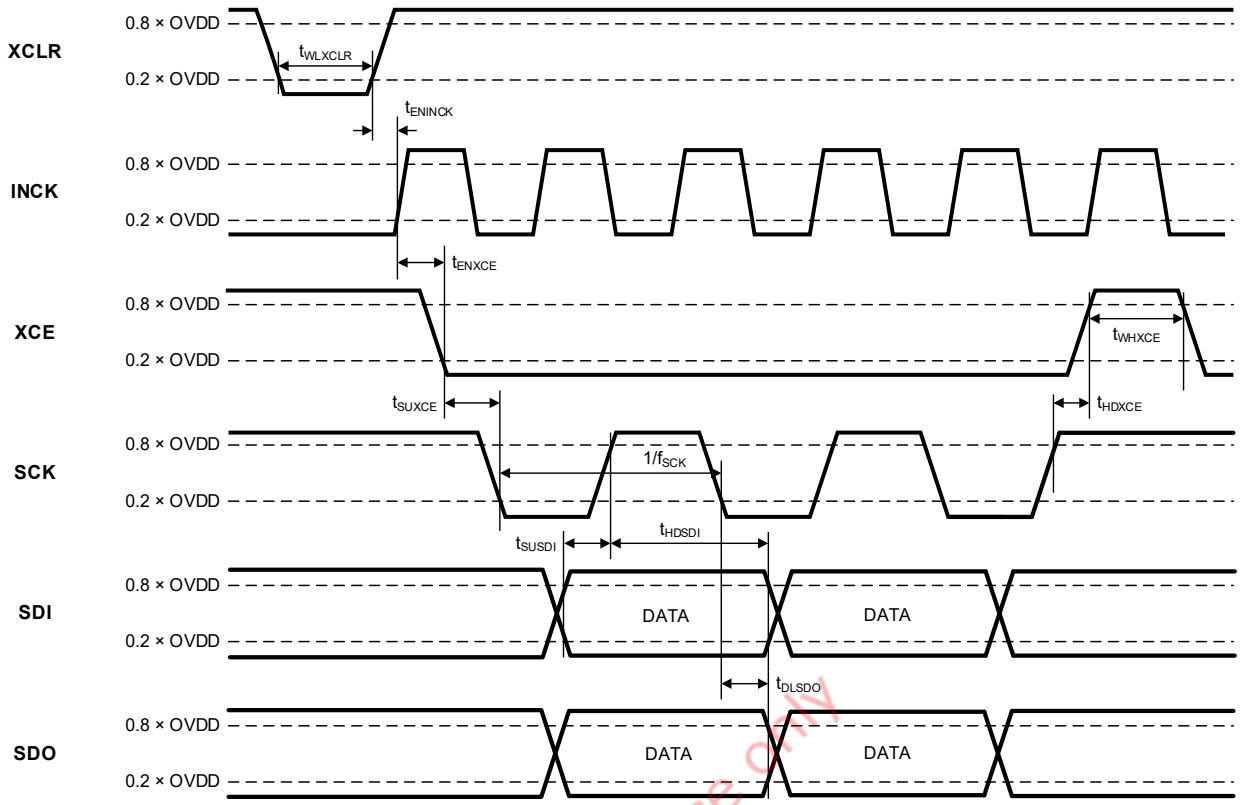
XTRIG Input Characteristics in Slave Mode (XMASTER = High) only



Item	Symbol	Min.	Typ.	Max.	Unit
XTRIG fall - XHS fall width	$t_{TGHDLYF}$	10	—	HMAX-10	INCK
XTRIG rise - XHS fall width	$t_{TGHDLYR}$	10	—	HMAX-10	INCK

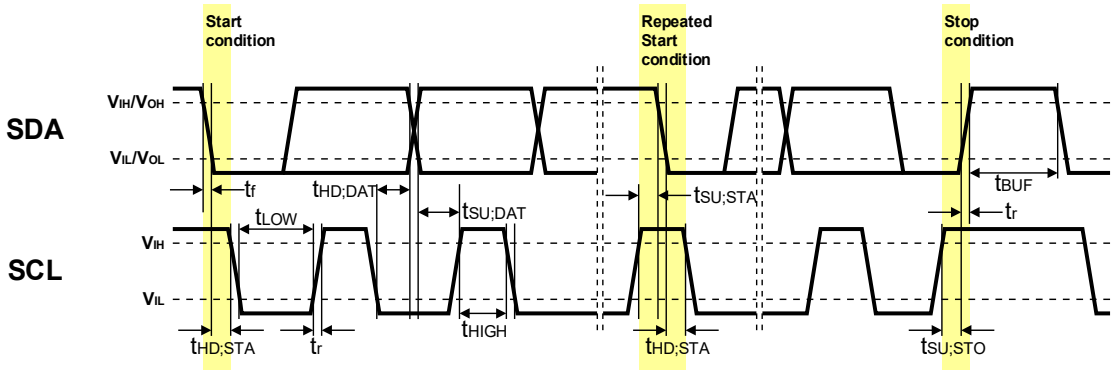
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level pulse width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
INCK effective margin	t_{ENINCK}	1	—	—	µs	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level pulse width	t_{WHXCE}	20	—	—	ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (/SCL) , SDI (/SDA)	Ci	—	—	10	pF	

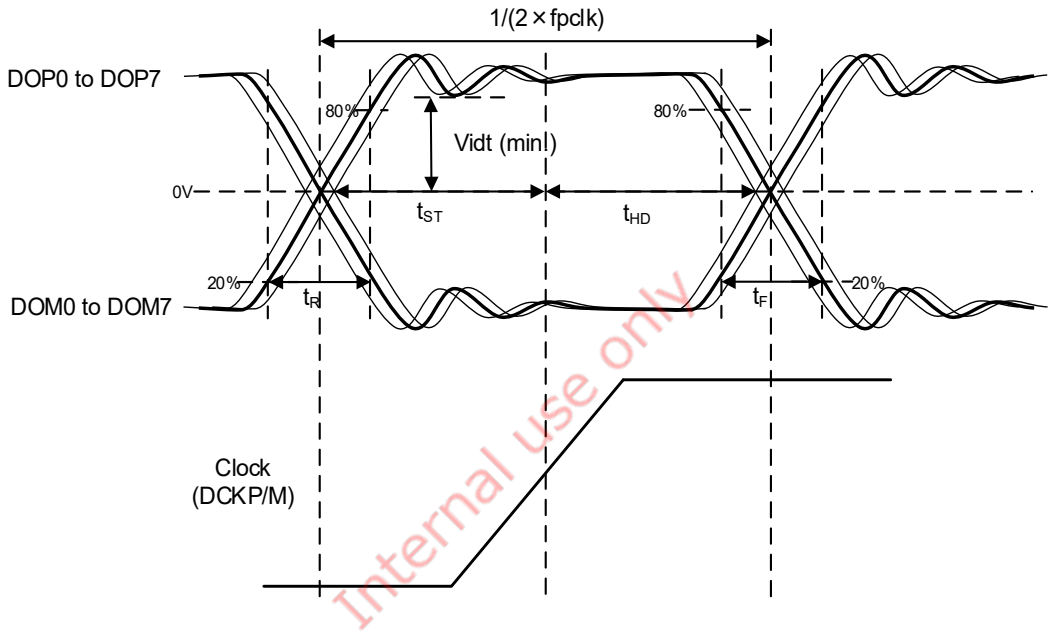
I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

SLVS Output AC Characteristics

Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
f_{clk}	Output frequency	—	594	—	Mbps	—
f_{pclk}	Clock frequency	—	297	—	MHz	—
t_{ST}	Setup time	505	—	—	ps	*1
t_{HD}	Hold time	505	—	—	ps	*1
t_R	DOP/DOM rise time	—	—	300	ps	*1, *2
t_F	DOP/DOM fall time	—	—	300	ps	*1, *2
|Vidt|	Differential voltage	140	—	—	mV	*1

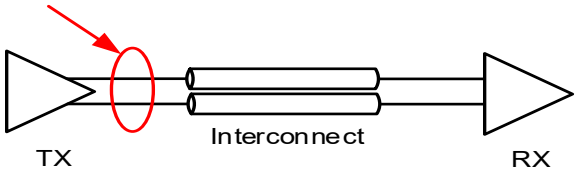
*1 Rin = 100Ω
*2 Differential 20% - 80%



Define of the characteristics of the SLVS

SLVS - EC Output AC Characteristics

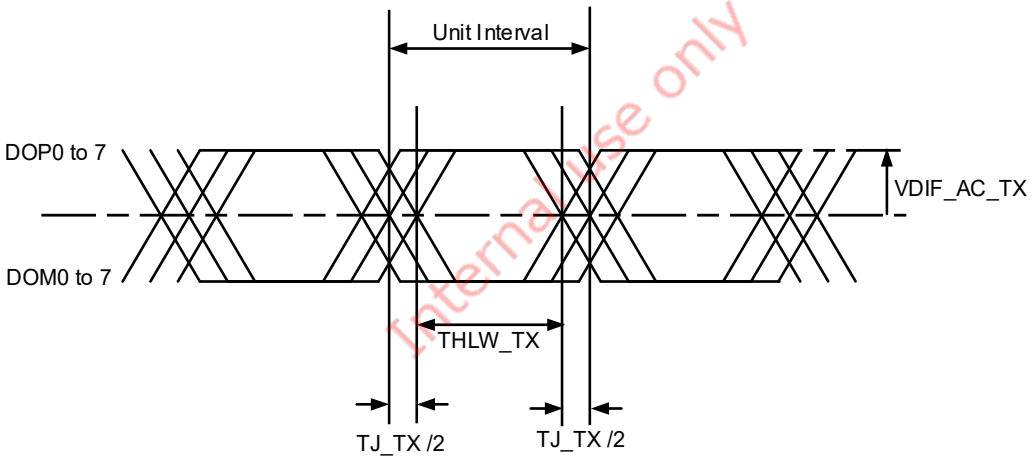
The characteristics of the TX of SLVS - EC are defined in the characteristic at the output pin of the package as shown in the figure below.



Define of the characteristics of the SLVS - EC

The details about SLVS - EC, please refer to the “SLVS - EC Specification Version 1.2”.
(Note: Data rate and CLK frequency are different from SLVS - EC Specification.)

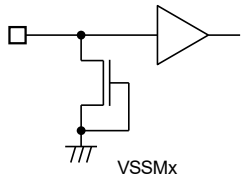
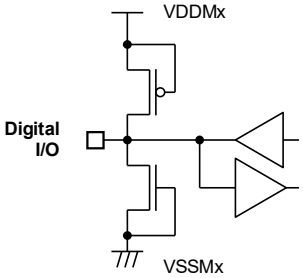
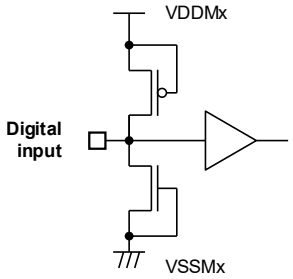
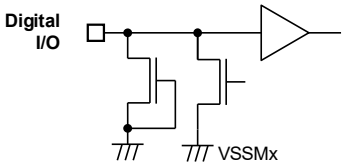
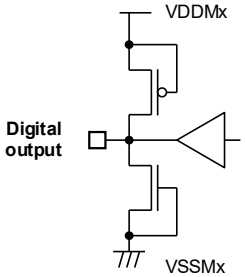
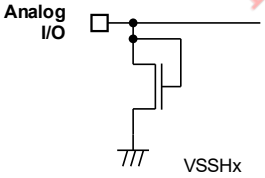
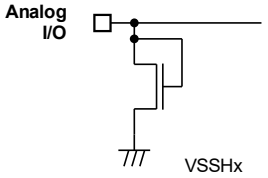
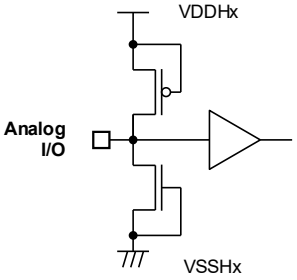
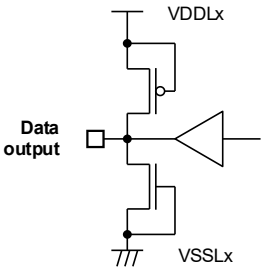
Item	Symbol	Min.	Typ.	Max.	Unit.	Remarks
Differential AC Voltage	VDIF_AC_TX	140	—	290	mV	100Ω differential onnection
Eye High/Low width	THLW_TX	0.2	—	—	UI	100Ω differential onnection
Deterministic Jitter	DJ_TX	—	—	0.3	UI	100Ω differential onnection
Total Jitter	TJ_TX	—	—	0.4	UI	100Ω differential onnection



AC output of TX in SLVS - EC

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR XCE XMASTER XTRIG1, 2 SLAMODE OMODE		SDI / SDA SCK / SCL	
SDO			
VCP1 VCP2		VRLOFG VRLTRX VRLTRY VRLSEL VRLTRG	
VBGR		DOPx DOMx DCKP DCKM x : 0 to 7	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

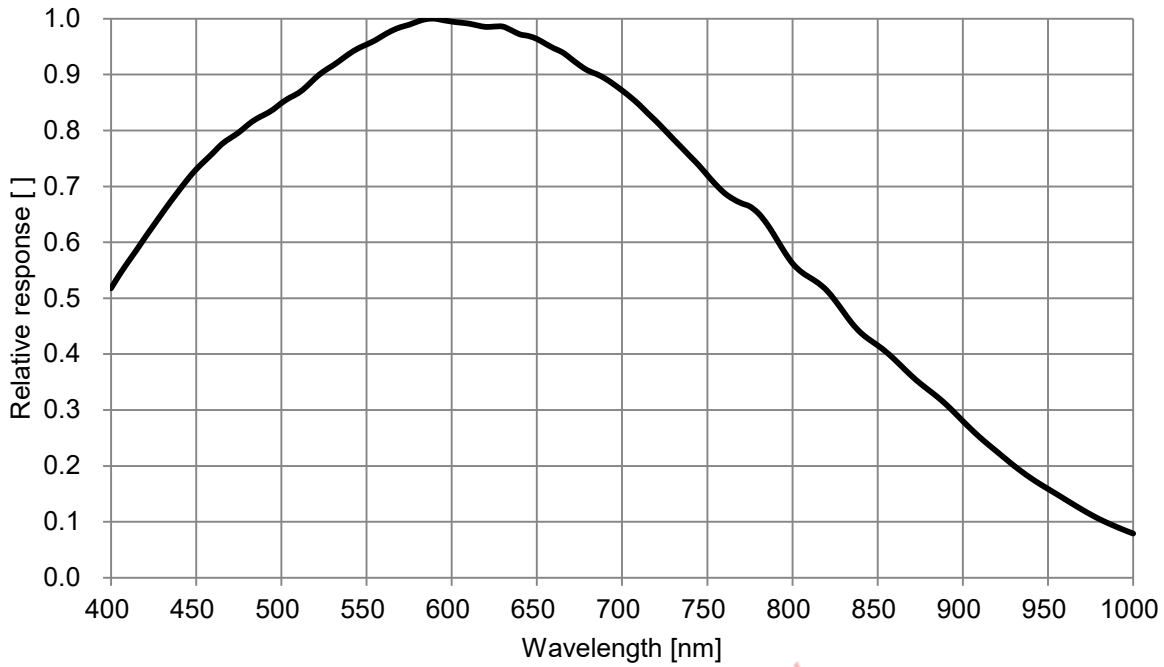


Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, All - pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	5828 (1425)	6859 (1677)	—	Digit (mV)	1	1/30 s storage, F8.0, 12 bit converted value, HCG mode
		2584 (632)	3042 (744)	—	Digit (mV)		1/30 s storage, F8.0, 12 bit converted value, LCG mode
Saturation signal	Vsat2D	4094 (1001*1)	—	—	Digit (mV)	2	Zone 0 to II' LCG mode
Video signal shading	SH01	—	—	20	%	3	Zone 0, I
	SH2D	—	—	25	%		Zone 0 to II'
Dark signal	Vdt	—	—	0.61 (0.15)	Digit (mV)	4	1/30 s storage HCG mode
Dark signal shading	ΔVdt	—	—	1.02 (0.25)	Digit (mV)	5	1/30 s storage HCG mode
PLS (Parasitic Light Sensitivity)	Sm	—	—	-93.9	dB	6	Zone II'
Conversion efficiency ratio	Rcg	—	2.3	—	—	7	HCG mode / LCG mode

Note) 1. Converted value into mV using 1Digit = 0.2445 mV for 12-bit output, 1Digit = 0.9779 mV for 10-bit output and 1Digit = 0.9779 mV for 8-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.
3. This sensor has Conversion efficiency setting. The characteristic is below.
HCG mode: High conversion efficiency mode.
LCG mode: Low conversion efficiency mode.

*1 In case of 8 bit, Vsat2D becomes 1/4 of it at 12 bit.

Zone Definition of Video Signal Shading

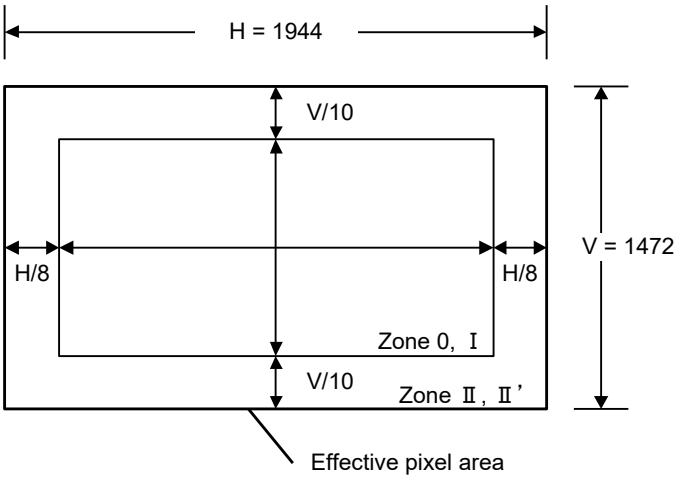


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the signal outputs (V) at the center of the screen, and substitute the values into the following formula.

   $$S = (V) \times 100 / 30 \text{ [mV]}$$

2. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal outputs, 419 mV, measure the minimum values of the signal outputs.

3. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the signal outputs is 419 mV. Then measure the maximum value (Vmax [mV]) and the minimum value (Vmin [mV]) of the signal outputs, and substitute the values into the following formula.

   $$SH = (Vmax - Vmin) / 419 \times 100 \text{ [\%]}$$

4. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/3 s integration at 3 frame/s and 1/30 s integration at 30 frame/s by 9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

5. Dark signal shading
   Measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output with the device junction temperature of 60 ˚C and the device in the light-obstructed state and 1/30 s integration. The measuring values substitute into the following formula.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

6. PLS
   Set the measurement condition to the standard imaging condition II, the output signal Vave measured by standard image condition. Then, adjust the luminous intensity to 500 times the intensity with average value of the signal output, Vave. When the charge drain is executed be the electronic shutter and the condition that not be readout from photo diode to analog memory, readout by dropping to 1/113 frame rate.

   $$Sm = 20 \times \log ((Vsm / Vave) \times (1 / 500) \times (1 / 113)) \text{ [dB]}$$

7. Conversion efficiency ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the signal outputs to 419 mV at the LCG mode, measure the average values of signal output and calculate the ratio between HCG mode and LCG mode.

Setting Registers Using Serial Communication

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

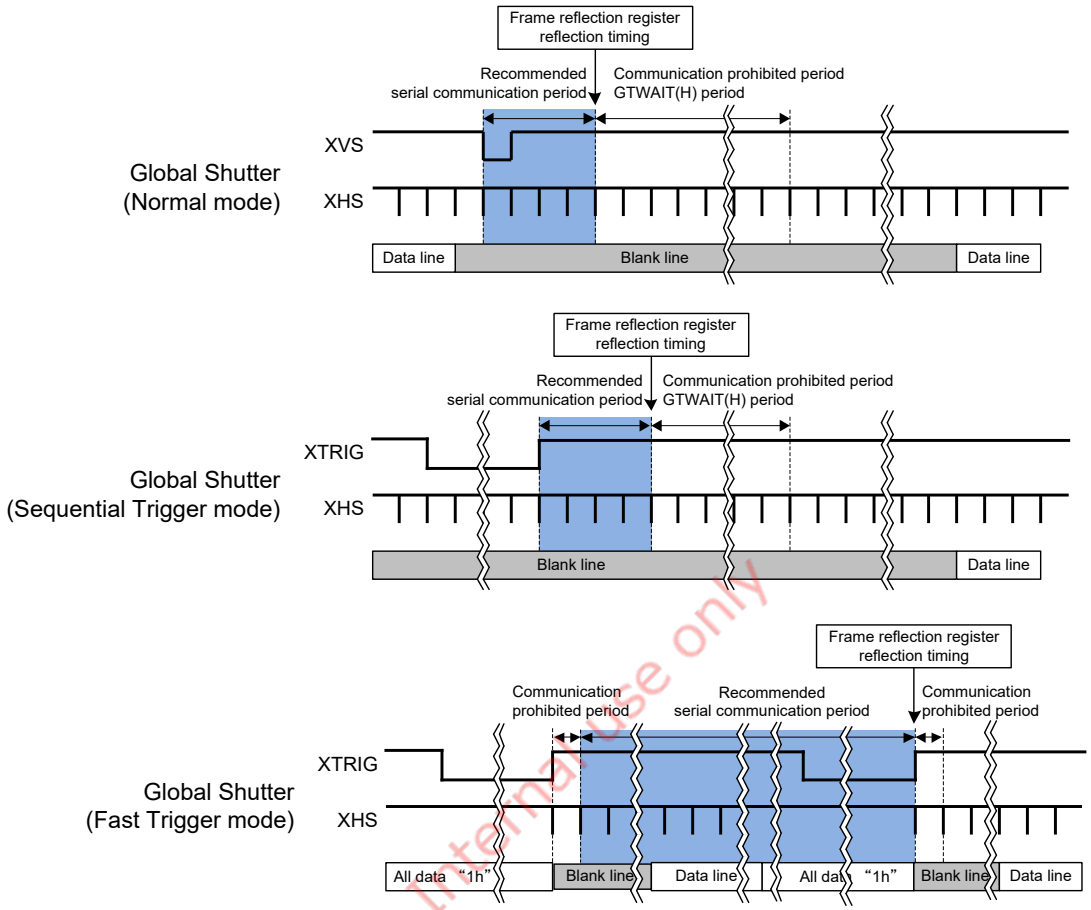
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	Chip ID: 02 Write: 02h / Read: 82h
	Chip ID: 03 Write: 03h / Read: 83h
	Chip ID: 04 Write: 04h / Read: 84h
	Chip ID: 05 Write: 05h / Read: 85h
	Chip ID: 06 Write: 06h / Read: 86h
	Chip ID: 07 Write: 07h / Read: 87h
	Chip ID: 08 Write: 08h / Read: 88h
	Chip ID: 09 Write: 09h / Read: 89h
	Chip ID: 0A Write: 0Ah / Read: 8Ah
	Chip ID: 0B Write: 0Bh / Read: 8Bh
	Chip ID: 0C Write: 0Ch / Read: 8Ch
	Chip ID: 10 Write: 10h / Read: 90h
	Chip ID: 11 Write: 11h / Read: 91h
	Chip ID: 12 Write: 12h / Read: 92h
	Chip ID: 13 Write: 13h / Read: 93h
	Chip ID: 14 Write: 14h / Read: 94h
	Chip ID: 15 Write: 15h / Read: 95h
	Chip ID: 16 Write: 16h / Read: 96h
	Chip ID: 17 Write: 17h / Read: 97h
	Chip ID: 18 Write: 18h / Read: 98h
	Chip ID: 19 Write: 19h / Read: 99h
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed.
Refer to GTWAIT table in “Global Shutter (Normal Mode) Operation” item about GTWAIT.



Register Write and Read (4-wire)

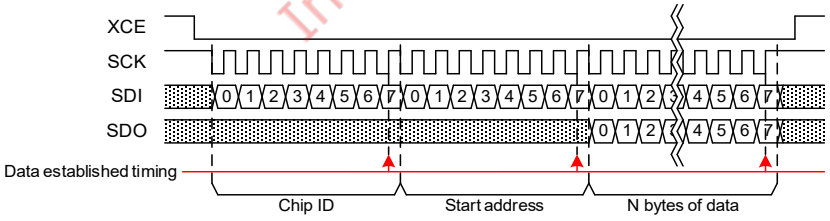
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 0Ch, 10h to 19h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

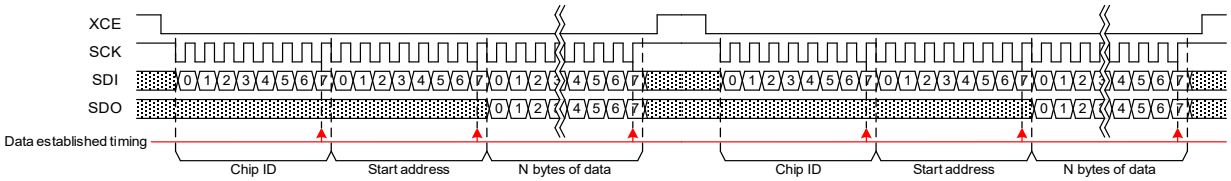
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 8Ch, 90h to 99h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



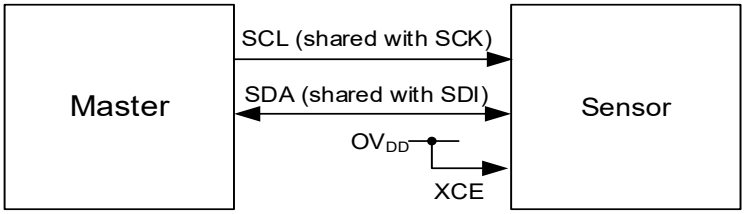
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

The sensor can use two kinds of slave addresses by switching the polarity of SLAMODE Pin for one I^2C bus, and can use a common slave address in both polarities of SLAMODE Pin for one I^2C bus.

SLAVE Address (SLAMODE = 0)

MSB							LSB
0	1	1	0	1	1	0	R / W

SLAVE Address (SLAMODE = 1)

MSB							LSB
0	1	1	0	1	1	1	R / W

SLAVE Address (SLAMODE = 0 / 1)

MSB							LSB
0	0	1	1	0	1	0	R / W

* R/W is data direction bit

R/W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

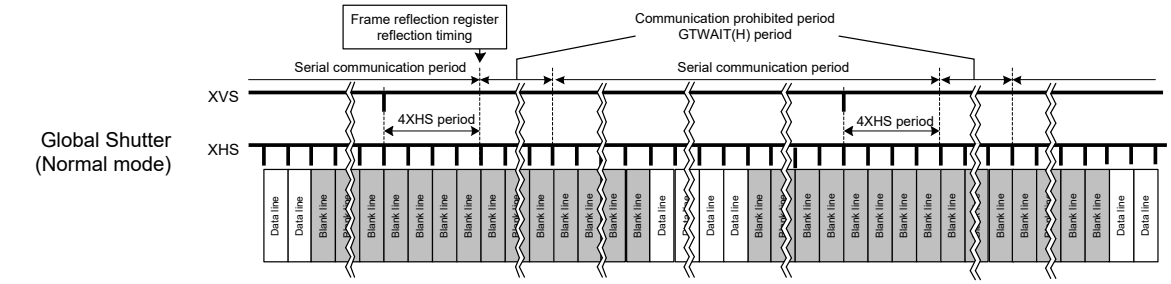
I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	J3	Serial clock input
SDA (common to SDI)	H3	Serial data communication

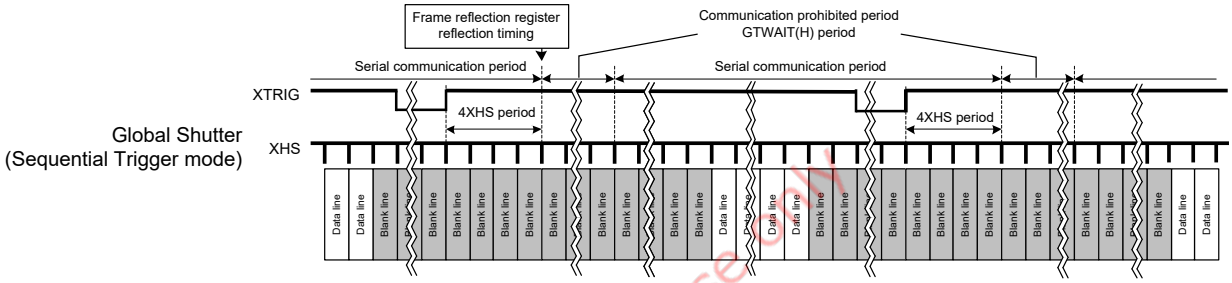
Register Communication Timing (I²C)

In I²C communication system, communication can be performed excluding the prohibited period as described in the below figure.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. Using REGHOLD function is recommended for register setting using I²C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.
Refer to GTWAIT table in “Global Shutter (Normal Mode) Operation” item about GTWAIT.

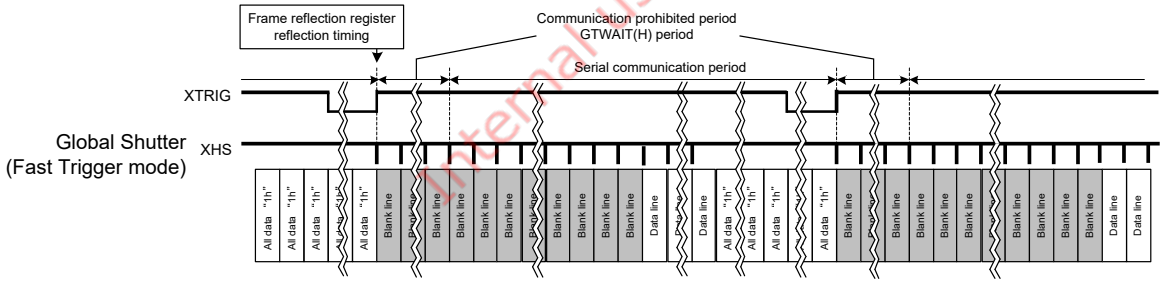
Global Shutter (Normal mode)



Global Shutter (Sequential Trigger mode)

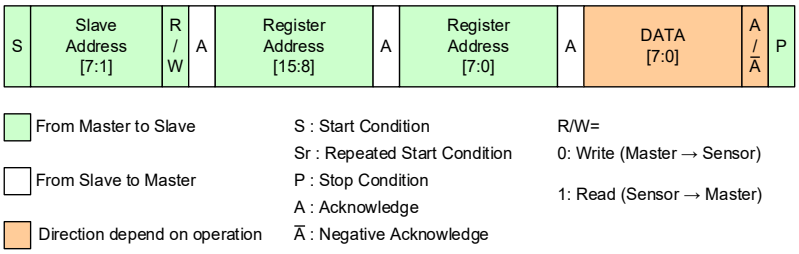


Global Shutter (Fast Trigger mode)



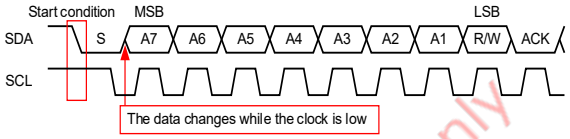
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

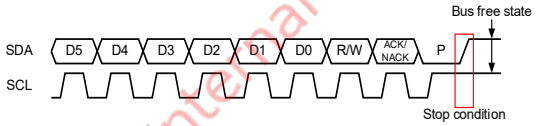


Communication protocol

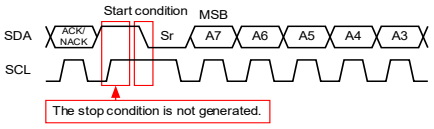
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

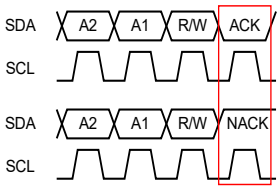


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



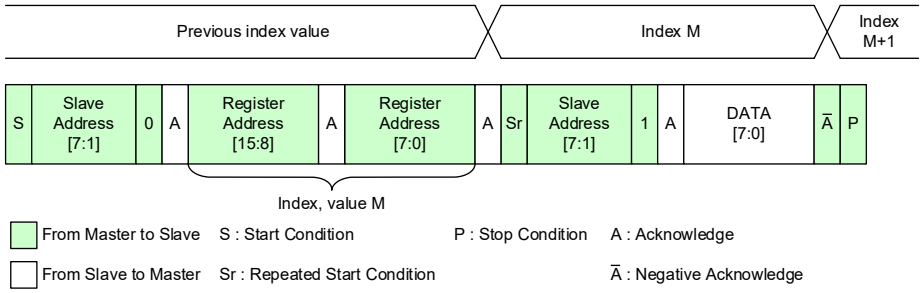
Acknowledge and Negative Acknowledge

I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

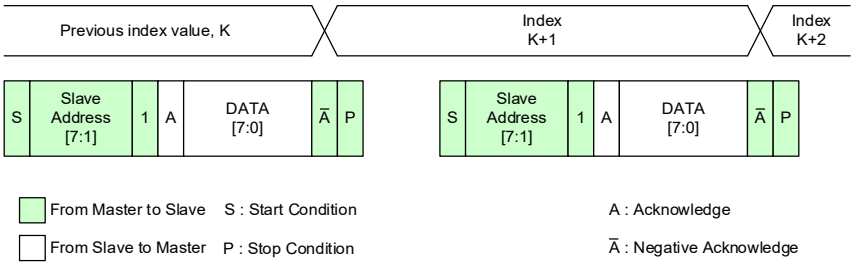
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

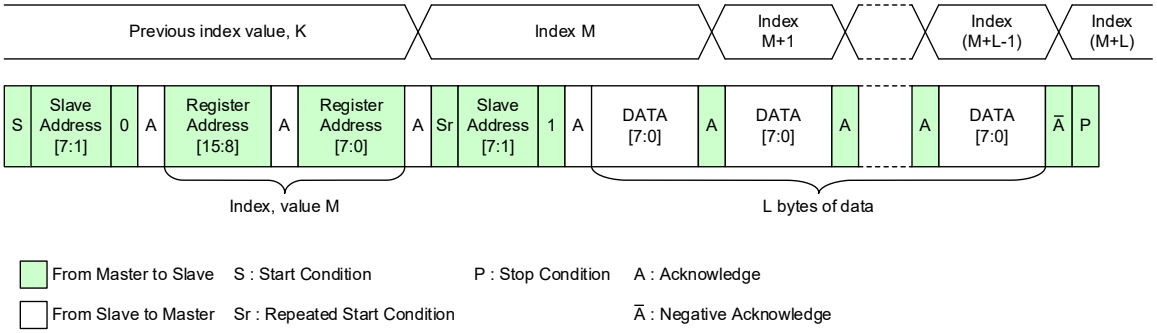
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

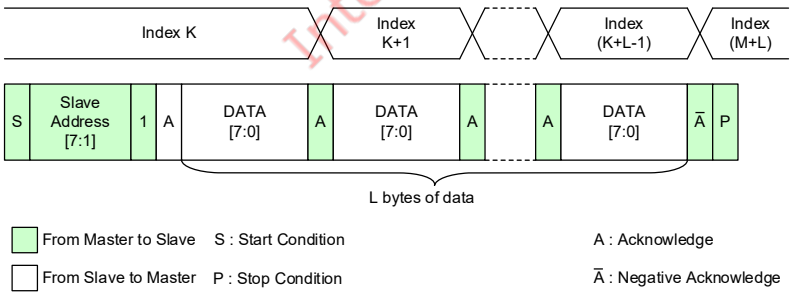
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

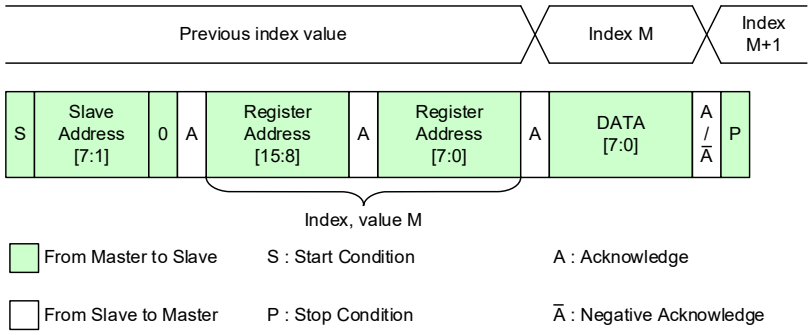
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

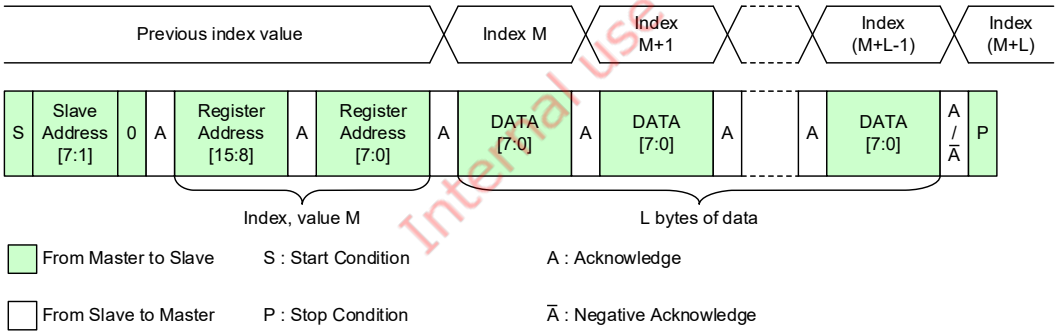
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 5376 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 0Ch, 10h to 19h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 5376 bytes.

There are three different register reflection timings.
About the Reflection timing column of the Register Map, registers noted as "I" are reflected immediately after writing to register, registers noted as "S" are set during standby mode and reflected after standby canceled, registers noted as "V" are reflected at “Fame reflection register reflection timing” on the figure described in the section of “Setting Registers with Serial Communication”.

Do not perform communication to addresses and setting not listed in the Register Map. Doing so may result in operation errors.

Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, I²C: 30**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3000h	0	STANDBY [0]	Standby mode 0: Normal operation 1: Standby	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
0Ch	300Ch	0	XMSTA [0]	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1	01h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
34h	3034h	0	REGHOLD [0]	Register hold 0: Invalid 1: Valid	0	00h	I
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ch	303Ch	0	WINMODE [3:0]	Drive mode setting of V direction 0h: All-pixel mode. 1h: 1/2 Subsampling mode 2h: FD Binning, Ch: Full-HD Others: Setting prohibited	0h	00h	S
		1					
		2					
		3					
		4	HMODE [4]	Drive mode setting of H direction 0: All-pixel 1: 1/2 Subsampling mode	0		S
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
D0h	30D0h	0	VOPB_VBLK_HWIDTH [12:0]	VOPB effective area and V Blank width setting	0798h	98h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D1h	30D1h	0				07h	
		1					
		2					
		3					
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
D2h	30D2h	0	FINFO_HWIDTH [12:0]	FINFO width setting	0410h	10h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D3h	30D3h	0				04h	
		1					
		2					
		3					
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
D4h	30D4h	0	VMAX [23:0]	LSB	000618h	18h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
D5h	30D5h	0				06h	
		1					
		2					
		3		When sensor master mode vertical span setting. (Number of operation lines count from 1)			
		4					
		5					
		6					
		7					
D6h	30D6h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
D8h	30D8h	0	HMAX [15:0]	LSB	0080h	80h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7		When sensor master mode horizontal span setting. (Number of operation clocks count from 1)			
D9h	30D9h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
DCh	30DCh	0	FREQ [1:0]	Set to data rate. 0: Normal 1: Data rate 1/2 Others: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
E2h	30E2h	0	GTWAIT [7:0]	Refer to the register list in each Readout mode	18h	18h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
E3h	30E3h	0	GSDLY [7:0]	Refer to the register list in each Readout mode	14h	14h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, I²C: 31**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3100h	0		Fixed to 0	0	00h	—
		1	OVERLAP_ROI_EN [1]	Selection of ROI mode 0: ROI Mode 1: Overlap ROI Mode	0		S
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
04h	3104h	0	FID0_ROIH1ON [0]	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV1ON [1]	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH2ON [2]	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV2ON [3]	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH3ON [4]	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV3ON [5]	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH4ON [6]	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV4ON [7]	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable	0		I
05h	3105h	0	FID0_ROIH5ON [0]	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable	0	00h	V
		1	FID0_ROIV5ON [1]	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable	0		I
		2	FID0_ROIH6ON [2]	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		3	FID0_ROIV6ON [3]	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable	0		I
		4	FID0_ROIH7ON [4]	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		5	FID0_ROIV7ON [5]	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable	0		I
		6	FID0_ROIH8ON [6]	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable	0		V
		7	FID0_ROIV8ON [7]	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable	0		I

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
20h	3120h	[7:0]	FID0_ROIPH1 [12:0]	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
21h	3121h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
22h	3122h	[7:0]	FID0_ROIPV1 [11:0]	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
23h	3123h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
24h	3124h	[7:0]	FID0_ROIWH1 [12:0]	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
25h	3125h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
26h	3126h	[7:0]	FID0_ROIWV1 [11:0]	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
27h	3127h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
28h	3128h	[7:0]	FID0_ROIPH2 [12:0]	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
29h	3129h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
2Ah	312Ah	[7:0]	FID0_ROIPV2 [11:0]	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
2Bh	312Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
2Ch	312Ch	[7:0]	FID0_ROIWH2 [12:0]	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
2Dh	312Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
2Eh	312Eh	[7:0]	FID0_ROIWV2 [11:0]	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
2Fh	312Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
30h	3130h	[7:0]	FID0_ROIPH3 [12:0]	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
31h	3131h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
32h	3132h	[7:0]	FID0_ROIPV3 [11:0]	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
33h	3133h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
34h	3134h	[7:0]	FID0_ROIWH3 [12:0]	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
35h	3135h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
36h	3136h	[7:0]	FID0_ROIWV3 [11:0]	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
37h	3137h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
38h	3138h	[7:0]	FID0_ROIPH4 [12:0]	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
39h	3139h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
3Ah	313Ah	[7:0]	FID0_ROIPV4 [11:0]	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
3Bh	313Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
3Ch	313Ch	[7:0]	FID0_ROIWH4 [12:0]	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
3Dh	313Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
3Eh	313Eh	[7:0]	FID0_ROIWV4 [11:0]	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
3Fh	313Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
40h	3140h	[7:0]	FID0_ROIPH5 [12:0]	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
41h	3141h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
42h	3142h	[7:0]	FID0_ROIPV5 [11:0]	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
43h	3143h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
44h	3144h	[7:0]	FID0_ROIWH5 [12:0]	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
45h	3145h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
46h	3146h	[7:0]	FID0_ROIWV5 [11:0]	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
47h	3147h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
48h	3148h	[7:0]	FID0_ROIPH6 [12:0]	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
49h	3149h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
4Ah	314Ah	[7:0]	FID0_ROIPV6 [11:0]	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
4Bh	314Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
4Ch	314Ch	[7:0]	FID0_ROIWH6 [12:0]	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
4Dh	314Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
4Eh	314Eh	[7:0]	FID0_ROIWV6 [11:0]	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
4Fh	314Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
50h	3150h	[7:0]	FID0_ROIPH7 [12:0]	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
51h	3151h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
52h	3152h	[7:0]	FID0_ROIPV7 [11:0]	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
53h	3153h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
54h	3154h	[7:0]	FID0_ROIWH7 [12:0]	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
55h	3155h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
56h	3156h	[7:0]	FID0_ROIWV7 [11:0]	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
57h	3157h	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
58h	3158h	[7:0]	FID0_ROIPH8 [12:0]	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8	0000h	00h	V
59h	3159h	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
5Ah	315Ah	[7:0]	FID0_ROIPV8 [11:0]	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
5Bh	315Bh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—
5Ch	315Ch	[7:0]	FID0_ROIWH8 [12:0]	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4	0000h	00h	V
5Dh	315Dh	[4:0]				00h	
		[7:5]		Fixed to 0h	0h		—
5Eh	315Fh	[7:0]	FID0_ROIWV8 [11:0]	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8	000h	00h	I
5Fh	315Fh	[3:0]				00h	
		[7:4]		Fixed to 0h	0h		—

Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C: 32**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3200h	0		0h: Except for Full HD 1h: 1080p - Full HD	0h	04h	S
		1					
		2		Fixed to 1	1		—
		3	HADD_ON [3]	H binning setting 0: H binning Off 1: H binning On	0		S
		4	HADD_ON_SEL [4]	H binning mode setting 0: H binning CLIP 1: H binning of average	0		S
		5	ADBIT [6:5]	AD conversion bits setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h		S
		6					
		7		Fixed to 0	0		—
04h	3204h	0	VREVERSE [0]	Vertical (V) direction readout inversion control 0: Normal 1: Inverted	0	00h	V
		1	HREVERSE [1]	Horizontal (H) direction readout inversion control 0: Normal 1: Inverted	0		V
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
20h	3220h	0	INCKSEL0 [7:0]	Set according to INCK frequency and drive mode.	52h	52h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3221h	0	INCKSEL1 [7:0]	Set according to INCK frequency and drive mode.	20h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
24h	3224h	0	INCKSEL2 [7:0]	Set according to INCK frequency and drive mode.	52h	52h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
25h	3225h	0	INCKSEL3 [7:0]	Set according to INCK frequency and drive mode.	20h	20h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
26h	3226h	0	FREQ_SYNC [7:0]	Refer to the register list in each Readout mode	83h	83h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
30h	3230h	0		Fixed to 1	1	39h	—
		1	FASTTRIG [1]	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode	0		S
		2		Refer to the register list in each Readout mode	0Eh		S
		3					
		4					
		5					
		6					
		7					
31h	3231h	0				00h	
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
32h	3232h	0	VINT_EN [0]	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable	1	03h	S
		1		Fixed to 1	1		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
40h	3240h	0	SHS [23:0]	LSB	000018h	18h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3241h	0				00h	
		1					
		2					
		3		Storage time adjustment Designated in line unit			
		4					
		5					
		6					
		7					
42h	3242h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, I²C: 33**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, I²C: 34**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
00h	3400h	0	TRIGEN [0]	Global shutter mode setting 0: Normal mode 1: Trigger mode	0	00h	I*1
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
30h	3430h	0	ODBIT [1:0]	Number of output bit setting 0h: 10 bit 1h: 12 bit 2h: 8 bit 3h: Setting prohibited	0h	00h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
35h	3435h	0	TOUT1SEL [1:0]	TOUT1 pin setting 0h: Low fixed 3h: Pulse output	0h	00h	S
		1					
		2	TOUT2SEL [3:2]	TOUT2 pin setting 0h: Low fixed 3h: Pulse output	0h		S
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ah	343Ah	0	TRIG_TOUT1_SEL [3:0]	TOUT1 output setting 0h: Low fixed 1h: Pulse1 output	0h	00h	S
		1					
		2					
		3					
		4	TRIG_TOUT2_SEL [7:4]	TOUT2 output setting 0h: Low fixed 2h: Pulse2 output	0h		S
		5					
		6					
		7					

*1 Refer to “Mode Transitions of Global Shutter Operation”

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
3Ch	343Ch	0		Fixed to 0	0	C0h	—
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4	SYNCSEL [5:4]	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z	0h		S
		5					
		6		Fixed to 1	1		—
		7		Fixed to 1	1		—
44h	3444h	0	STBSLVS [3:0]	Channel standby control of SLVS 1h: activate 8ch 2h: activate 4ch Others: Setting prohibited	1h	01h	S
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
45h	3445h	0	OPORTSEL [3:0]	SLVS channel selection 1h: 8 ch 3h: 4 ch Others: Setting prohibited	1h	01h	S
		1					
		2					
		3					
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
78h	3478h	0	PULSE1_EN_NOR [0]	Pulse1 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE1_EN_TRIG [1]	Pulse1 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE1_POL [2]	Pulse1 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
79h	3479h	0	PULSE1_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Ah	347Ah	0				00h	
		1					
		2					
		3		Pulse1 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
7Bh	347Bh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
7Ch	347Ch	0	PULSE1_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
7Dh	347Dh	0				00h	
		1					
		2					
		3		Pulse1 active period end timing setting Designated in line units from readout start (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
7Eh	347Eh	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
80h	3480h	0	PULSE2_EN_NOR [0]	Pulse2 output in normal mode 0: Disable 1: Enable	0	00h	S
		1	PULSE2_EN_TRIG [1]	Pulse2 output in trigger mode 0: Disable 1: Enable	0		S
		2	PULSE2_POL [2]	Pulse2 polarity selection 0: High active 1: Low active	0		S
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 1	0		S
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
81h	3481h	0	PULSE2_UP [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
82h	3482h	0				00h	
		1					
		2					
		3		Pulse2 active period start timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
83h	3483h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
84h	3484h	0	PULSE2_DN [23:0]	LSB	000000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
85h	3485h	0				00h	
		1					
		2					
		3		Pulse2 active period end timing setting Designated in line units from reference point (For details, see the “Pulse Output Function”)			
		4					
		5					
		6					
		7					
86h	3486h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			

Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, I²C: 35**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
02h	3502h	0	GAIN_RTS [7:0]	Setting of Gain Reflection Timing at Normal mode. 08h: Gain reflect at the frame 09h: Gain reflect at the next frame (Same timing as SHS reflecting output.) Others: Setting prohibited	00h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
10h	3510h	0	FDG_SEL [0]	Conversion gain switching 0: LCG Mode 1: HCG Mode	0	00h	V
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
14h	3514h	0	GAIN [8:0]	LSB Digital gain setting 0 dB (000d) to 48 dB (480d) 0.1 dB Step (Refer to Address 02h about detail of Reflection Timing.)	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
15h	3515h	0		MSB		00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
C0h	35C0h	0	BLKLEVEL [11:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4					
		5		Black level offset value setting Recommended value. 00Fh: 8 bit 03Ch: 10 bit 0F0h: 12 bit			
		6					
		7					
C1h	35C1h	0				00h	
		1					
		2					
		3		MSB			
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, I²C: 36**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, I²C: 37**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, I²C: 38**h)

Please refer to the other register map file for the register that has not been described.

Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, I²C: 39**h)

Please refer to the other register map file for the register that has not been described.

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
04h	3904h	0	LANESEL [2:0]	Setting of SLVS - EC output Lane 0h: 8Lane 2h: 4Lane 3h: 2Lane 4h: 1Lane Others: Setting prohibited	0h	00h	S
		1					
		2					
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
20h	3920h	0	CRC_EN [0]	CRC insertion at the end of line 0: Without CRC insertion 1: With CRC insertion	0	00h	S
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
21h	3921h	0	ECC_EN [1:0]	ECC insertion in lines 0h: Without ECC 1h: With ECC (parity 2 byte) 2h: With ECC (parity 4 byte) 3h: Setting prohibited	2h	02h	S
		1					
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
22h	3922h	0	INIT_LENGTH [4:0]	Set the length of low output period during mode change and initialization. (00h to 10h)	0Ah	0Ah	S
		1					
		2					
		3					
		4					
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
24h	3924h	0	SYNCCODE_LEN [23:0]	LSB	007FFFh	FFh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
25h	3925h	0		Sync Code transfer times 000001h: minimum		7Fh	
		1					
		2					
		3					
		4					
		5					
		6					
		7					
26h	3926h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
28h	3928h	0	DESKEWCODE_LEN [7:0]	Deskew Code transfer times 01h: minimum	10h	10h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
2Ah	392Ah	0	DESKEWCODE_INTVL [7:0]	Deskew Code transmission interval 04h: minimum Set the setting in multiple of 4.	10h	10h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
2Ch	392Ch	0	STBYCODE_LEN [7:0]	Standby Code transfer times 03h: minimum	10h	10h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
30h	3930h	0	SYNCCODE [8:0]	Set the symbol following the comma symbol within the standby code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	0AAh	AAh	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
31h	3931h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
32h	3932h	0	DESKEWCODE [8:0]	Set the symbol following the comma symbol within the Deskew Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	060h	60h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
33h	3933h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
34h	3934h	0	IDLECODE1 [8:0]	Set the 1st symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
35h	3935h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
36h	3936h	0	IDLECODE2 [8:0]	Set the 2nd symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
37h	3937h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
38h	3938h	0	IDLECODE3 [8:0]	Set the 3rd symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
39h	3939h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—
3Ah	393Ah	0	IDLECODE4 [8:0]	Set the 4th symbol for the Idle Code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	000h	00h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Bh	393Bh	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Address		bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
40h	3940h	0	STBYCODE [8:0]	Set the symbol following the comma symbol within the standby code bit[7:0] Any symbol bit[8] 0h: D character 1h: K character	003h	03h	S
		1					
		2					
		3					
		4					
		5					
		6					
		7					
41h	3941h	0				00h	
		1		Fixed to 0	0		—
		2		Fixed to 0	0		—
		3		Fixed to 0	0		—
		4		Fixed to 0	0		—
		5		Fixed to 0	0		—
		6		Fixed to 0	0		—
		7		Fixed to 0	0		—

Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, I²C: 3Ah)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, I²C: 40h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, I²C: 41h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, I²C: 42h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 13 (Write: Chip ID = 13h, Read: Chip ID = 93h, I²C: 43h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 14 (Write: Chip ID = 14h, Read: Chip ID = 94h, I²C: 44h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 15 (Write: Chip ID = 15h, Read: Chip ID = 95h, I²C: 45h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 16 (Write: Chip ID = 16h, Read: Chip ID = 96h, I²C: 46h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 17 (Write: Chip ID = 17h, Read: Chip ID = 97h, I²C: 47h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 18 (Write: Chip ID = 18h, Read: Chip ID = 98h, I²C: 48h)**

Please refer to the other register map file for the register that has not been described.

Chip ID = 19 (Write: Chip ID = 19h, Read: Chip ID = 99h, I²C: 49h)**

Please refer to the other register map file for the register that has not been described.

Readout Drive Modes

The table below lists the operating modes available with this sensor. (Each value is the Max. frame rate of the each number of ch.)

FREQ (CID = 02h, Address = DCh, [1:0]) = 0h

When SLVS output

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS ch[*1]	A/D conversion	Number of recording pixels		Total number of pixels (Average)[*2]		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	174.6	4.752	8	8	1936	1464	2208.0	1540	138.0	276.0	200.8
	93.5	2.376	4				2072.0	1532	259.0	518.0	376.8
	143.0	4.752	8	10			2163.2	1536	169.0	338.0	245.9
	75.4	2.376	4				2054.4	1532	321.0	642.0	467.0
	121.1	4.752	8	12			2133.4	1532	200.0	400.0	291.0
	63.4	2.376	4				2042.7	1528	383.0	766.0	557.1
All pixel (Vertical / Horizontal 1/2 subsampling)	596.7	4.752	8	8	968	732	1232.0	808	77.0	154.0	112.0
	337.9	2.376	4				1104.0	796	138.0	276.0	200.8
	498.9	4.752	8	10			1190.4	800	93.0	186.0	135.3
	277.3	2.376	4				1081.6	792	169.0	338.0	245.9
	425.7	4.752	8	12			1162.7	800	109.0	218.0	158.6
	235.5	2.376	4				1066.7	788	200.0	400.0	291.0
2 × 2 Vertical FD binning mode	599.6	4.752	8	8	968	732	1232.0	804	77.0	154.0	112.0
	339.6	2.376	4				1104.0	792	138.0	276.0	200.8
	501.5	4.752	8	10			1190.4	796	93.0	186.0	135.3
	278.7	2.376	4				1081.6	788	169.0	338.0	245.9
	427.8	4.752	8	12			1162.7	796	109.0	218.0	158.6
	236.7	2.376	4				1066.7	784	200.0	400.0	291.0
HD 1080p	120.0	3.564	8	10	1920	1080	2640.0	1125	275.0	550.0	—
	60.0	1.782	4				2640.0		550.0	1100.0	—
	120.0	3.564	8	12			2200.0		275.0	550.0	—
	60.0	1.782	4				2200.0		550.0	1100.0	—
ROI	[*4]	4.752	8	8	[*3]	[*3]	2208.0	[*4]	138.0	276.0	200.8
	[*4]	2.376	4				2072.0		259.0	518.0	376.8
	[*4]	4.752	8	10			2163.2		169.0	338.0	245.9
	[*4]	2.376	4				2054.4		321.0	642.0	467.0
	[*4]	4.752	8	12			2133.4		200.0	400.0	291.0
	[*4]	2.376	4				2042.7		383.0	766.0	557.1

When SLVS - EC output

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS - EC Lane*1	A/D conversion	Number of recording pixels		Total number of pixels (Average)*2		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	409.2	19.008	8	8	1936	1464	3712.0	1564	58.0	116.0	84.4
	263.5	9.504	4				2912.0	1548	91.0	182.0	132.4
	138.4	4.752	2				2800.0	1532	175.0	350.0	254.6
	70.8	2.376	1				2736.0	1532	342.0	684.0	497.5
	371.8	19.008	8	10			3276.8	1560	64.0	128.0	93.1
	216.6	9.504	4				2841.6	1544	111.0	222.0	161.5
	112.7	4.752	2				2752.0	1532	215.0	430.0	312.8
	57.4	2.376	1				2707.2	1528	423.0	846.0	615.3
	231.2	19.008	8	12			4437.4	1544	104.0	208.0	151.3
	182.6	9.504	4				2816.0	1540	132.0	264.0	192.0
	94.6	4.752	2				2730.7	1532	256.0	512.0	372.4
	48.2	2.376	1				2688.0	1528	504.0	1008.0	733.1
All pixel (Vertical / Horizontal 1/2 subsampling)	780.5	19.008	8	8	968	732	3712.0	820	58.0	116.0	84.4
	780.5	9.504	4				1856.0	820	58.0	116.0	84.4
	493.6	4.752	2				1504.0	800	94.0	188.0	136.8
	261.7	2.376	1				1440.0	788	180.0	360.0	261.9
	710.8	19.008	8	10			3276.8	816	64.0	128.0	93.1
	710.8	9.504	4				1638.4	816	64.0	128.0	93.1
	407.0	4.752	2				1459.2	800	114.0	228.0	165.9
	214.1	2.376	1				1408.0	788	220.0	440.0	320.0
	446.2	19.008	8	12			4437.4	800	104.0	208.0	151.3
	446.2	9.504	4				2218.7	800	104.0	208.0	151.3
	348.0	4.752	2				1429.4	796	134.0	268.0	195.0
	180.5	2.376	1				1392.0	788	261.0	522.0	379.7
2 × 2 Vertical FD binning mode	784.4	19.008	8	8	968	732	3712.0	816	58.0	116.0	84.4
	784.4	9.504	4				1856.0	816	58.0	116.0	84.4
	496.1	4.752	2				1504.0	796	94.0	188.0	136.8
	263.0	2.376	1				1440.0	784	180.0	360.0	261.9
	714.3	19.008	8	10			3276.8	812	64.0	128.0	93.1
	714.3	9.504	4				1638.4	812	64.0	128.0	93.1
	409.1	4.752	2				1459.2	796	114.0	228.0	165.9
	215.2	2.376	1				1408.0	784	220.0	440.0	320.0
	448.4	19.008	8	12			4437.4	796	104.0	208.0	151.3
	448.4	9.504	4				2218.7	796	104.0	208.0	151.3
	349.8	4.752	2				1429.4	792	134.0	268.0	195.0
	181.4	2.376	1				1392.0	784	261.0	522.0	379.7
ROI	*4	19.008	8	8	*3	*3	3712.0	*4	58.0	116.0	84.4
	*4	9.504	4				2912.0		91.0	182.0	132.4
	*4	4.752	2				2800.0		175.0	350.0	254.6
	*4	2.376	1				2736.0		342.0	684.0	497.5
	*4	19.008	8	10			3276.8		64.0	128.0	93.1
	*4	9.504	4				2841.6		111.0	222.0	161.5
	*4	4.752	2				2752.0		215.0	430.0	312.8
	*4	2.376	1				2707.2		423.0	846.0	615.3
	*4	19.008	8	12			4437.4		104.0	208.0	151.3
	*4	9.504	4				2816.0		132.0	264.0	192.0
	*4	4.752	2				2730.7		256.0	512.0	372.4
	*4	2.376	1				2688.0		504.0	1008.0	733.1

*1 The data rate of each output Lane is value that is obtained by total data rate divided by the number of Lanes.
Example) In All - pixel 409.2 [frame/s] mode: 19.008 [Gbps] / 8 = 2376 [Mbps]

*2 It is possible that the blank pixel number of 1H changes by 1 pixel.
For the setting value to register HMAX / VMAX, see the section of each drive mode settings.

*3 Designated cropping area (ROI).

*4 See the section of “ROI mode”.

FREQ (CID = 02h, Address = DCh, [1:0]) = 1h

When SLVS output

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS ch[*1]	A/D conversion	Number of recording pixels		Total number of pixels (Average)[*2]		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	90.0	2.376	8	8	1936	1464	2152.0	1532	269.0	538.0	391.3
	47.4	1.188	4				2048.0	1528	512.0	1024.0	744.8
	73.2	2.376	8	10			2118.4	1532	331.0	662.0	481.5
	38.2	1.188	4				2032.0	1528	635.0	1270.0	923.7
	61.6	2.376	8	12			2101.4	1528	394.0	788.0	573.1
	32.0	1.188	4				2024.0	1528	759.0	1518.0	1104.0
All pixel (Vertical / Horizontal 1/2 subsampling)	317.2	2.376	8	8	968	732	1176.0	796	147.0	294.0	213.9
	175.1	1.188	4				1076.0	788	269.0	538.0	391.3
	263.2	2.376	8	10			1145.6	788	179.0	358.0	260.4
	142.3	1.188	4				1059.2	788	331.0	662.0	481.5
	222.2	2.376	8	12			1130.7	788	212.0	424.0	308.4
	120.1	1.188	4				1050.7	784	394.0	788.0	573.1
2 × 2 Vertical FD binning mode	318.8	2.376	8	8	968	732	1176.0	792	147.0	294.0	213.9
	176.0	1.188	4				1076.0	784	269.0	538.0	391.3
	264.5	2.376	8	10			1145.6	784	179.0	358.0	260.4
	143.0	1.188	4				1059.2	784	331.0	662.0	481.5
	223.3	2.376	8	12			1130.7	784	212.0	424.0	308.4
	120.8	1.188	4				1050.7	780	394.0	788.0	573.1
ROI	[*4]	2.376	8	8	[*3]	[*3]	2152.0	[*4]	269.0	538.0	391.3
	[*4]	1.188	4				2048.0		512.0	1024.0	744.8
	[*4]	2.376	8	10			2118.4		331.0	662.0	481.5
	[*4]	1.188	4				2032.0		635.0	1270.0	923.7
	[*4]	2.376	8	12			2101.4		394.0	788.0	573.1
	[*4]	1.188	4				2024.0		759.0	1518.0	1104.0

When SLVS - EC output

Drive mode	Frame rate [frame/s]	Data rate [Gbps]	SLVS - EC Lane*1	A/D conversion	Number of recording pixels		Total number of pixels (Average)*2		Number of INCK in 1H		
					H	V	H	V	INCK: 37.125 MHz	INCK: 74.25 MHz	INCK: 54 MHz
All pixel	242.8	9.504	8	8	1936	1464	3168.0	1544	99.0	198.0	144.0
	133.8	4.752	4				2896.0	1532	181.0	362.0	263.3
	69.6	2.376	2				2784.0	1532	348.0	696.0	506.2
	35.6	1.188	1				2728.0	1528	682.0	1364.0	992.0
	202.5	9.504	8	10			3046.4	1540	119.0	238.0	173.1
	109.6	4.752	4				2828.8	1532	221.0	442.0	321.5
	56.6	2.376	2				2745.6	1528	429.0	858.0	624.0
	28.8	1.188	1				2700.8	1524	844.0	1688.0	1227.7
	173.4	9.504	8	12			2965.4	1540	139.0	278.0	202.2
	92.4	4.752	4				2794.7	1532	262.0	524.0	381.1
	47.6	2.376	2				2720.0	1528	510.0	1020.0	741.9
	24.2	1.188	1				2682.7	1524	1006.0	2012.0	1463.3
All pixel (Vertical / Horizontal 1/2 subsampling)	780.5	9.504	8	8	968	732	1856.0	820	58.0	116.0	84.4
	464.0	4.752	4				1600.0	800	100.0	200.0	145.5
	253.3	2.376	2				1488.0	788	186.0	372.0	270.6
	132.2	1.188	1				1432.0	784	358.0	716.0	520.8
	672.3	9.504	8	10			1740.8	812	68.0	136.0	99.0
	388.6	4.752	4				1536.0	796	120.0	240.0	174.6
	208.4	2.376	2				1446.4	788	226.0	452.0	328.8
	107.8	1.188	1				1404.8	784	439.0	878.0	638.6
	446.2	9.504	8	12			2218.7	800	104.0	208.0	151.3
	333.1	4.752	4				1493.4	796	140.0	280.0	203.7
	176.4	2.376	2				1424.0	788	267.0	534.0	388.4
	91.0	1.188	1				1386.7	784	520.0	1040.0	756.4
2 × 2 Vertical FD binning mode	784.4	9.504	8	8	968	732	1856.0	816	58.0	116.0	84.4
	466.3	4.752	4				1600.0	796	100.0	200.0	145.5
	254.5	2.376	2				1488.0	784	186.0	372.0	270.6
	132.9	1.188	1				1432.0	780	358.0	716.0	520.8
	675.6	9.504	8	10			1740.8	808	68.0	136.0	99.0
	390.6	4.752	4				1536.0	792	120.0	240.0	174.6
	209.5	2.376	2				1446.4	784	226.0	452.0	328.8
	108.4	1.188	1				1404.8	780	439.0	878.0	638.6
	448.4	9.504	8	12			2218.7	796	104.0	208.0	151.3
	334.8	4.752	4				1493.4	792	140.0	280.0	203.7
	177.3	2.376	2				1424.0	784	267.0	534.0	388.4
	91.5	1.188	1				1386.7	780	520.0	1040.0	756.4
ROI	*4	9.504	8	8	*3	*3	3168.0	*4	99.0	198.0	144.0
	*4	4.752	4				2896.0		181.0	362.0	263.3
	*4	2.376	2				2784.0		348.0	696.0	506.2
	*4	1.188	1				2728.0		682.0	1364.0	992.0
	*4	9.504	8	10			3046.4		119.0	238.0	173.1
	*4	4.752	4				2828.8		221.0	442.0	321.5
	*4	2.376	2				2745.6		429.0	858.0	624.0
	*4	1.188	1				2700.8		844.0	1688.0	1227.7
	*4	9.504	8	12			2965.4		139.0	278.0	202.2
	*4	4.752	4				2794.7		262.0	524.0	381.1
	*4	2.376	2				2720.0		510.0	1020.0	741.9
	*4	1.188	1				2682.7		1006.0	2012.0	1463.3

*1 The data rate of each output Lane is value that is obtained by total data rate divided by the number of Lanes.
Example) In All - pixel 242.8 [frame/s] mode: 9.504 [Gbps] / 8 = 1188 [Mbps]

*2 It is possible that the blank pixel number of 1H changes by 1 pixel.
For the setting value to register HMAX / VMAX, see the section of each drive mode settings.

*3 Designated cropping area (ROI).

*4 See the section of “ROI mode”.

Restriction on Image Data Output

If the shutter releases on outputting the image data in this product, blank or Idle Code is inserted in the imade data because of shutter stabilization wait time. Shutter stabilization wait time depends on the readout mode.
The insertion timing of shutter stabilization wait time changes depending on the shutter release timing.
During the shutter stabilization wait time, the sync codes (SLVS) or Start Code, End Code and Packet Header (SLVS - EC) is not output. Refer to the sync codes or Start Code, End Code and Packet Header from the sensor and perform synchronization.

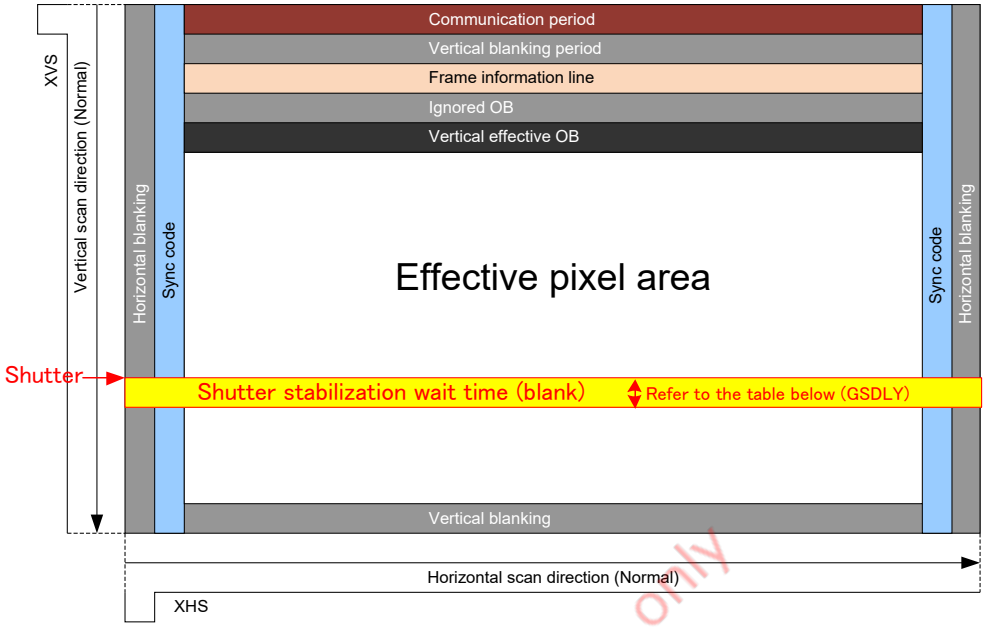


Image Drawing of Sutter stabilization wait time inserted (SLVS output)

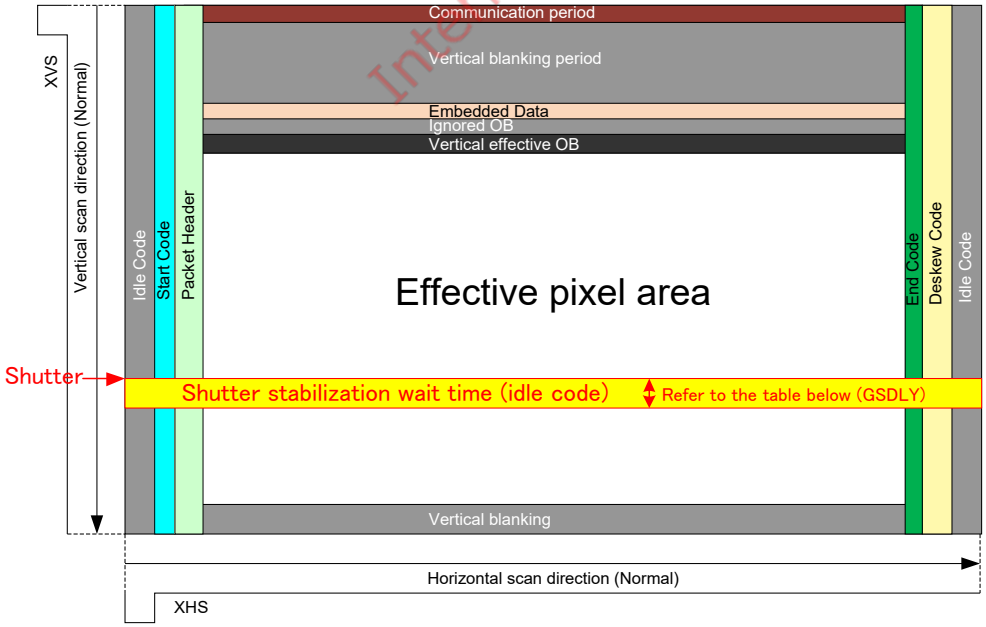


Image Drawing of Sutter stabilization wait time inserted (SLVS - EC output)

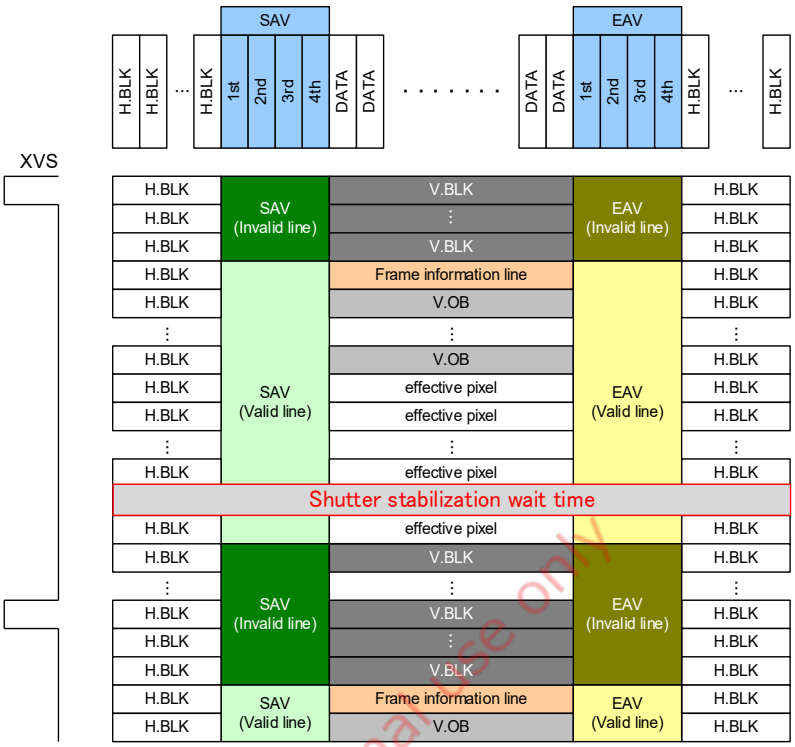
Refer to GSDLY table in “Global Shutter (Normal Mode) Operation” item about Shutter stabilization wait time.

Image Data Output Format

SLVS Output Format

Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



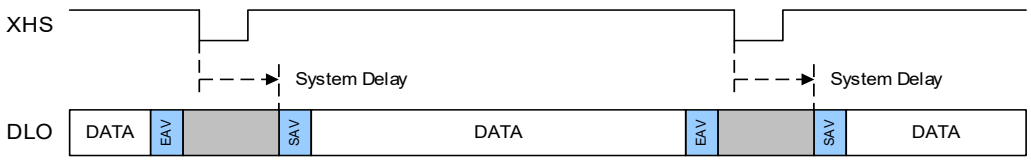
Sync Code Output Timing

List of Sync Code

Sync code	1st code			2nd code			3rd code			4th code		
	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
SAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	80h	200h	800h
EAV (Valid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	9Dh	274h	9D0h
SAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	ABh	2ACh	AB0h
EAV (Invalid line)	FFh	3FFh	FFFh	00h	000h	000h	00h	000h	000h	B6h	2D8h	B60h

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



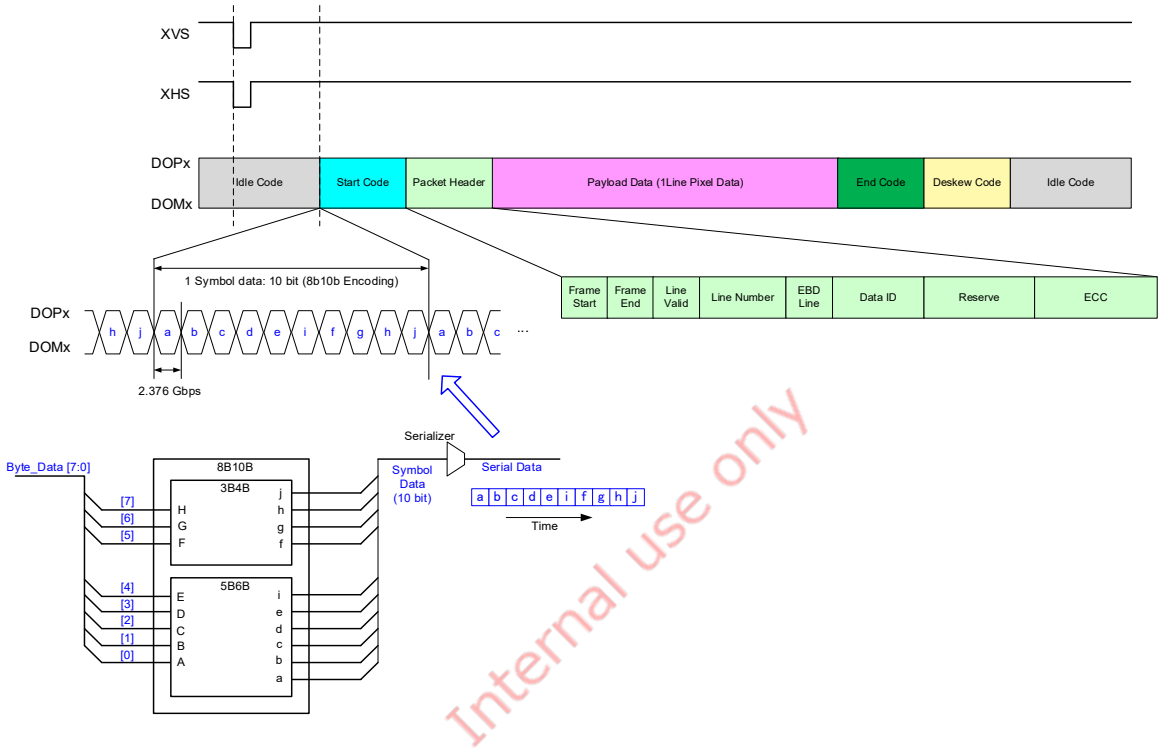
SLVS - EC Output Format

Line Format and Frame Format (Sync Signals and Data Output Timing)

The format of each line and each frame of this sensor are described below.
The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals. Timing control is performed at the falling edge of both the XVS and XHS signals.

Line Format

The figure below shows the line format of each line. 1 Symbol consists of 10 bits regardless of readout drive mode.
Refer to “SLVS - EC Specification Version 1.2” for detail.
(Note: Data rate and CLK frequency are different from SLVS - EC Specification.)



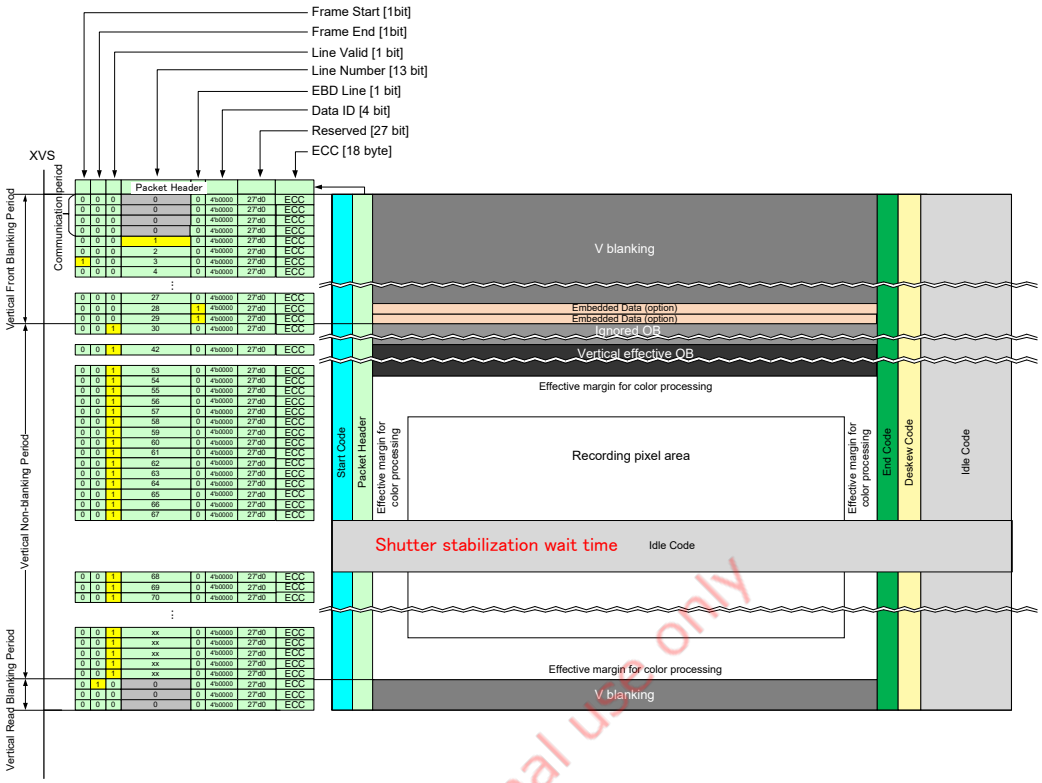
Line Format

Frame Format

Nomal frame formats in following cases are described.

Nomal frame

As an example, the figure below shows XVS timing and contents of the header in each line in the case of all - pixel scan readout mode (12 bits).



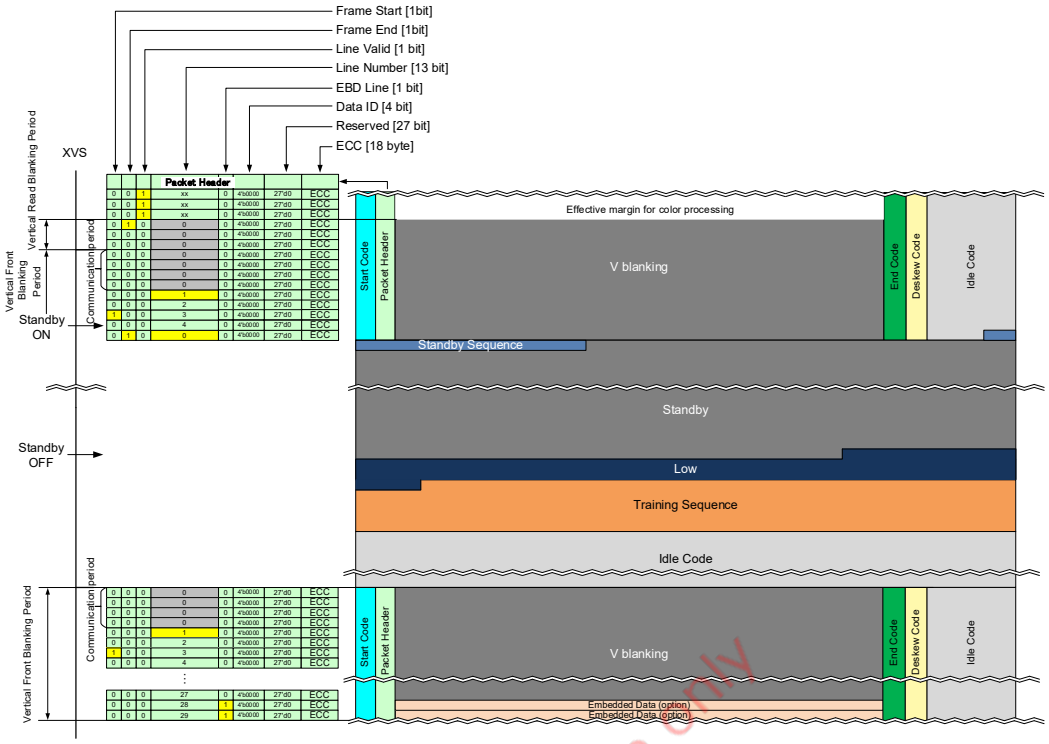
Frame Format (Normal frame, in the case of readout mode)

Contents of Header

Item	Function
Frame Start	1 is output when Line Number = 3d. (In all readout drive mode)
Frame End	1 is output on the top line of rear vertical blanking period.
Line Valid	Continuously output 1 during vertical non-blanking period.
Line Number	Line Number is reset to 1 while blanking period in the top of the frame, and incremented by 1 unit to after blanking. Its output 0 on the after blanking period
EBD Line	1 is output on embedded data output line
Data ID	Fixed to 4'b0000
Reserved	Fixed to 0
ECC	Refer to SLVS - EC Specification Version 1.2

Standby mode

This sensor generates training sequence in standby canceling, mode changing, and so on.
The timing of next line that 1 is output in Frame Start in normal frame, standby sequence, training sequence, idle codes are output. During this, Start Code, Packet Header and End Code are not output.



SLVS - EC Frame Format (Standby mode)

Register related to SLVS - EC

Payload Data ECC, CRC Setting

The registers ECC_EN can set ECC option for payload data error correction. The registers CRC_EN can set CRC option for data transfer error correction. ECC_EN and CRC_EN cannot be used together. And, change ECC_EN or CRC_EN value during initialize communication of standby cancel sequence. See “SLVS - EC Specification Version 1.2” for details of payload data, ECC and CRC. (Note: Data rate and CLK frequency are different from SLVS - EC Specification.)

Register List of ECC, CRC Setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
CRC_EN	0Bh	20h (3920h)	[0]	0h	0h: Without CRC insertion 1h: With CRC insertion ECC option and CRC option cannot be used together
ECC_EN		21h (3921h)	[1:0]	2h	0h: Without ECC insertion. 1h: With ECC [parity 2 byte] 2h: With ECC [parity 4 byte] ECC option and CRC option cannot be used together

Attribute Register and PHY Control Code

Correspondence of attribute register and PHY control code in “SLVS - EC Specification” to this sensor’s registers are shown below.

Attribute Register

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
INIT_LENGTH	0Bh	22h (3922h)	[4:0]	0Ah	Low output period during mode change and initialization. Setting range: 00h to 10h
SYNCCODE_LEN		24 to 26h (3924h to 3926h)	[23:0]	007FFFh	Sync code repeat count in training sequence. Minimum: 000001h
DESKEWCODE_LEN		28h (3928h)	[7:0]	10h	Deskew code repeat count in training sequence. Minimum: 01h
DESKEWCODE_INTVL		2Ah (392Ah)	[7:0]	10h	Idle code repeat count between deskew code in training sequence. Set the value of multiple of 4 Minimum: 04h
STBYCODE_LEN		2Ch (392Ch)	[7:0]	10h	Standby code repeat count in standby sequence. Minimum: 03h
SYNCCODE		30h to 31h (3930h to 3931h)	[8:0]	0AAh	PHY Control Code : See Sync Code
DESKEWCODE		32h to 33h (3932h to 3933h)	[8:0]	060h	PHY Control Code : see Deskew Code
IDLECODE1		34h to 35h (3934h to 3935h)	[8:0]	000h	PHY Control Code : see Idle Code
IDLECODE2		36h to 37h (3936h to 3937h)	[8:0]	000h	PHY Control Code : see Idle Code
IDLECODE3		38h to 39h (3938h to 3939h)	[8:0]	000h	PHY Control Code : see Idle Code
IDLECODE4		3Ah to 3Bh (393Ah to 393Bh)	[8:0]	000h	PHY Control Code : see Idle Code
STBYCODE		40h to 41h (3940h to 3941h)	[8:0]	003h	PHY Control Code : see Standby Code

PHY Control Code

PHY Control Code	Register name	Address [bit]	Description	8b10b symbol configuration			
Idle Code	IDLECODE1	34h[7:0]	Any symbol	IDLECODE1 (def D.00.0)	IDLECODE2 (def D.00.0)	IDLECODE3 (def D.00.0)	IDLECODE4 (def D.00.0)
		35h[0]	0:D character 1:K character				
	IDLECODE2	36h [7:0]	Any symbol				
		37h[0]	0:D character 1:K character				
	IDLECODE3	38h[7:0]	Any symbol				
		39h[0]	0:D character 1:K character				
	IDLECODE4	3Ah[7:0]	Any symbol				
		3Bh[0]	0:D character 1:K character				
Start Code	—	—	—	K.28.5	K.27.7	K.28.2	K.27.7
End Code	—	—	—	K.28.5	K.29.7	K.30.7	K.29.7
Pad Code	—	—	—	K.23.7	K.28.4	K.28.6	K.28.3
Sync Code	SYNCCODE	30h[7:0]	Any symbol	K.28.5	SYNCCODE (def D.10.5)	←	←
		31h[0]	0:D character 1:K character				
Deskew Code	DESKEWCODE	32h[7:0]	Any symbol	K.28.5	DESKEW CODE (def D.00.3)	←	←
		33h[0]	0:D character 1:K character				
Standby Code	STBYCODE	40h[7:0]	Any symbol	K.28.5	STBYCODE (def D.03.0)	←	←
		41h[0]	0:D character 1:K character				

Image Data Output Format on each Readout mode

Switching of SLVS output / SLVS - EC output is done in OMODE pin setting.

SLVS output: Low
SLVS - EC output: High

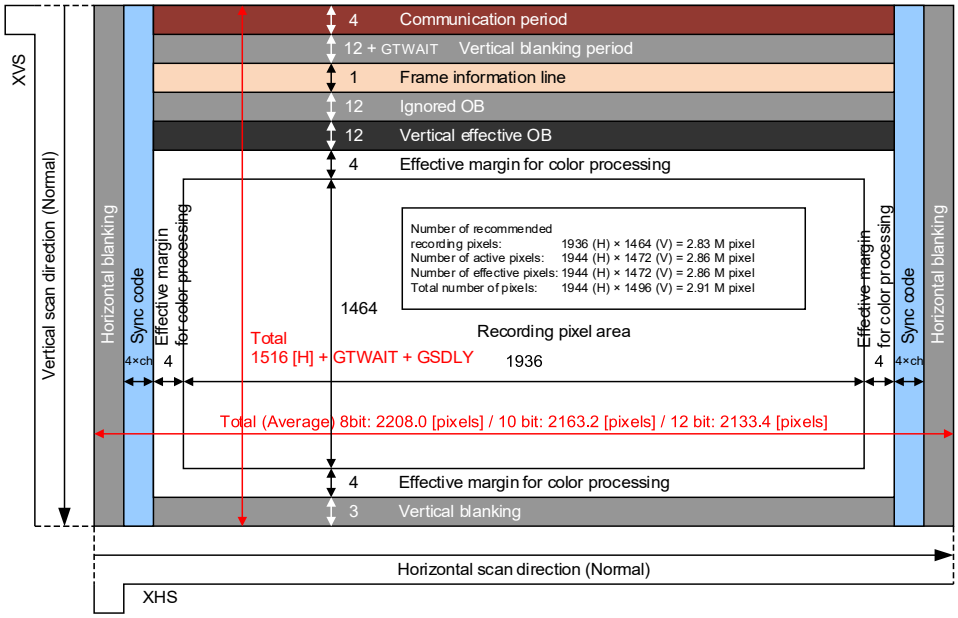
All - pixel scan

When SLVS output

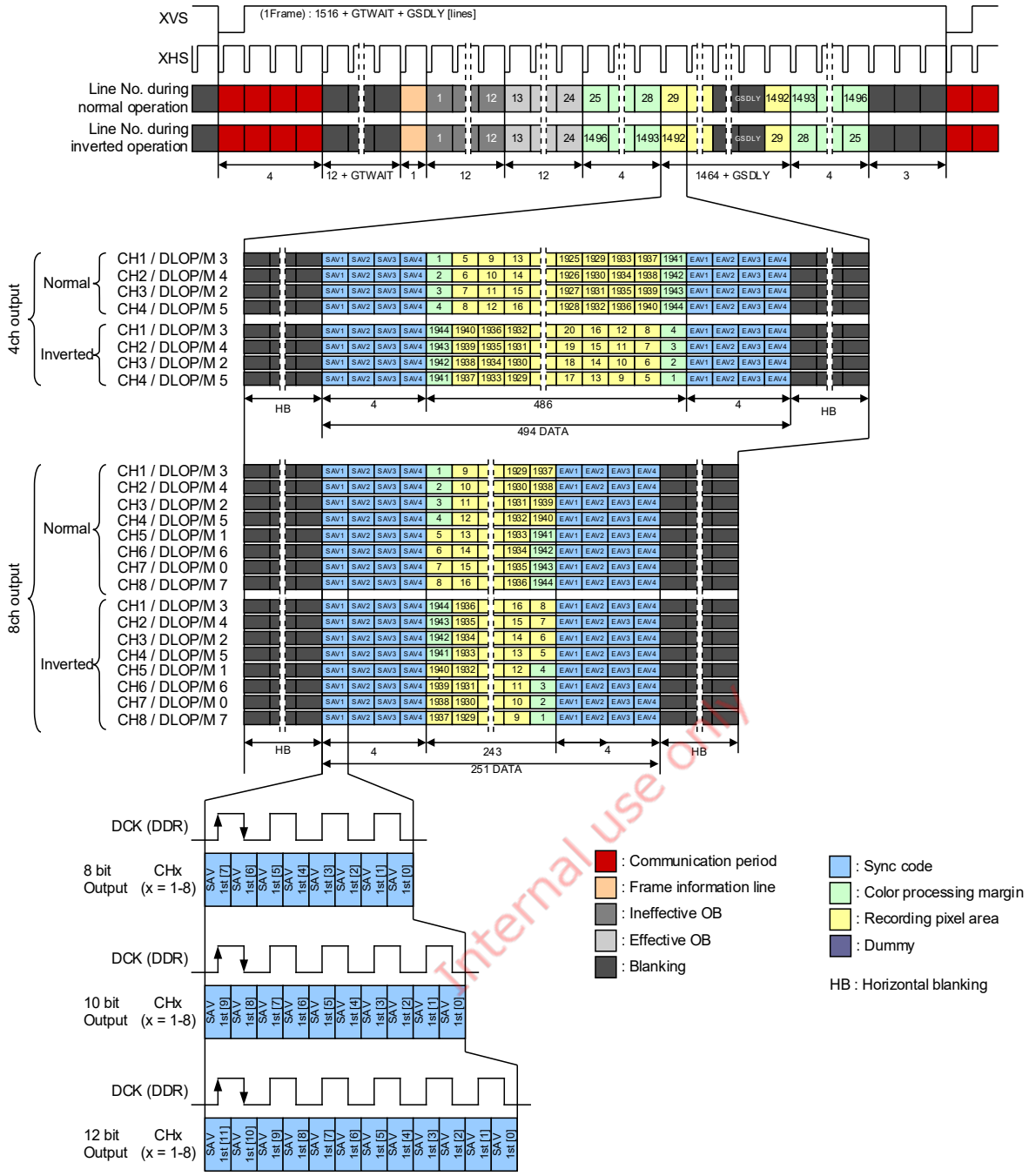
Register List of All - pixel scan mode

Please refer to the other register map file for the register that has not been described.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				174.6 [frame/s]	93.5 [frame/s]	143.0 [frame/s]	75.4 [frame/s]	121.1 [frame/s]	63.4 [frame/s]	FREQ = 0h
				90.0 [frame/s]	47.4 [frame/s]	73.2 [frame/s]	38.2 [frame/s]	61.6 [frame/s]	32.0 [frame/s]	FREQ = 1h
Chip ID = 02h										
3Ch	[3:0]	WINMODE	0h	0h						All-pixel mode
	[4]	HMODE	0	0						All-pixel
D4h	[7:0]	VMAX	618h	604h	5FCh	600h	5FCh	5FCh	5F8h	FREQ = 0h
D5h	[7:0]			5FCh	5F8h	5FCh	5F8h	5F8h	5F8h	FREQ = 1h
D6h	[7:0]									
D8h	[7:0]	HMAX	080h	114h	206h	152h	282h	190h	2FEh	FREQ = 0h
D9h	[7:0]			21Ah	400h	296h	4F6h	314h	5EEh	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	18h	0Ch	08h	0Ch	08h	08h	04h	FREQ = 0h
				08h	04h	08h	04h	04h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	0Ch	08h	08h	08h	08h	08h	FREQ = 0h
				08h	08h	08h	08h	08h	08h	FREQ = 1h
Chip ID = 04h										
00h	[1:0]		0h	0h						
	[3]	HADD_ON	0	0						All-pixel
	[4]	HADD_ON_SEL	0	0						All-pixel
	[6:5]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]		0Eh	10h						
31h	[1:0]									
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	2h	N/A	2h	N/A	2h	4 ch SLVS
45h	[3:0]	OPORTSEL	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	4 ch SLVS
Chip ID = 07h										
C0h	[7:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
C1h	[3:0]									



Pixel Array Image Drawing in All - pixel scan Mode
(SLVS output Shutter stabilization wait time is not included)



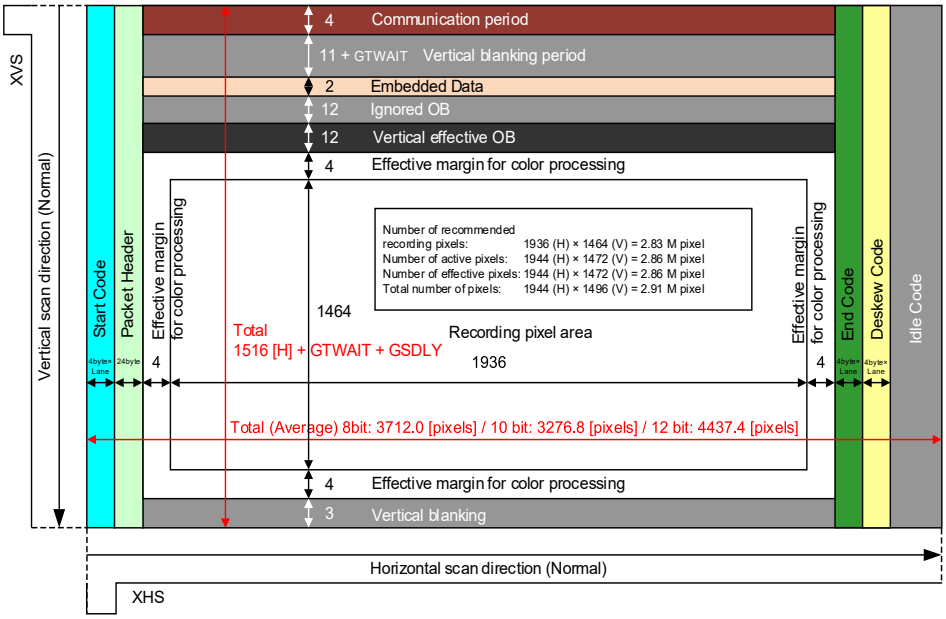
Drive Timing Chart for Serial Output in All - pixel Scan Mode (SLVS output)

When SLVS - EC output

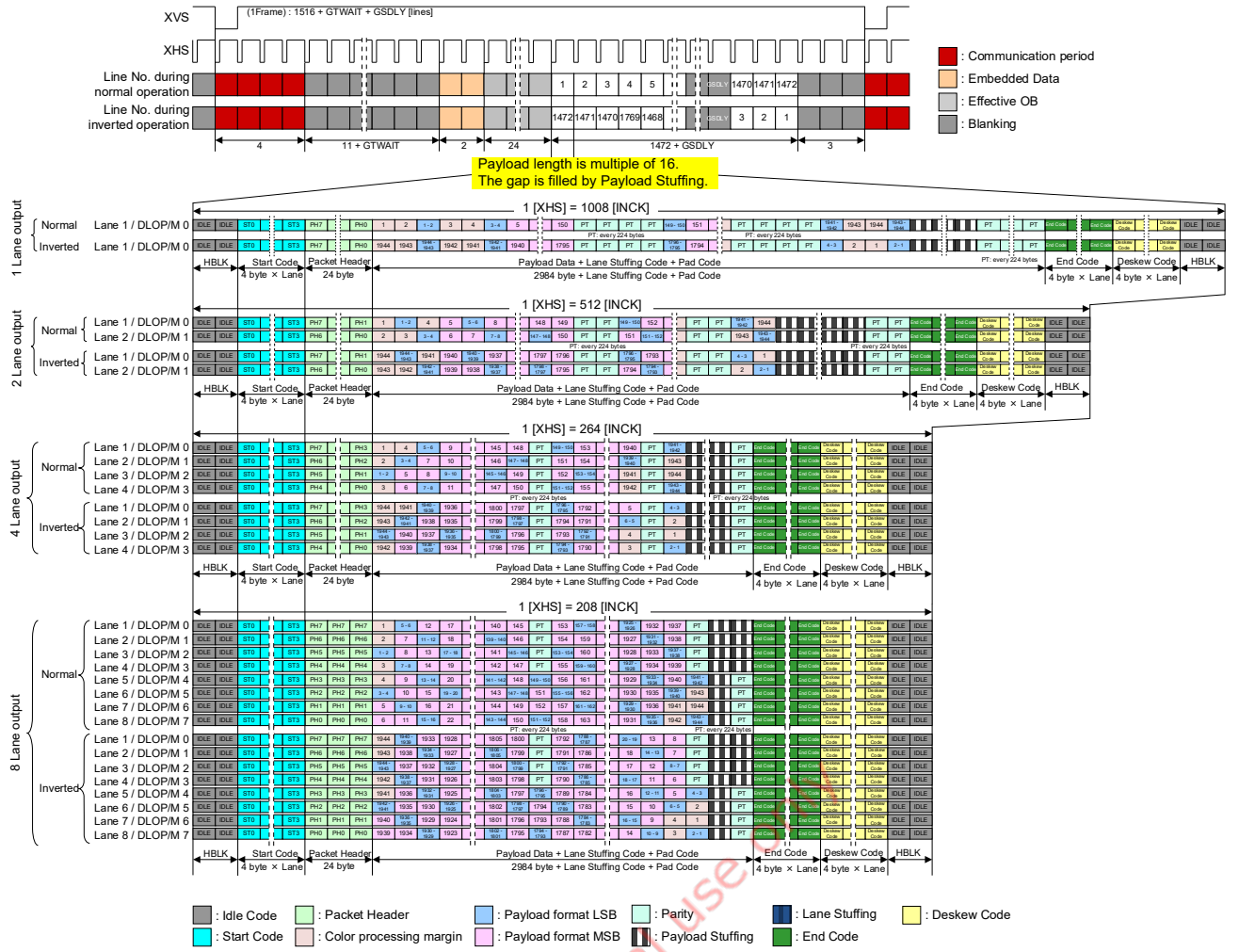
Register List of All - pixel scan mode

Please refer to the other register map file for the register that has not been described.

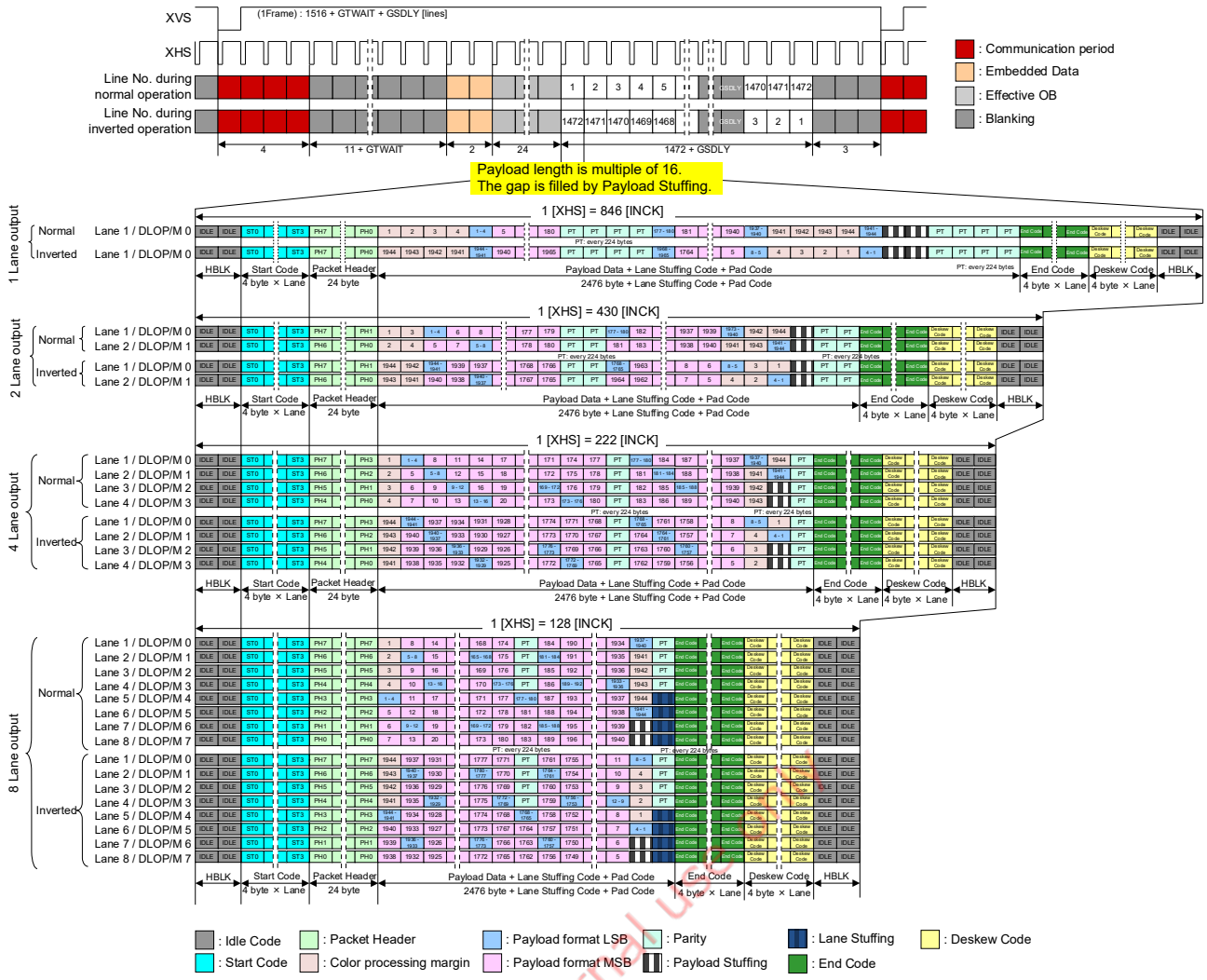
Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				409.2 [frame/s]	263.5 [frame/s]	138.4 [frame/s]	70.8 [frame/s]	371.8 [frame/s]	216.6 [frame/s]	112.7 [frame/s]	57.4 [frame/s]	231.2 [frame/s]	182.6 [frame/s]	94.6 [frame/s]	48.2 [frame/s]	FREQ = 0h
				242.8 [frame/s]	133.8 [frame/s]	69.6 [frame/s]	35.6 [frame/s]	202.5 [frame/s]	109.6 [frame/s]	56.6 [frame/s]	28.8 [frame/s]	173.4 [frame/s]	92.4 [frame/s]	47.6 [frame/s]	24.2 [frame/s]	FREQ = 1h
Chip ID = 02h																
3Ch	[3:0]	WINMODE	0h	0h												All-pixel mode
	[4]	HMODE	0	0												All-pixel
D4h	[7:0]	VMAX	618h	61Ch	60Ch	5FCh	5FCh	618h	608h	5FCh	5F8h	608h	604h	5FCh	5F8h	FREQ = 0h
D5h	[7:0]			608h	5FCh	5FCh	5F8h	604h	5FCh	5F8h	5F4h	604h	5FCh	5F8h	5F4h	FREQ = 1h
D6h	[7:0]															
D8h	[7:0]	HMAX	080h	074h	0B6h	15Eh	2ACh	080h	0DEh	1AEh	34Eh	0D0h	108h	200h	3F0h	FREQ = 0h
D9h	[7:0]			0C6h	16Ah	2B8h	554h	0EEh	1BAh	35Ah	698h	116h	20Ch	3FCh	7DCh	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h												
E2h	[7:0]	GTWAIT	18h	1Ch	10h	08h	08h	18h	10h	08h	04h	10h	0Ch	08h	04h	FREQ = 0h
				10h	08h	08h	04h	0Ch	08h	04h	04h	0Ch	08h	04h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	14h	10h	08h	08h	14h	0Ch	08h	08h	0Ch	0Ch	08h	08h	FREQ = 0h
				0Ch	08h	08h	08h	0Ch	08h	08h	04h	0Ch	08h	08h	04h	FREQ = 1h
Chip ID = 04h																
00h	[1:0]		0h	0h												
	[3]	HADD_ON	0	0												All-pixel
	[4]	HADD_ON_SEL	0	0												All-pixel
	[6:5]	ADBIT	0h	2h				0h				1h				0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 83h FREQ = 1: 93h												
30h	[7:2]		0Eh	10h												
31h	[1:0]															
Chip ID = 06h																
30h	[1:0]	ODBIT	0h	2h				0h				1h				0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h																
C0h	[7:0]	BLKLEVEL	03Ch	00Fh				03Ch				0F0h				Recommended value
C1h	[3:0]															
Chip ID = 0Bh																
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	8 Lane
				N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	4 Lane
				N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	2 Lane
				N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	1 Lane



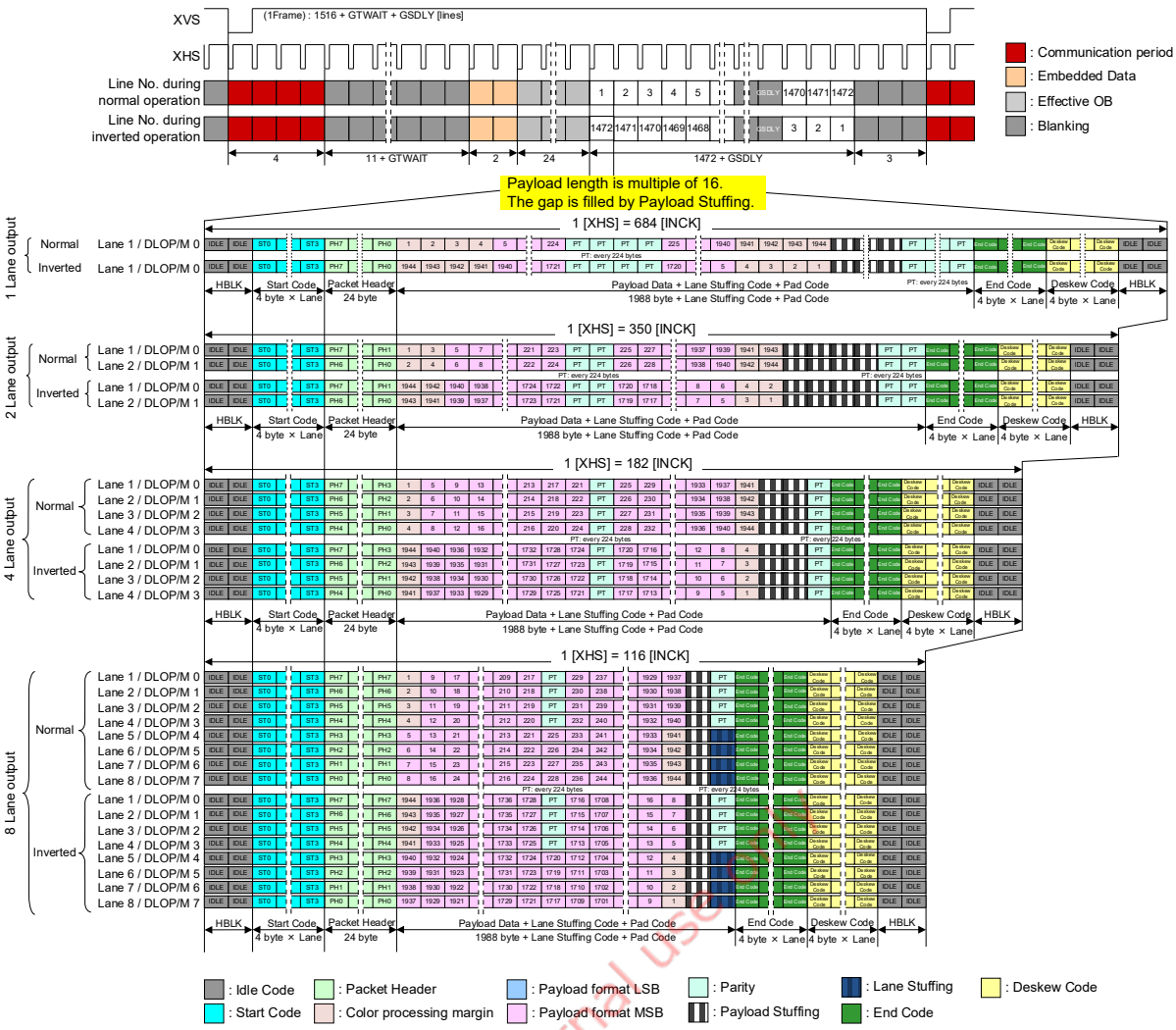
Pixel Array Image Drawing in All - pixel scan Mode
(SLVS - EC output Shutter stabilization wait time is not included)



Drive Timing Chart for SLVS - EC Output in All - pixel Scan Mode (SLVS - EC output, AD 12bit)



Drive Timing Chart for SLVS - EC Output in All - pixel Scan Mode (SLVS - EC output, AD 10bit)



Drive Timing Chart for SLVS - EC Output in All - pixel Scan Mode (SLVS - EC output, AD 8bit)

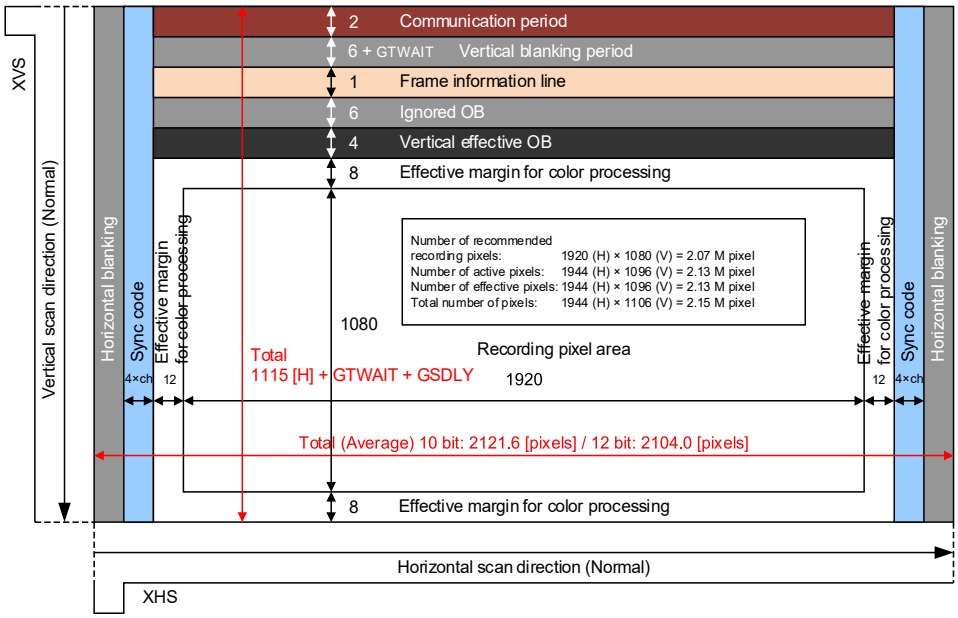
1080p - Full HD mode

Only SLVS output

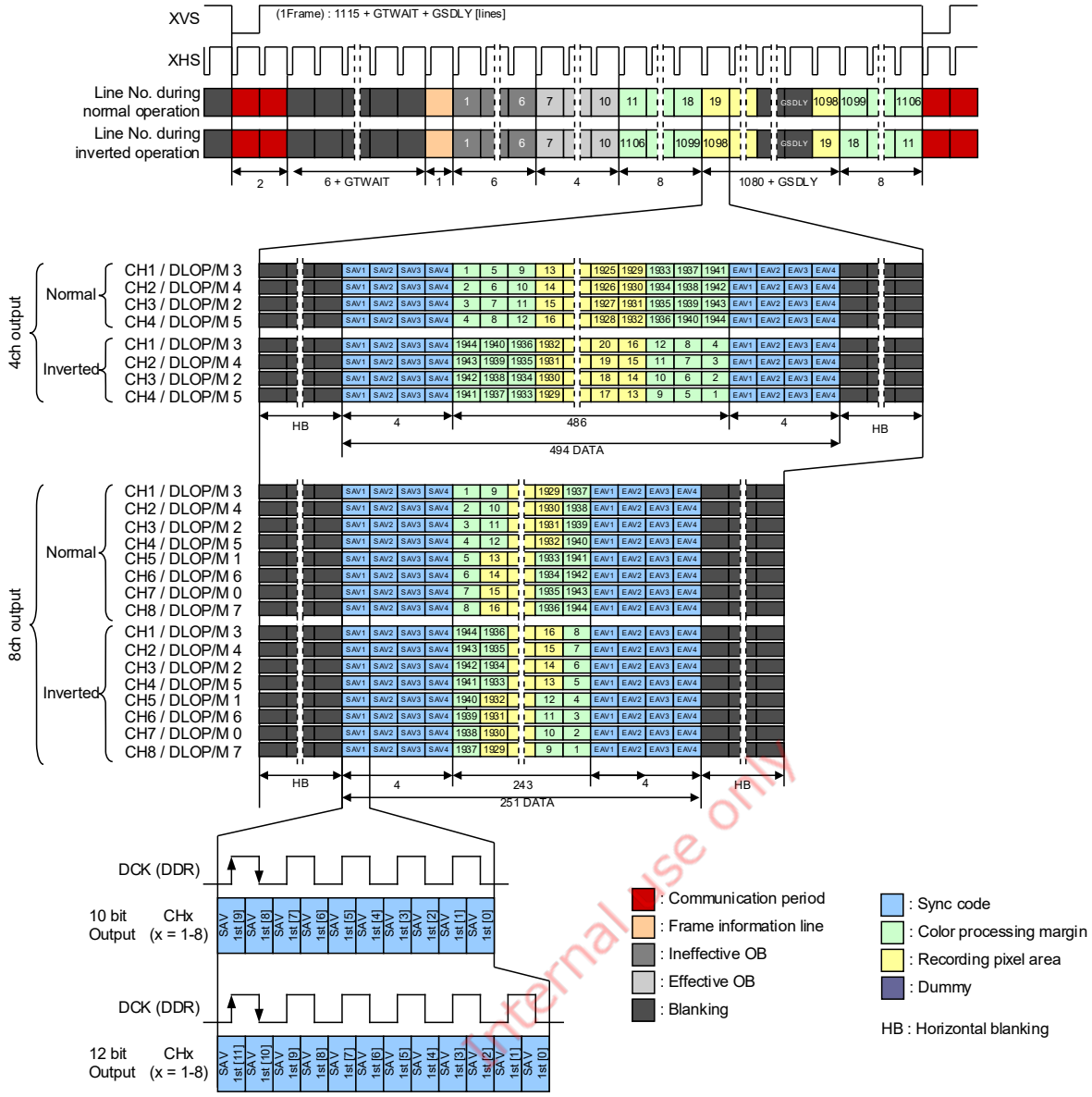
Register List of 1080p - Full HD mode

Please refer to the other register map file for the register that has not been described.

Address	bit	Register name	Initial Value	Setting value				Remarks
				AD = 10 bit		AD = 12 bit		
				120.0 [frame/s]	60.0 [frame/s]	120.0 [frame/s]	60.0 [frame/s]	FREQ = 0h
Chip ID = 02h								
3Ch	[3:0]	WINMODE	0h	Ch				1080p Full HD mode
	[4]	HMODE	0	0				
D4h	[7:0]	VMAX	618h	465h				FREQ = 0h
D5h	[7:0]							
D6h	[7:0]							
D8h	[7:0]	HMAX	080h	226h	44Ch	226h	44Ch	FREQ = 0h
D9h	[7:0]							
DCh	[1:0]	FREQ	0h	0h				
E2h	[7:0]	GTWAIT	18h	06h				FREQ = 0h
E3h	[7:0]	GSDLY	14h	04h				FREQ = 0h
Chip ID = 04h								
00h	[1:0]		0h	1h				
	[3]	HADD_ON	0	0				
	[4]	HADD_ON_SEL	0	0				
	[6:5]	ADBIT	0h	0h		1h		0: 10 bit 1: 12 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz: 50h INCK = 74.25 MHz: 52h				
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h				
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz: 50h INCK = 74.25 MHz: 52h				
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 18h				
26h	[7:0]	FREQ_SYNC	83h	54h				
30h	[7:2]		0Eh	08h				
31h	[1:0]							
Chip ID = 06h								
30h	[1:0]	ODBIT	0h	0h		1h		0: 10 bit 1: 12 bit
44h	[3:0]	STBSLVS	1h	1h	N/A	1h	N/A	8 ch SLVS
				N/A	2h	N/A	2h	4 ch SLVS
45h	[3:0]	OPORTSEL	1h	1h	N/A	1h	N/A	8 ch SLVS
				N/A	3h	N/A	3h	4 ch SLVS
Chip ID = 07h								
C0h	[7:0]	BLKLEVEL	03Ch	03Ch		0F0h		Recommended value
C1h	[3:0]							



Pixel Array Image Drawing in 1080p - Full HD scan Mode
(SLVS output Shutter stabilization wait time is not included)



Drive Timing Chart for Serial Output in 1080p - Full HD Scan Mode (SLVS output)

ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 64 areas that specified by horizontal 8 points and vertical 8 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All - pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
This sensor supports ROI + 2 × 2 Vertical FD binning mode.
This section is written in case of All - pixel scan mode for example on this document.

When SLVS output

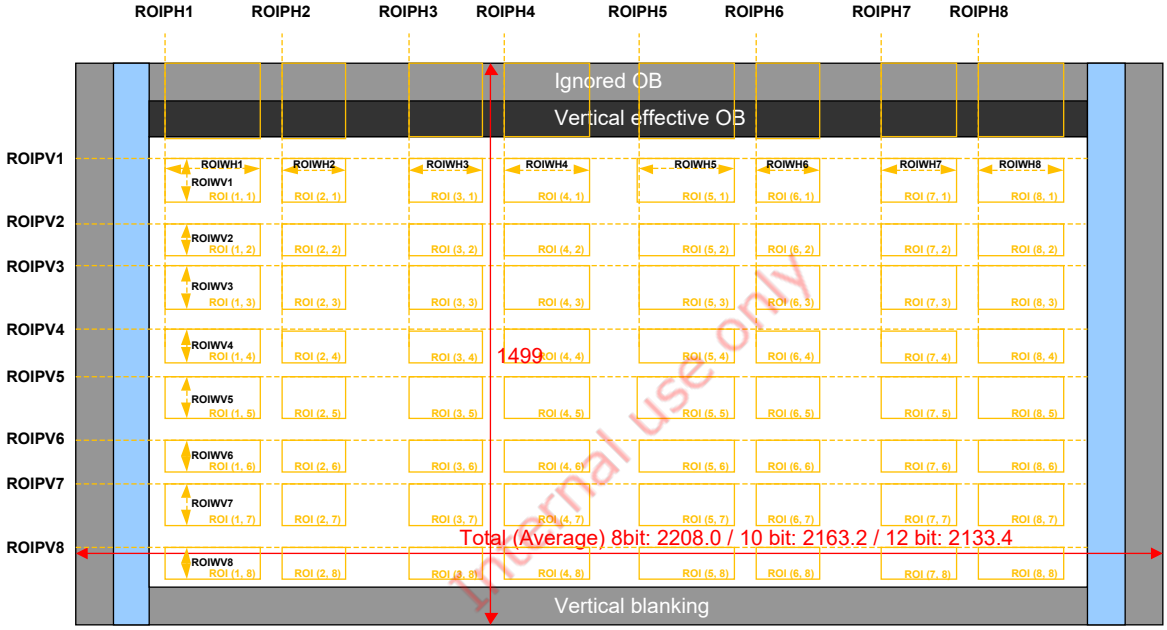
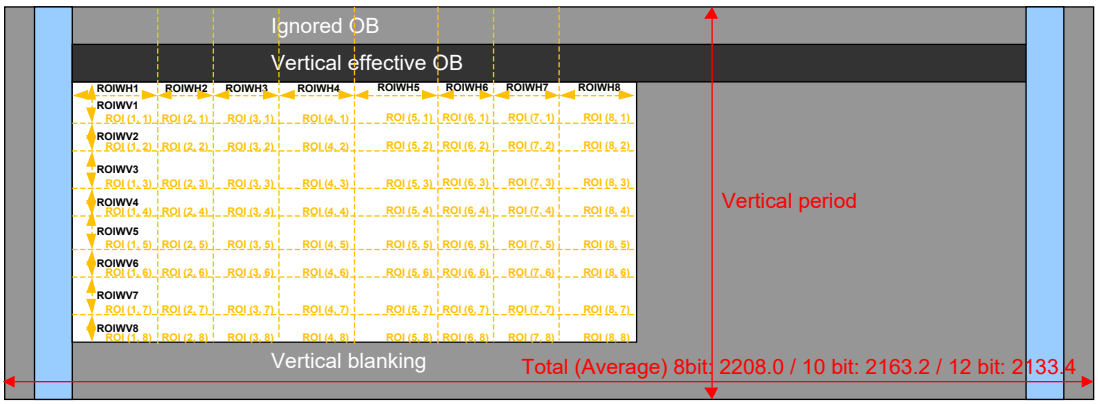


Image Drawing of Designated Areas in ROI Mode (SLVS output)



Details of Image Drawing (SLVS output)

Register List of ROI mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
3Ch	[3:0]	WINMODE	0h	0h						All-pixel mode
	[4]	HMODE	0	0						All-pixel
D4h	[7:0]	VMAX	618h	*1	*2	*3	*4	*5	*6	
D5h	[7:0]									
D6h	[7:0]									
D8h	[7:0]	HMAX	080h	114h	206h	152h	282h	190h	2FEh	FREQ = 0h
D9h	[7:0]			21Ah	400h	296h	4F6h	314h	5EEh	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	18h	0Ch	08h	0Ch	08h	08h	04h	FREQ = 0h
				08h	04h	08h	04h	04h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	0Ch	08h	08h	08h	08h	08h	FREQ = 0h
				08h	08h	08h	08h	08h	08h	FREQ = 1h
Chip ID = 03h										
04h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH2ON	0	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV2ON	0	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH3ON	0	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV3ON	0	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH4ON	0	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV4ON	0	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable						
05h	[0]	FID0_ROIH5ON	0	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable						
	[1]	FID0_ROIV5ON	0	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable						
	[2]	FID0_ROIH6ON	0	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable						
	[3]	FID0_ROIV6ON	0	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable						
	[4]	FID0_ROIH7ON	0	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable						
	[5]	FID0_ROIV7ON	0	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable						
	[6]	FID0_ROIH8ON	0	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable						
	[7]	FID0_ROIV8ON	0	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable						
20h	[7:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8						
21h	[4:0]									
22h	[7:0]	FID0_ROIPV1	000h	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
23h	[3:0]									
24h	[7:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 4						
25h	[4:0]									
26h	[7:0]	FID0_ROIWV1	000h	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8						
27h	[3:0]									
28h	[7:0]	FID0_ROIPH2	0000h	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8						
29h	[4:0]									
2Ah	[7:0]	FID0_ROIPV2	000h	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
2Bh	[3:0]									
2Ch	[7:0]	FID0_ROIWH2	0000h	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4						
2Dh	[4:0]									

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
2Eh 2Fh	[7:0] [3:0]	FID0_ROIWV2	000h	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8						
30h 31h	[7:0] [4:0]	FID0_ROIPH3	0000h	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8						
32h 33h	[7:0] [3:0]	FID0_ROIPV3	000h	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
34h 35h	[7:0] [4:0]	FID0_ROIWH3	0000h	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4						
36h 37h	[7:0] [3:0]	FID0_ROIWV3	000h	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8						
38h 39h	[7:0] [4:0]	FID0_ROIPH4	0000h	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8						
3Ah 3Bh	[7:0] [3:0]	FID0_ROIPV4	000h	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
3Ch 3Dh	[7:0] [4:0]	FID0_ROIWH4	0000h	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4						
3Eh 3Fh	[7:0] [3:0]	FID0_ROIWV4	000h	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8						
40h 41h	[7:0] [4:0]	FID0_ROIPH5	0000h	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8						
42h 43h	[7:0] [3:0]	FID0_ROIPV5	000h	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
44h 45h	[7:0] [4:0]	FID0_ROIWH5	0000h	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4						
46h 47h	[7:0] [3:0]	FID0_ROIWV5	000h	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8						
48h 49h	[7:0] [4:0]	FID0_ROIPH6	0000h	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8						
4Ah 4Bh	[7:0] [3:0]	FID0_ROIPV6	000h	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
4Ch 4Dh	[7:0] [4:0]	FID0_ROIWH6	0000h	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4						
4Eh 4Fh	[7:0] [3:0]	FID0_ROIWV6	000h	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8						
50h 51h	[7:0] [4:0]	FID0_ROIPH7	0000h	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8						
52h 53h	[7:0] [3:0]	FID0_ROIPV7	000h	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
54h 55h	[7:0] [4:0]	FID0_ROIWH7	0000h	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4						
56h 57h	[7:0] [3:0]	FID0_ROIWV7	000h	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8						
58h 59h	[7:0] [4:0]	FID0_ROIPH8	0000h	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8						
5Ah 5Bh	[7:0] [3:0]	FID0_ROIPV8	000h	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						
5Ch 5Dh	[7:0] [4:0]	FID0_ROIWH8	0000h	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4						
5Eh 5Fh	[7:0] [3:0]	FID0_ROIWV8	000h	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8						

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 04h										
00h	[1:0]		0h	0h						
	[3]	HADD_ON	0	0						All-pixel
	[4]	HADD_ON_SEL	0	0						All-pixel
	[6:5]	ADBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]		0Eh	10h						
31h	[1:0]									
Chip ID = 06h										
30h	[1:0]	ODBIT	0h	2h		0h		1h		0: 10 bit 1: 12 bit 2: 8 bit
44h	[3:0]	STBSLVS	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	2h	N/A	2h	N/A	2h	4 ch SLVS
45h	[3:0]	OPORTSEL	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	4 ch SLVS
Chip ID = 07h										
C0h	[7:0]	BLKLEVEL	03Ch	00Fh		03Ch		0F0h		Recommended value
C1h	[3:0]									

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
  ROIPH1 + ROIWH1 < ROIPH2
  ROIPH2 + ROIWH2 < ROIPH3
  ROIPH3 + ROIWH3 < ROIPH4
…
  ROIPH8 + ROIWH8 ≤ 1944d

  ROIPV1 + ROIWV1 < ROIPV2
  ROIPV2 + ROIWV2 < ROIPV3
  ROIPV3 + ROIWV3 < ROIPV4
…
  ROIPV8 + ROIWV8 ≤ 1472d

* Set the horizontal width in multiple of 4 and horizontal position, vertical width / position setting in multiple of 8.

* Minimum width of the window is as below.
  ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≥ 8d

  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≥ 8d

Frame rate on ROI mode

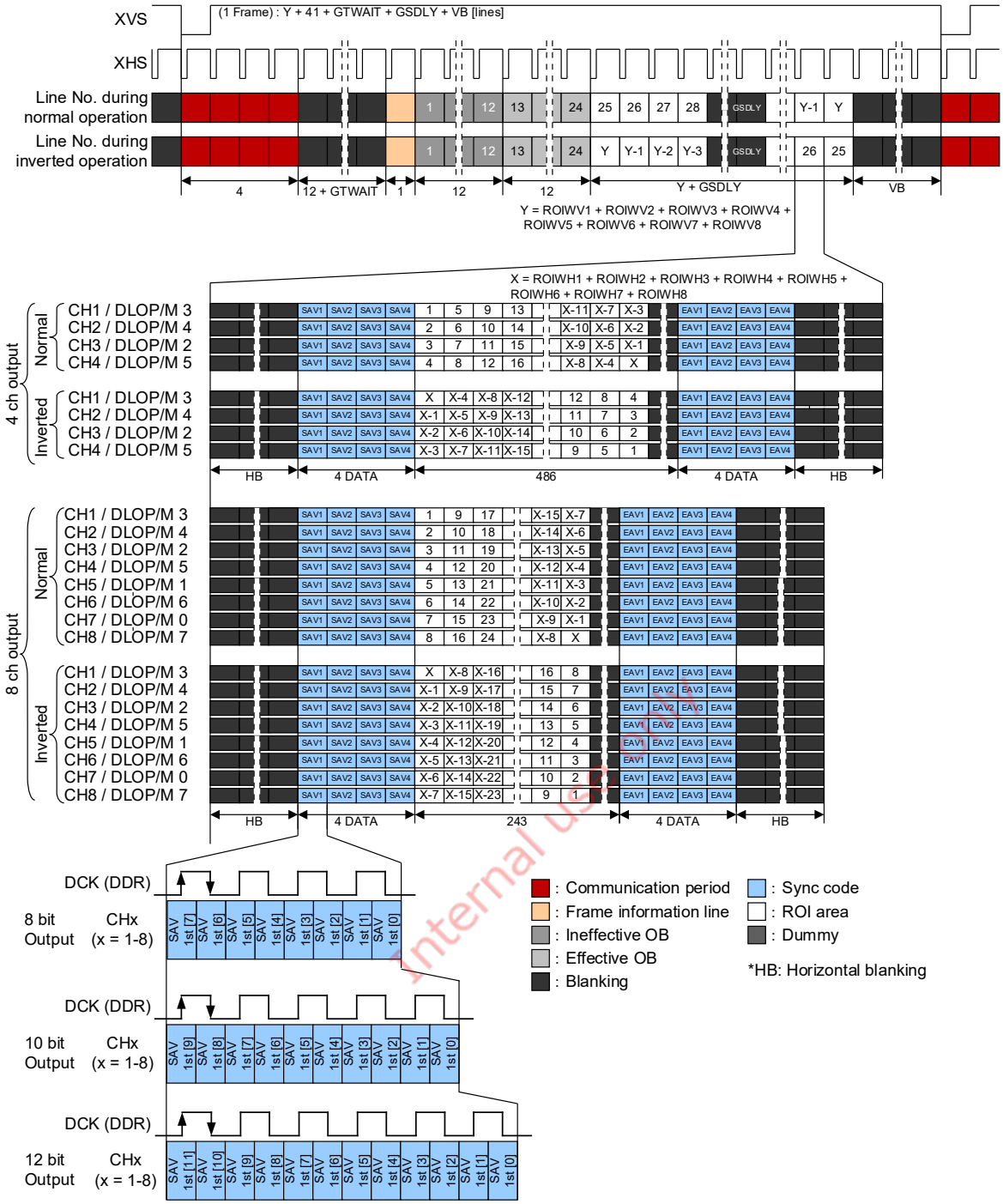
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

* Number of lines per frame or VMAX
  V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + GTWAIT + GSDLY + 44
  Refer to GTWAIT and GSDLY table in “Global Shutter (Normal Mode) Operation” item.
* 1H period: Change according to the data rate settings and the number of SLVS channels.
  Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 600
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 8 (minimum value)

Frame rate List of each setting

Register settings No. in register list	1 H period [µs]		Frame rate [frame/s]			
	FREQ 0h	FREQ 1h	Total number of ROI: 600 [line]		Total number of ROI: 8 [line]	
			FREQ = 0h	FREQ = 1h	FREQ = 0h	FREQ = 1h
*1	3.71	7.24	402.72	209.10	3539.75	2029.57
*2	6.97	13.79	217.18	110.53	2107.93	1132.96
*3	4.55	8.91	330.83	169.93	3051.03	1649.41
*4	8.64	17.10	175.23	89.12	1700.79	913.50
*5	5.38	10.61	281.25	143.63	2729.77	1472.27
*6	10.31	20.44	147.76	74.56	1514.56	764.26



Drive Timing Chart for Serial Output in ROI Mode (SLVS output)

When SLVS - EC output

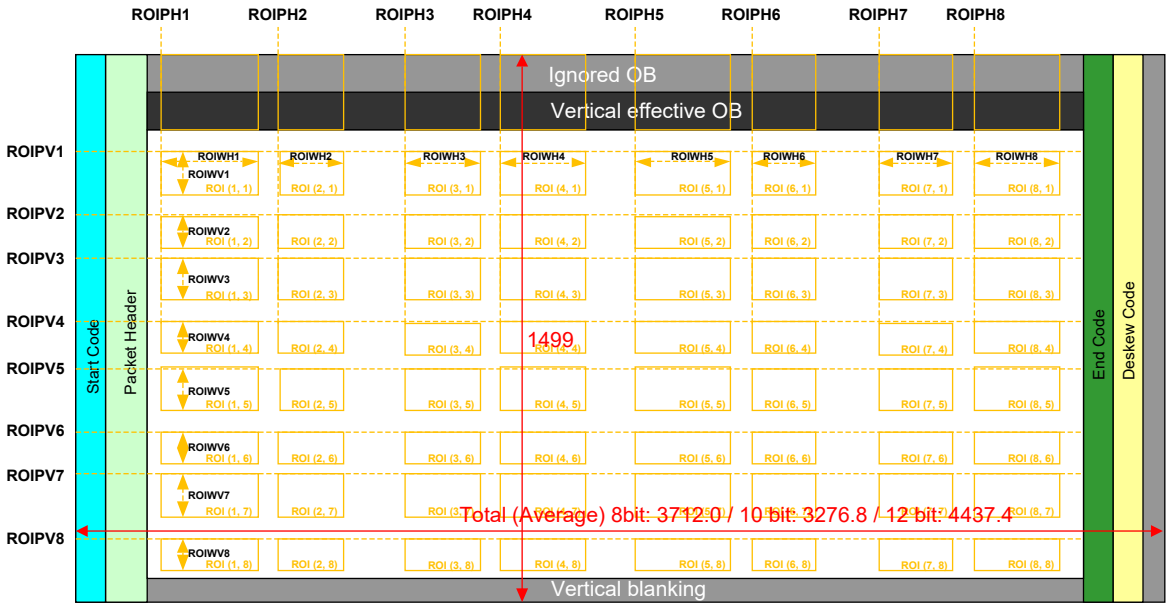
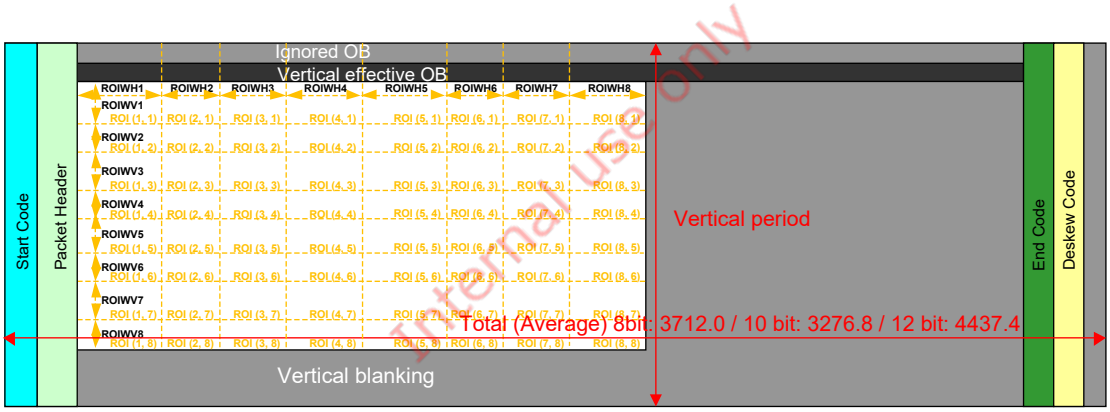


Image Drawing of Designated Areas in ROI Mode
(SLVS - EC output Shutter stabilization wait time is not included)



Details of Image Drawing
(SLVS - EC output Shutter stabilization wait time is not included)

Register List of ROI mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	*10 [frame/s]	*11 [frame/s]	*12 [frame/s]	
Chip ID = 02h																
3Ch	[3:0]	WINMODE	0h	0h												All-pixel mode
	[4]	HMODE	0	0												All-pixel
D4h	[7:0]	VMAX	618h	*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11	*12	
D5h	[7:0]															
D6h	[7:0]															
D8h	[7:0]	HMAX	080h	074h	0B6h	15Eh	2ACh	080h	0DEh	1AEh	34Eh	0D0h	108h	200h	3F0h	FREQ = 0h
D9h	[7:0]			0C6h	16Ah	2B8h	554h	0EEh	1BAh	35Ah	698h	116h	20Ch	3FCh	7DCh	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h												
E2h	[7:0]	GTWAIT	18h	1Ch	10h	08h	08h	18h	10h	08h	04h	10h	0Ch	08h	04h	FREQ = 0h
				10h	08h	08h	04h	0Ch	08h	04h	04h	0Ch	08h	04h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	14h	10h	08h	08h	14h	0Ch	08h	08h	0Ch	0Ch	08h	08h	FREQ = 0h
				0Ch	08h	08h	08h	0Ch	08h	08h	04h	0Ch	08h	08h	04h	FREQ = 1h
Chip ID = 03h																
04h	[0]	FID0_ROIH1ON	0	The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8) 0: Disable 1: Enable												
	[1]	FID0_ROIV1ON	0	The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8) 0: Disable 1: Enable												
	[2]	FID0_ROIH2ON	0	The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8) 0: Disable 1: Enable												
	[3]	FID0_ROIV2ON	0	The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8) 0: Disable 1: Enable												
	[4]	FID0_ROIH3ON	0	The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8) 0: Disable 1: Enable												
	[5]	FID0_ROIV3ON	0	The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8) 0: Disable 1: Enable												
	[6]	FID0_ROIH4ON	0	The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8) 0: Disable 1: Enable												
	[7]	FID0_ROIV4ON	0	The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8) 0: Disable 1: Enable												
05h	[0]	FID0_ROIH5ON	0	The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8) 0: Disable 1: Enable												
	[1]	FID0_ROIV5ON	0	The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8) 0: Disable 1: Enable												
	[2]	FID0_ROIH6ON	0	The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8) 0: Disable 1: Enable												
	[3]	FID0_ROIV6ON	0	The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8) 0: Disable 1: Enable												
	[4]	FID0_ROIH7ON	0	The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8) 0: Disable 1: Enable												
	[5]	FID0_ROIV7ON	0	The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8) 0: Disable 1: Enable												
	[6]	FID0_ROIH8ON	0	The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8) 0: Disable 1: Enable												
	[7]	FID0_ROIV8ON	0	The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8) 0: Disable 1: Enable												
20h	[7:0]	FID0_ROIPH1	0000h	Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 8												
21h	[4:0]															
22h	[7:0]	FID0_ROIPV1	000h	Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8												
23h	[3:0]															
24h	[7:0]	FID0_ROIWH1	0000h	Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8) *Set the value of multiple of 4												
25h	[4:0]															
26h	[7:0]	FID0_ROIWV1	000h	Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 8												
27h	[3:0]															
28h	[7:0]	FID0_ROIPH2	0000h	Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 8												
29h	[4:0]															
2Ah	[7:0]	FID0_ROIPV2	000h	Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8												
2Bh	[3:0]															
2Ch	[7:0]	FID0_ROIWH2	0000h	Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4												
2Dh	[4:0]															

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	*10 [frame/s]	*11 [frame/s]	*12 [frame/s]	
2Eh 2Fh	[7:0] [3:0]	FID0_ROIWV2	000h	Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 8												
30h 31h	[7:0] [4:0]	FID0_ROIPH3	0000h	Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 8												
32h 33h	[7:0] [3:0]	FID0_ROIPV3	000h	Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8												
34h 35h	[7:0] [4:0]	FID0_ROIWH3	0000h	Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4												
36h 37h	[7:0] [3:0]	FID0_ROIWV3	000h	Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 8												
38h 39h	[7:0] [4:0]	FID0_ROIPH4	0000h	Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 8												
3Ah 3Bh	[7:0] [3:0]	FID0_ROIPV4	000h	Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8												
3Ch 3Dh	[7:0] [4:0]	FID0_ROIWH4	0000h	Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4												
3Eh 3Fh	[7:0] [3:0]	FID0_ROIWV4	000h	Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 8												
40h 41h	[7:0] [4:0]	FID0_ROIPH5	0000h	Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 8												
42h 43h	[7:0] [3:0]	FID0_ROIPV5	000h	Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8												
44h 45h	[7:0] [4:0]	FID0_ROIWH5	0000h	Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4												
46h 47h	[7:0] [3:0]	FID0_ROIWV5	000h	Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 8												
48h 49h	[7:0] [4:0]	FID0_ROIPH6	0000h	Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 8												
4Ah 4Bh	[7:0] [3:0]	FID0_ROIPV6	000h	Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8												
4Ch 4Dh	[7:0] [4:0]	FID0_ROIWH6	0000h	Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4												
4Eh 4Fh	[7:0] [3:0]	FID0_ROIWV6	000h	Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 8												
50h 51h	[7:0] [4:0]	FID0_ROIPH7	0000h	Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 8												
52h 53h	[7:0] [3:0]	FID0_ROIPV7	000h	Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8												
54h 55h	[7:0] [4:0]	FID0_ROIWH7	0000h	Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4												
56h 57h	[7:0] [3:0]	FID0_ROIWV7	000h	Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 8												
58h 59h	[7:0] [4:0]	FID0_ROIPH8	0000h	Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 8												
5Ah 5Bh	[7:0] [3:0]	FID0_ROIPV8	000h	Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8												
5Ch 5Dh	[7:0] [4:0]	FID0_ROIWH8	0000h	Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4												
5Eh 5Fh	[7:0] [3:0]	FID0_ROIWV8	000h	Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 8												

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	*10 [frame/s]	*11 [frame/s]	*12 [frame/s]	
Chip ID = 04h																
00h	[1:0]		0h	0h												
	[3]	HADD_ON	0	0												All-pixel
	[4]	HADD_ON_SEL	0	0												All-pixel
	[6:5]	ADBIT	0h	2h				0h				1h				0: 10 bit 1: 12 bit 2: 8 bit
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 83h FREQ = 1: 93h												
30h	[7:2]		0Eh	10h												
31h	[1:0]															
Chip ID = 06h																
30h	[1:0]	ODBIT	0h	2h				0h				1h				0: 10 bit 1: 12 bit 2: 8 bit
Chip ID = 07h																
C0h	[7:0]	BLKLEVEL	03Ch	00Fh				03Ch				0F0h				Recommended value
C1h	[3:0]															
Chip ID = 0Bh																
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	8 Lane
				N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	4 Lane
				N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	2 Lane
				N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	1 Lane

Restrictions on ROI mode

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
  ROIPH1 + ROIWH1 < ROIPH2
  ROIPH2 + ROIWH2 < ROIPH3
  ROIPH3 + ROIWH3 < ROIPH4
…
  ROIPH8 + ROIWH8 ≤ 1944d

  ROIPV1 + ROIWV1 < ROIPV2
  ROIPV2 + ROIWV2 < ROIPV3
  ROIPV3 + ROIWV3 < ROIPV4
…
  ROIPV8 + ROIWV8 ≤ 1472d

* Set the horizontal width in multiple of 4 and horizontal position, vertical width / position setting in multiple of 8.

* Minimum width of the window is as below.

  ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≥ 8d

  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≥ 8d

Frame rate on ROI mode

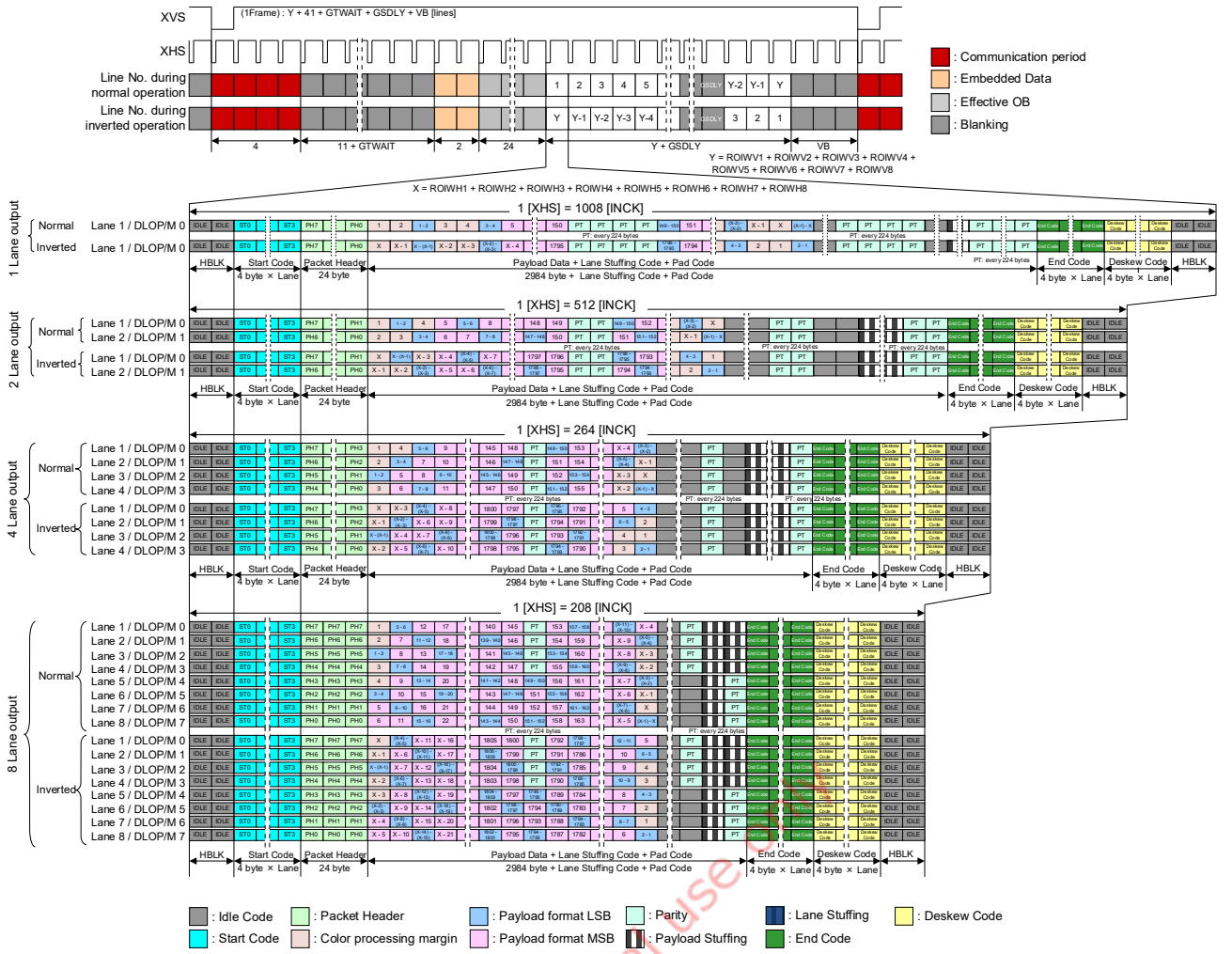
Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))

* Number of lines per frame or VMAX
  V_{TR} = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + GTWAIT + GSDLY + 44
  Refer to GTWAIT and GSDLY table in “Global Shutter (Normal Trigger Mode) Operation” item.
* 1H period: Change according to the data rate settings and the number of SLVS - EC Lanes.
  Calculate by number of INCK in 1 H and the period of INCK.

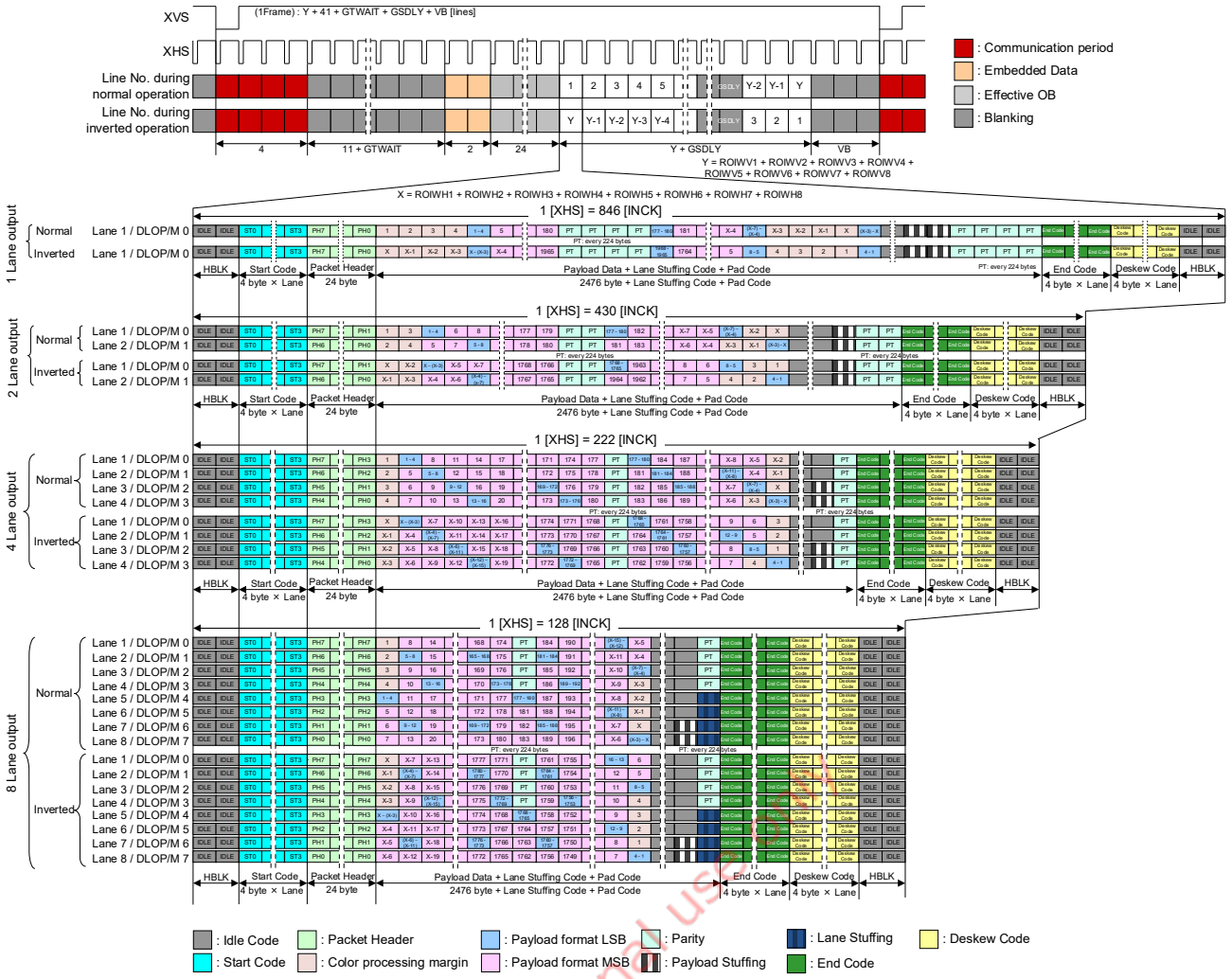
The example of ROI setting is shown below.
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 600
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 8 (minimum value)

Frame rate List of each setting

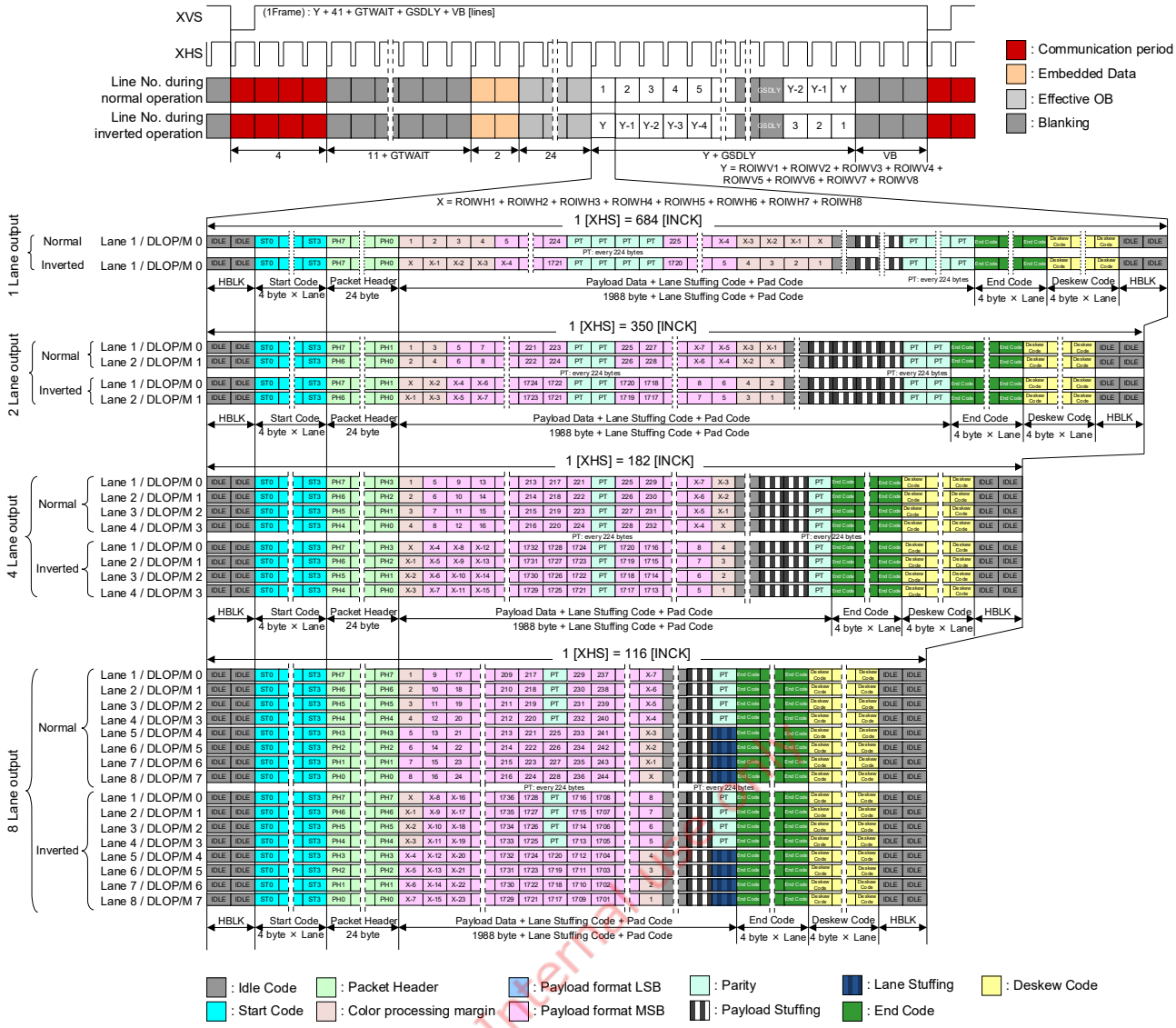
Register settings No. in register list	1 H period [µs]		Frame rate [frame/s]			
	FREQ 0h	FREQ 1h	Total number of ROI: 600 [line]		Total number of ROI: 8 [line]	
			FREQ = 0h	FREQ = 1h	FREQ = 0h	FREQ = 1h
*1	1.56	2.66	924.98	558.03	6400.86	4687.50
*2	2.45	4.87	603.50	310.77	4856.75	3016.33
*3	4.71	9.37	321.42	161.63	3119.74	1568.83
*4	9.21	18.37	164.47	82.98	1596.36	850.55
*5	1.72	3.20	843.13	467.02	6042.48	4104.93
*6	2.98	5.95	497.70	254.52	4180.74	2470.38
*7	5.79	11.55	261.62	131.91	2539.32	1352.16
*8	11.39	22.73	133.78	67.46	1371.34	733.11
*9	2.80	3.74	531.20	399.82	4462.13	3514.29
*10	3.55	7.05	421.03	214.69	3700.65	2083.80
*11	6.89	13.73	219.72	110.96	2132.64	1137.40
*12	13.58	27.10	112.28	56.60	1150.94	615.05



Drive Timing Chart for Serial Output in ROI Mode (SLVS - EC output, AD 12bit)



Drive Timing Chart for Serial Output in ROI Mode (SLVS - EC output, AD 10bit)



Drive Timing Chart for Serial Output in ROI Mode (SLVS - EC output, AD 8bit)

Overlap ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 8 areas, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All - pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, this sensor doesn't support ROI mode.
This sensor support ROI + 2 × 2 Vertical FD binning mode.
This section is written in case of all - pixel scan mode for example on this document.

When SLVS output

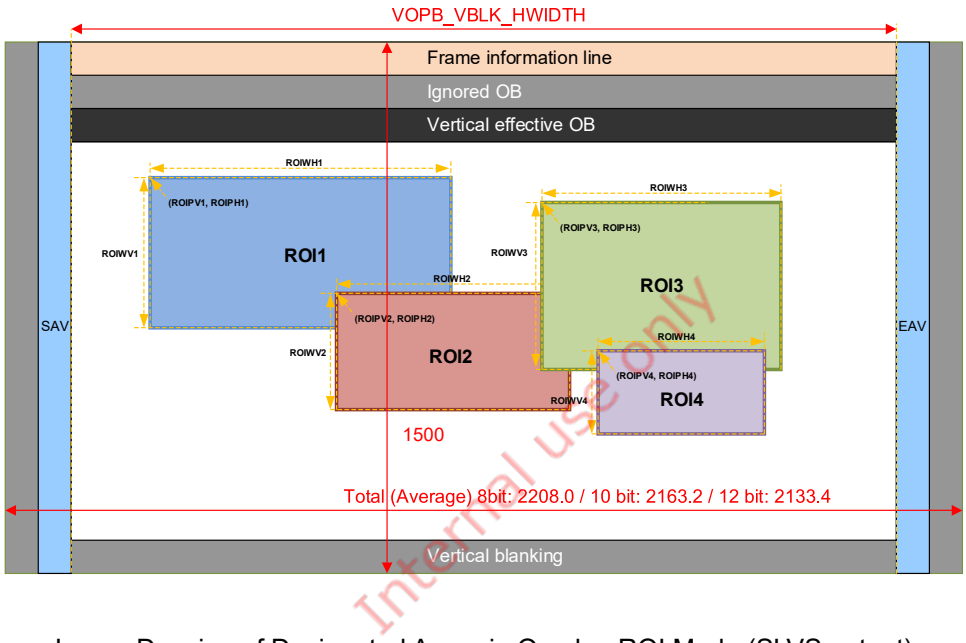
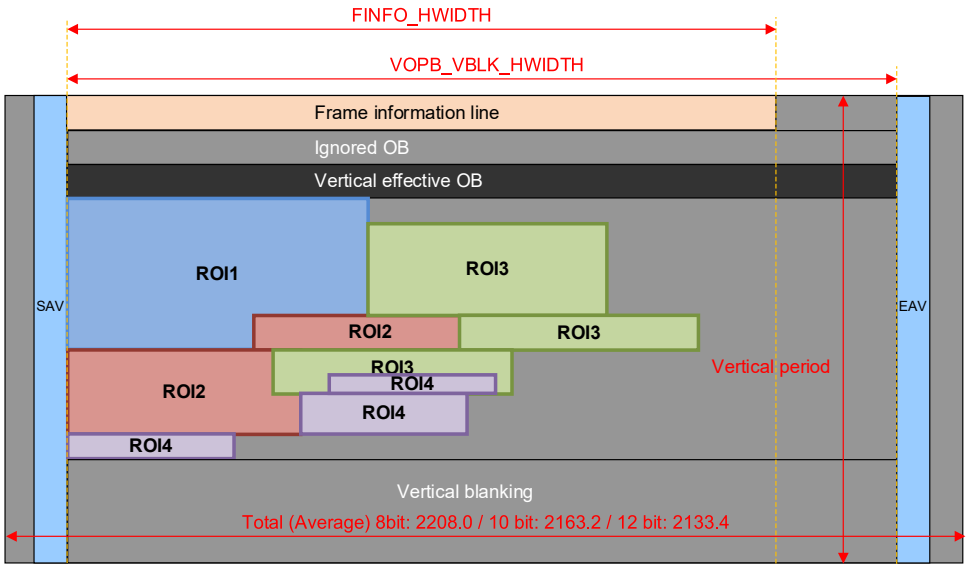


Image Drawing of Designated Areas in Overlap ROI Mode (SLVS output)



Details of Image Drawing (SLVS output)

Register List of Overlap ROI mode

Please set ROI mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	
Chip ID = 02h										
D0h	[7:0]	VOPB_VBLK_HWIDTH	0798h	VOPB effective area and V Blank width setting						
D1h	[4:0]									
D2h	[7:0]	FINFO_HWIDTH	0410h	FINFO width setting						
D3h	[4:0]									
Chip ID = 03h										
00h	[1]	OVERLAP_ROI_EN	0h	1h						

Restrictions on Overlap ROI mode

The register settings should satisfy following conditions:

ROIPH1 + ROIWH1 ≤ 1944d
ROIPH2 + ROIWH2 ≤ 1944d
ROIPH3 + ROIWH3 ≤ 1944d
…
ROIPH8 + ROIWH8 ≤ 1944d

ROIPV1 + ROIWV1 ≤ 1472d
ROIPV2 + ROIWV2 ≤ 1472d
ROIPV3 + ROIWV3 ≤ 1472d
…
ROIPV8 + ROIWV8 ≤ 1472d

16d ≤ VOPB_VBLK_HWIDTH ≤ 1944d

FINFO_HWIDTH ≤ 1944d

* Set the horizontal width, VOPB width and FINFO width setting in multiple of 4 and horizontal position and vertical position / width setting in multiple of 8.

* Minimum width of the window is as below.
ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d

ROIWV1 ≥ 8d, ROIWV2 ≥ 8d, ROIWV3 ≥ 8d, … ROIWV8 ≥ 8d

*Minimum output width is as below.
10 / 12 bit mode
Minimum horizontal output width ≥ 260d
FINFO_HWIDTH ≥ 260d

8 bit mode
Minimum horizontal output width ≥ 516d
FINFO_HWIDTH ≥ 516d

8 / 10 / 12 bit mode
Minimum vertical output width ≥ 8d

Frame rate on Overlap ROI mode

Frame rate [frame/s] = 1 / (("Number of lines per frame" or VMAX) × (1 H period))
When the maximum vertical output width is 600 or 8 lines, refer to ROI mode.

When SLVS - EC output

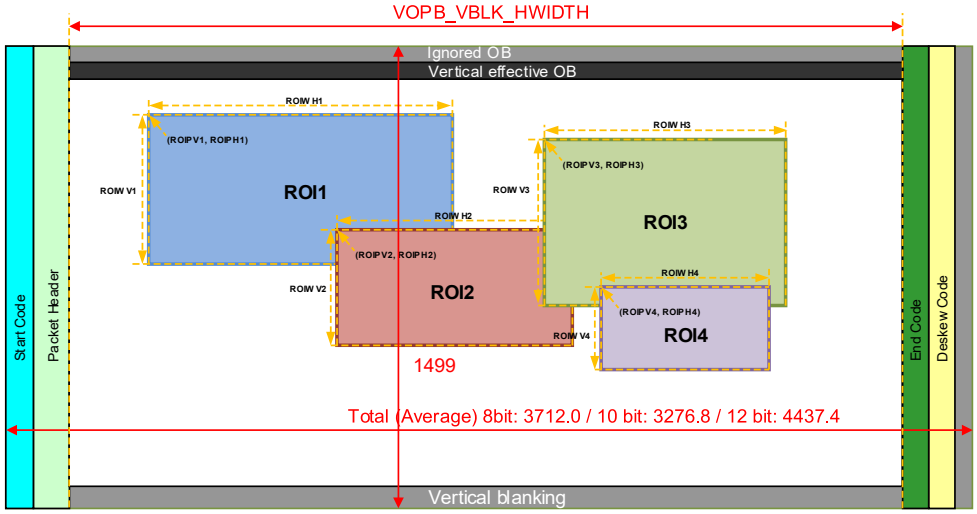
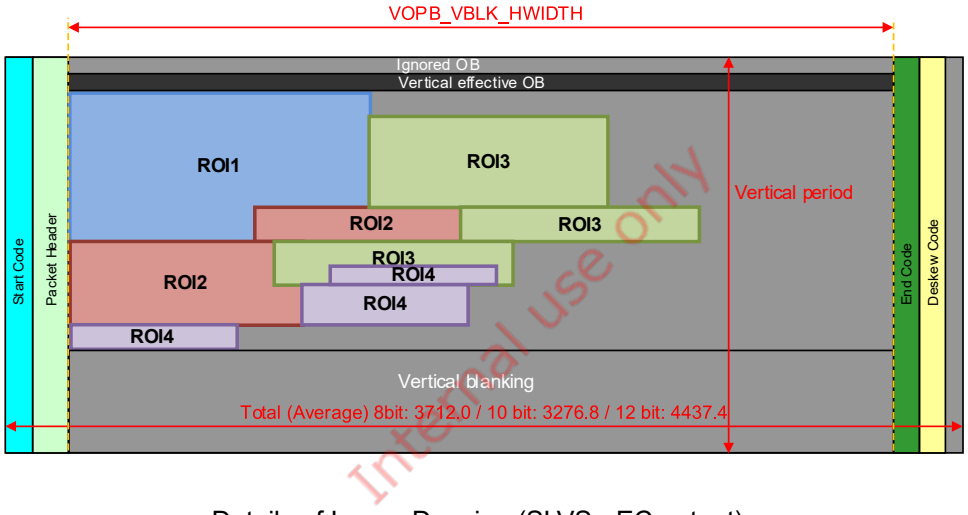


Image Drawing of Designated Areas in Overlap ROI Mode (SLVS - EC output)



Details of Image Drawing (SLVS - EC output)

Register List of Overlap ROI mode

Please set ROI mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				*1 [frame/s]	*2 [frame/s]	*3 [frame/s]	*4 [frame/s]	*5 [frame/s]	*6 [frame/s]	*7 [frame/s]	*8 [frame/s]	*9 [frame/s]	*10 [frame/s]	*11 [frame/s]	*12 [frame/s]	
Chip ID = 02h																
D0h	[7:0]	VOPB_VBLK_ HWIDTH	0C90h	VOPB effective area and V Blank width setting												
D1h	[4:0]															
Chip ID = 03h																
00h	[1]	OVERLAP_ROI_EN	0h	1h												

Restrictions on Overlap ROI mode

The register settings should satisfy following conditions:

ROIPH1 + ROIWH1 ≤ 1944d
ROIPH2 + ROIWH2 ≤ 1944d
ROIPH3 + ROIWH3 ≤ 1944d
…
ROIPH8 + ROIWH8 ≤ 1944d

ROIPV1 + ROIWV1 ≤ 1472d
ROIPV2 + ROIWV2 ≤ 1472d
ROIPV3 + ROIWV3 ≤ 1472d
…
ROIPV8 + ROIWV8 ≤ 1472d

16d ≤ VOPB_VBLK_HWIDTH ≤ 1944d

* Set the horizontal width, VOPB width setting in multiple of 4 and horizontal position and vertical position / width setting in multiple of 8.

* Minimum width of the window is as below.
ROIWH1 ≥ 8d, ROIWH2 ≥ 8d, ROIWH3 ≥ 8d, …. ROIWH8 ≥ 8d

ROIWV1 ≥ 8d, ROIWV2 ≥ 8d, ROIWV3 ≥ 8d, … ROIWV8 ≥ 8d

*Minimum output width is as below.
10 / 12 bit mode
Minimum horizontal output width ≥ 260d

8 bit mode
Minimum horizontal output width ≥ 516d

8 / 10 / 12 bit mode
Minimum vertical output width ≥ 8d

Frame rate on Overlap ROI mode

Frame rate [frame/s] = 1 / ((“Number of lines per frame” or VMAX) × (1 H period))
When the maximum vertical output width is 600 or 8 lines, refer to ROI mode.

Vertical / Horizontal 1/2 Subsampling mode

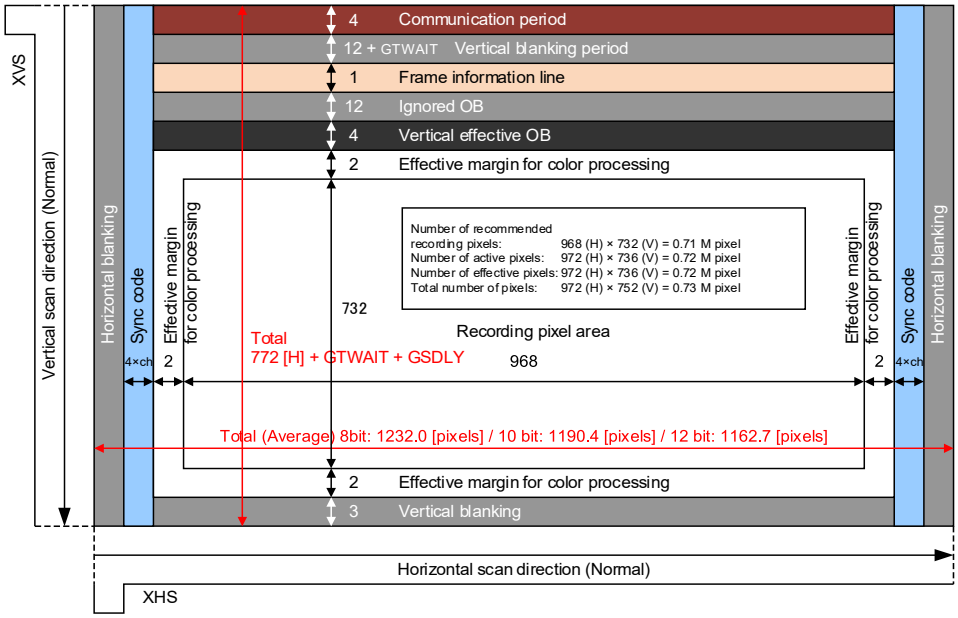
V direction and H direction must be set in this mode. (WINMODE = 1h, HMODE = 1)

When SLVS output

Register List of Vertical / Horizontal 1/2 subsampling mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				596.7 [frame/s]	337.9 [frame/s]	498.9 [frame/s]	277.3 [frame/s]	425.7 [frame/s]	235.5 [frame/s]	FREQ = 0h
				317.2 [frame/s]	175.1 [frame/s]	263.2 [frame/s]	142.3 [frame/s]	222.2 [frame/s]	120.1 [frame/s]	FREQ = 1h
Chip ID = 02h										
3Ch	[3:0]	WINMODE	0h	1h						Subsampling mode
	[4]	HMODE	0	1						Subsampling
D4h	[7:0]	VMAX	618h	328h	31Ch	320h	318h	320h	314h	FREQ = 0h
D5h	[7:0]			31Ch	314h	314h	314h	314h	310h	FREQ = 1h
D6h	[7:0]									
D8h	[7:0]	HMAX	080h	09Ah	114h	0BAh	152h	0DAh	190h	FREQ = 0h
D9h	[7:0]			126h	21Ah	166h	296h	1A8h	314h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	18h	14h	0Ch	10h	0Ch	10h	08h	FREQ = 0h
				0Ch	08h	08h	08h	08h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	10h	0Ch	0Ch	08h	0Ch	08h	FREQ = 0h
				0Ch	08h	08h	08h	08h	08h	FREQ = 1h
Chip ID = 04h										
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]		0Eh	10h						
31h	[1:0]									
Chip ID = 06h										
44h	[3:0]	STBSLVS	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	2h	N/A	2h	N/A	2h	4 ch SLVS
45h	[3:0]	OPORTSEL	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	4 ch SLVS



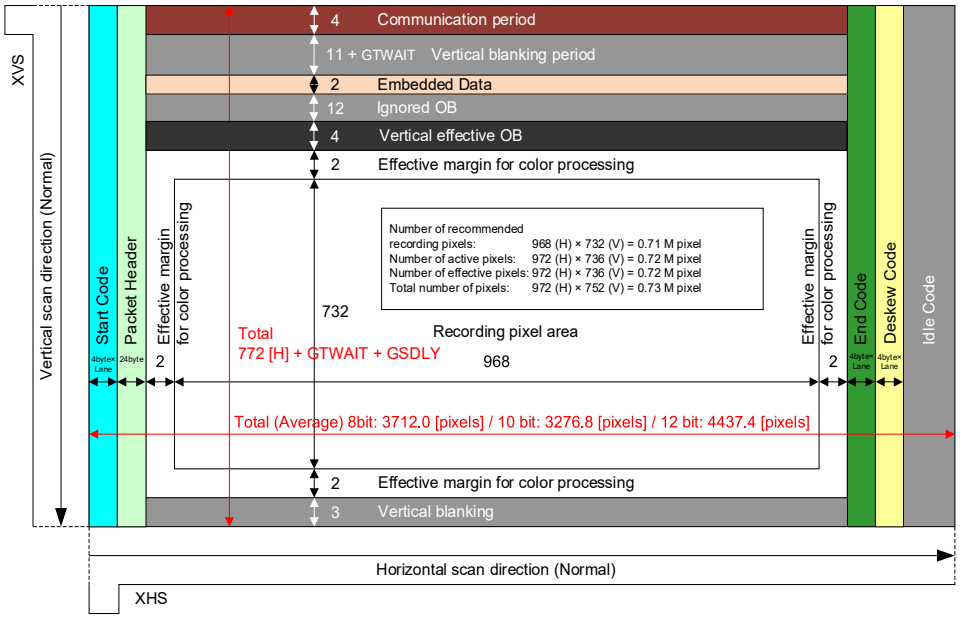
Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode
(SLVS output Shutter stabilization wait time is not included)

When SLVS - EC output

Register List of Vertical / Horizontal 1/2 subsampling mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				780.5 [frame/s]	780.5 [frame/s]	493.6 [frame/s]	261.7 [frame/s]	710.8 [frame/s]	710.8 [frame/s]	407.0 [frame/s]	214.1 [frame/s]	446.2 [frame/s]	446.2 [frame/s]	348.0 [frame/s]	180.5 [frame/s]	FREQ = 0h
				780.5 [frame/s]	464.0 [frame/s]	253.3 [frame/s]	132.2 [frame/s]	672.3 [frame/s]	388.6 [frame/s]	208.4 [frame/s]	107.8 [frame/s]	446.2 [frame/s]	333.1 [frame/s]	176.4 [frame/s]	91.0 [frame/s]	FREQ = 1h
Chip ID = 02h																
3Ch	[3:0]	WINMODE	0h	1h												Subsampling mode
	[4]	HMODE	0	1												Subsampling
D4h	[7:0]	VMAX	618h	334h	334h	320h	314h	330h	330h	320h	314h	320h	320h	31Ch	314h	FREQ = 0h
D5h	[7:0]			334h	320h	314h	310h	32Ch	31Ch	314h	310h	320h	31Ch	314h	310h	FREQ = 1h
D6h	[7:0]															
D8h	[7:0]	HMAX	080h	074h	074h	0BCh	168h	080h	080h	0E4h	1B8h	0D0h	0D0h	10Ch	20Ah	FREQ = 0h
D9h	[7:0]			074h	0C8h	174h	2CCh	088h	0F0h	1C4h	36Eh	0D0h	118h	216h	410h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h												
E2h	[7:0]	GTWAIT	18h	1Ch	1Ch	10h	08h	18h	18h	10h	08h	10h	10h	0Ch	08h	FREQ = 0h
				1Ch	10h	08h	04h	18h	0Ch	08h	04h	10h	0Ch	08h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	14h	14h	0Ch	08h	14h	14h	0Ch	08h	0Ch	0Ch	0Ch	08h	FREQ = 0h
				14h	0Ch	08h	08h	10h	0Ch	08h	08h	0Ch	0Ch	08h	08h	FREQ = 1h
Chip ID = 04h																
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 83h FREQ = 1: 93h												
30h	[7:2]		0Eh	10h												
31h	[1:0]															
Chip ID = 0Bh																
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	8 Lane
				N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	4 Lane
				N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	2 Lane
				N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	1 Lane



Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode
(SLVS - EC output Shutter stabilization wait time is not included)

2 × 2 Vertical FD binning mode

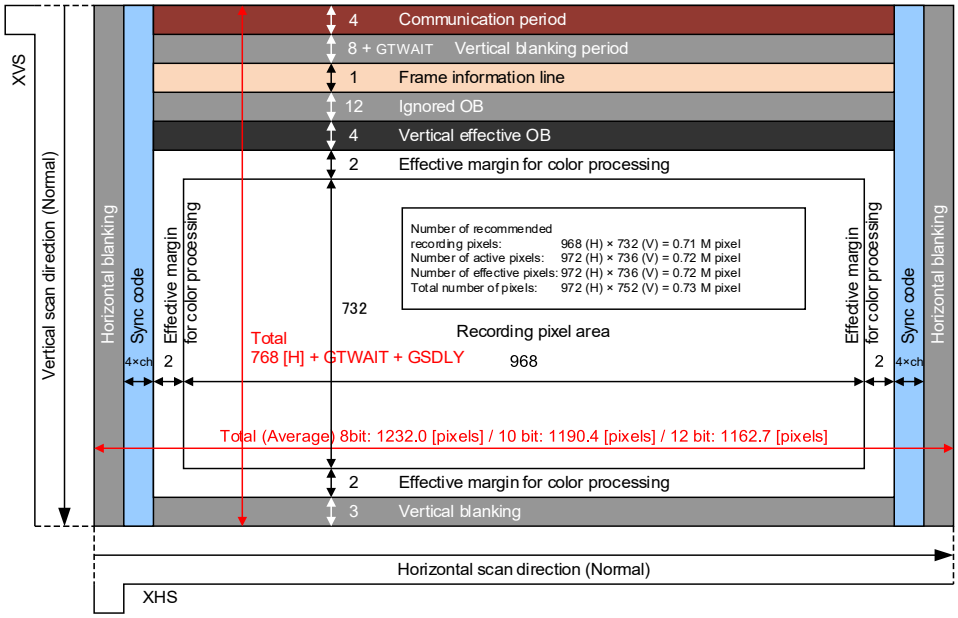
By setting 2 × 2 Vertical FD binning mode, the frame rate becomes faster than All - pixel mode.
V direction and H direction must be set in this mode. (WINMODE = 2h, HADD_ON = 1)

When SLVS output

Register List of 2 × 2 Vertical FD binning mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value						Remarks
				AD = 8 bit		AD = 10 bit		AD = 12 bit		
				599.6 [frame/s]	339.6 [frame/s]	501.5 [frame/s]	278.7 [frame/s]	427.8 [frame/s]	236.7 [frame/s]	FREQ = 0h
				318.8 [frame/s]	176.0 [frame/s]	264.5 [frame/s]	143.0 [frame/s]	223.3 [frame/s]	120.8 [frame/s]	FREQ = 1h
Chip ID = 02h										
3Ch	[3:0]	WINMODE	0h	2h						Binning mode
D4h	[7:0]	VMAX	618h	324h	318h	31Ch	314h	31Ch	310h	FREQ = 0h
D5h	[7:0]			318h	310h	310h	310h	310h	30Ch	FREQ = 1h
D6h	[7:0]									
D8h	[7:0]	HMAX	080h	09Ah	114h	0BAh	152h	0DAh	190h	FREQ = 0h
D9h	[7:0]			126h	21Ah	166h	296h	1A8h	314h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h						
E2h	[7:0]	GTWAIT	18h	14h	0Ch	10h	0Ch	10h	08h	FREQ = 0h
				0Ch	08h	08h	08h	08h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	10h	0Ch	0Ch	08h	0Ch	08h	FREQ = 0h
				0Ch	08h	08h	08h	08h	08h	FREQ = 1h
Chip ID = 04h										
00h	[1:0]		0h	0h						
	[3]	HADD_ON	0	1						Binning ON
	[4]	HADD_ON_SEL	0	0 / 1						Binning on CLIP = 0 Average = 1
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h						
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h						
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 93h FREQ = 1: A3h						
30h	[7:2]		0Eh	0Ch						
31h	[1:0]									
Chip ID = 06h										
44h	[3:0]	STBSLVS	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	2h	N/A	2h	N/A	2h	4 ch SLVS
45h	[3:0]	OPORTSEL	1h	1h	N/A	1h	N/A	1h	N/A	8 ch SLVS
				N/A	3h	N/A	3h	N/A	3h	4 ch SLVS



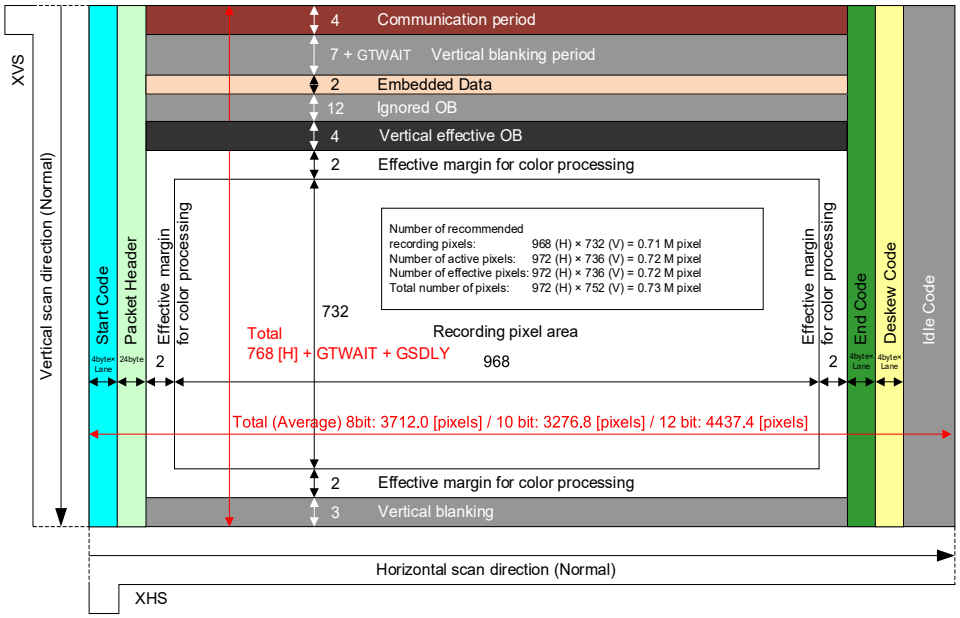
Pixel Array Image Drawing in 2 × 2 Vertical FD binning mode
(SLVS output Shutter stabilization wait time is not included)

When SLVS - EC output

Register List of 2 × 2 Vertical FD binning mode

Please set All - pixel scan mode to the settings other than the following.

Address	bit	Register name	Initial Value	Setting value												Remarks
				AD = 8 bit				AD = 10 bit				AD = 12 bit				
				784.4 [frame/s]	784.4 [frame/s]	496.1 [frame/s]	263.0 [frame/s]	714.3 [frame/s]	714.3 [frame/s]	409.1 [frame/s]	215.2 [frame/s]	448.4 [frame/s]	448.4 [frame/s]	349.8 [frame/s]	181.4 [frame/s]	FREQ = 0h
				784.4 [frame/s]	466.3 [frame/s]	254.5 [frame/s]	132.9 [frame/s]	675.6 [frame/s]	390.6 [frame/s]	209.5 [frame/s]	108.4 [frame/s]	448.4 [frame/s]	334.8 [frame/s]	177.3 [frame/s]	91.5 [frame/s]	FREQ = 1h
Chip ID = 02h																
3Ch	[3:0]	WINMODE	0h	2h												Binning mode
D4h	[7:0]	VMAX	618h	330h	330h	31Ch	310h	32Ch	32Ch	31Ch	310h	31Ch	31Ch	318h	310h	FREQ = 0h
D5h	[7:0]			330h	31Ch	310h	30Ch	328h	318h	310h	30Ch	31Ch	318h	310h	30Ch	FREQ = 1h
D6h	[7:0]															
D8h	[7:0]	HMAX	080h	074h	074h	0BCh	168h	080h	080h	0E4h	1B8h	0D0h	0D0h	10Ch	20Ah	FREQ = 0h
D9h	[7:0]			074h	0C8h	174h	2CCh	088h	0F0h	1C4h	36Eh	0D0h	118h	216h	410h	FREQ = 1h
DCh	[1:0]	FREQ	0h	0h / 1h												
E2h	[7:0]	GTWAIT	18h	1Ch	1Ch	10h	08h	18h	18h	10h	08h	10h	10h	0Ch	08h	FREQ = 0h
				1Ch	10h	08h	04h	18h	0Ch	08h	04h	10h	0Ch	08h	04h	FREQ = 1h
E3h	[7:0]	GSDLY	14h	14h	14h	0Ch	08h	14h	14h	0Ch	08h	0Ch	0Ch	0Ch	08h	FREQ = 0h
				14h	0Ch	08h	08h	10h	0Ch	08h	08h	0Ch	0Ch	08h	08h	FREQ = 1h
Chip ID = 04h																
00h	[1:0]		0h	0h												
	[3]	HADD_ON	0	1												Binning ON
	[4]	HADD_ON_SEL	0	0 / 1												Binning on CLIP = 0 Average = 1
20h	[7:0]	INCKSEL0	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
21h	[7:0]	INCKSEL1	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
24h	[7:0]	INCKSEL2	52h	INCK = 37.125 MHz / 54 MHz: 50h INCK = 74.25 MHz: 52h												
25h	[7:0]	INCKSEL3	20h	INCK = 37.125 MHz / 74.25 MHz: 20h INCK = 54 MHz: 16h												
26h	[7:0]	FREQ_SYNC	83h	FREQ = 0: 83h FREQ = 1: 93h												
30h	[7:2]		0Eh	0Ch												
31h	[1:0]															
Chip ID = 0Bh																
04h	[2:0]	LANESEL	0h	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	0h	N/A	N/A	N/A	8 Lane
				N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	N/A	2h	N/A	N/A	4 Lane
				N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	N/A	N/A	3h	N/A	2 Lane
				N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	N/A	N/A	N/A	4h	1 Lane



Pixel Array Image Drawing in 2 × 2 Vertical FD binning mode
(SLVS - EC Shutter stabilization wait time is not included)

Description of Various Function

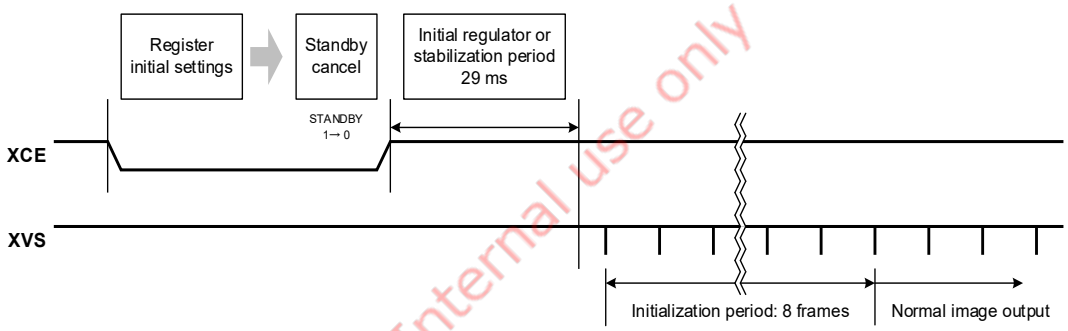
Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit			
STANDBY	02h	00h (3000h)	[0]	1h	1h: Standby 0h: Operating	Register communication is executed even in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (29 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [23:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.

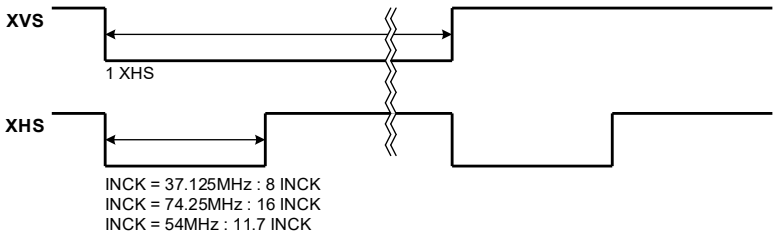
Pin Processing

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master mode	High: OV_{DD} Low: GND
	High fixed	Slave mode	

Register List of Slave Mode and Master Mode

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I^2C	Bit			
XMSTA	02h	0Ch (300Ch)	[0]	1h	1h: Master operation ready (Initial value) 0h: Master operation start	The master operation starts by setting 0.
VMAX [23:0]		D4h (30D4h)	[7:0]	000618h	See the item of each drive mode	Line number per frame designated (Master mode and Slave mode common setting.)
		D5h (30D5h)	[7:0]			
		D6h (30D6h)	[7:0]			
HMAX [15:0]		D8h (30D8h)	[7:0]	0080h	See the item of each drive mode	Clock number per line designated (Master mode and Slave mode common setting.)
		D9h (30D9h)	[7:0]			

XVS / XHS Output Waveform in Master Mode



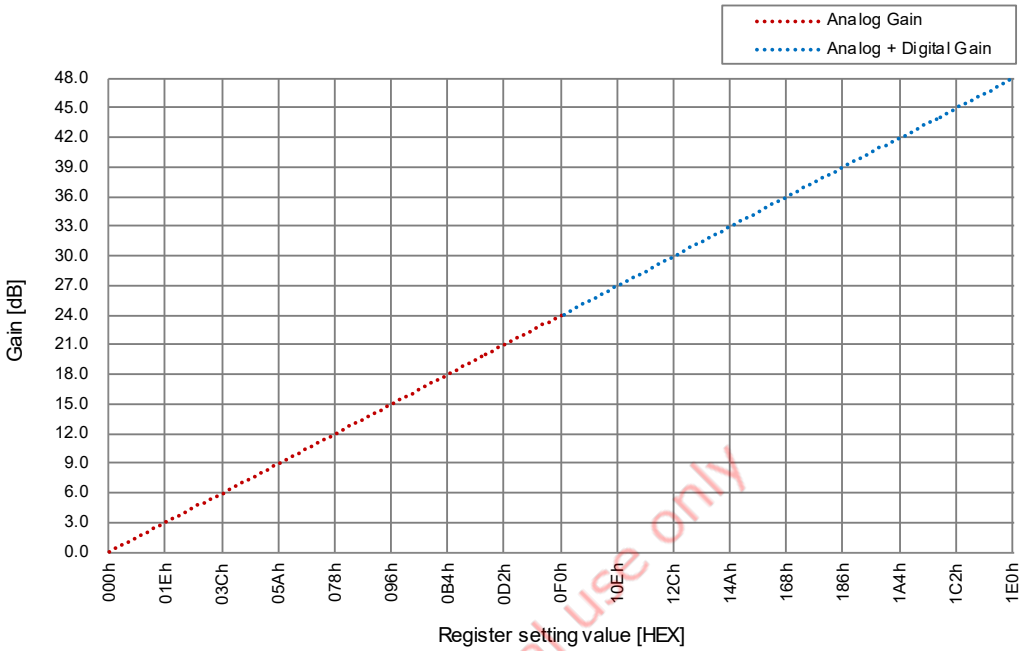
Gain Adjustment Function

PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.
The value which is ten times the gain is set to register.

Example)
When set to 6 dB:

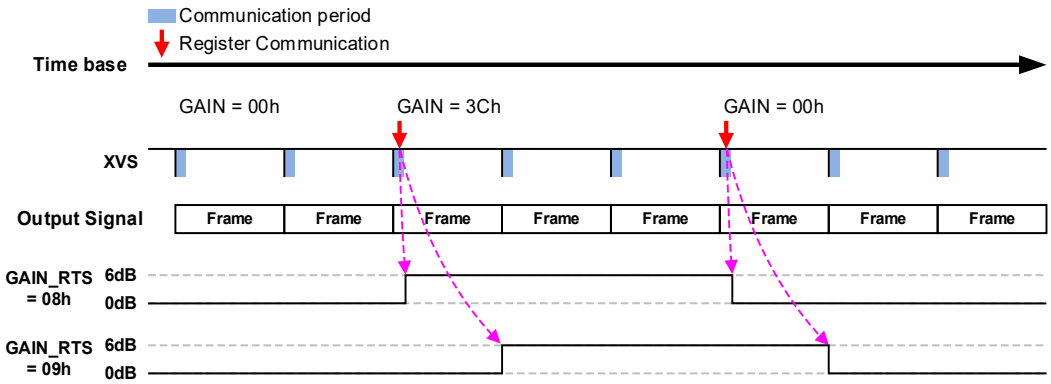
6 × 10 = 60d, GAIN = 03Ch



Register List of Gain setting

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit		Setting range	
GAIN [8:0]	07h	14h (3514h)	[7:0]	000h	000h to 1E0h (0d to 480d)	Setting value: Gain [dB] × 10
		15h (3515h)	[0]			

Gain Reflection Timing is changed by the set value of GAIN_RTS as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to FFFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  8 bit output: 00Fh (15 d)
  10 bit output: 03Ch (60 d)
  12 bit output: 0F0h (240 d)

Register List of Black level adjustment

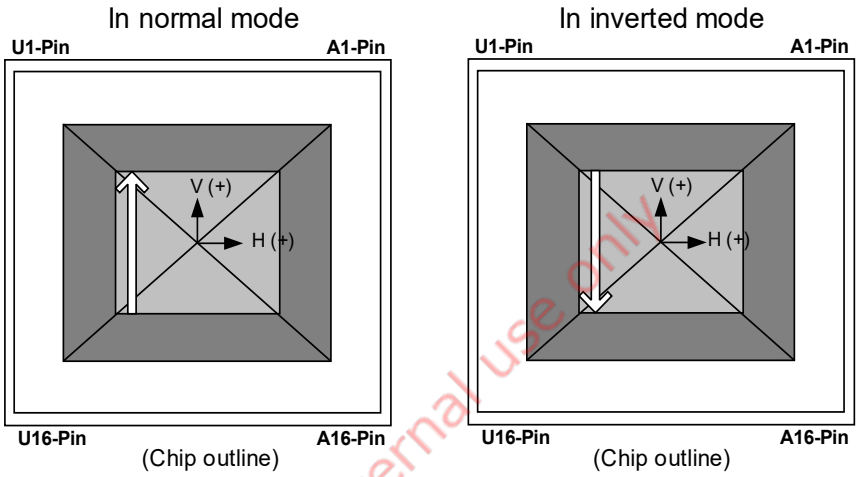
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
BLKLEVEL [11:0]	07h	C0h (35C0h)	[7:0]	03Ch	000h to FFFh
		C1h (35C1h)	[3:0]		

Horizontal / Vertical Normal Operation and Inverted Operation

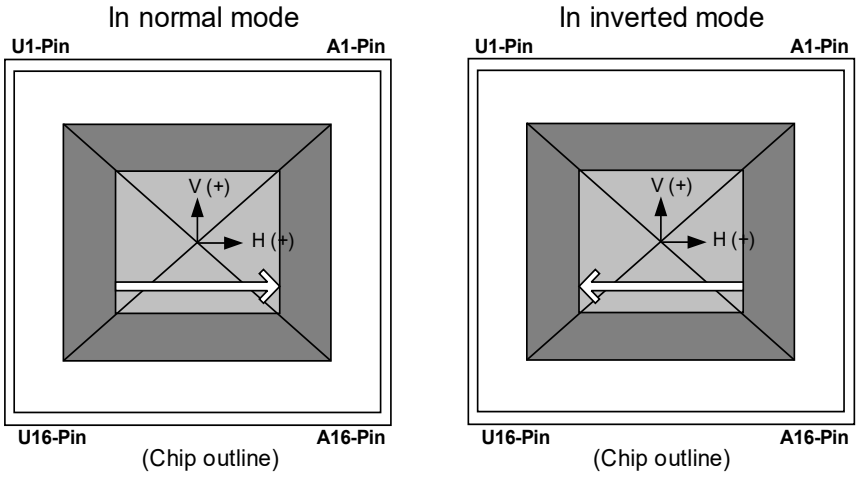
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of “Readout Drive Modes” for the order of readout lines in normal and inverted modes.

Register List of Readout Drive Direction setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VREVERSE	04h	04h (3204h)	[0]	0h	0h: Normal (Initial value) 1h: Inverted
HREVERSE			[1]	0h	0h: Normal (Initial value) 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a global shutter function that integrates to all line collectively by using memory in each pixel.
This sensor has a variable electronic shutter function that can control the integration time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal.
This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

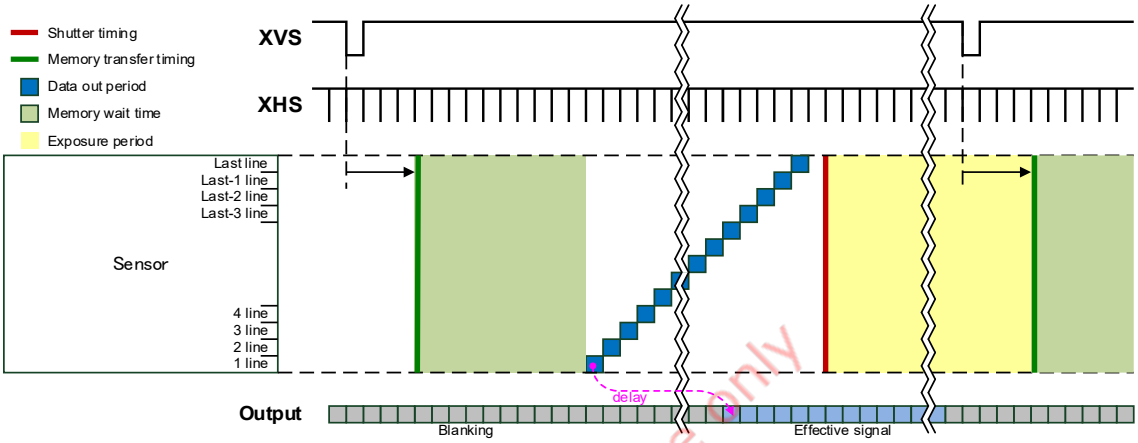


Image Drawing of Global Shutter (Normal mode) Operation

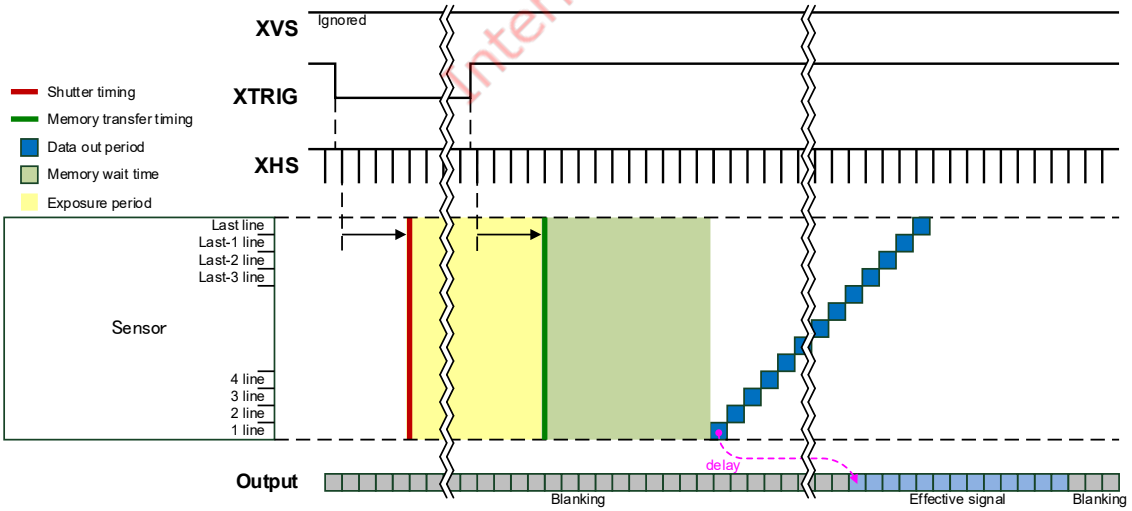


Image Drawing of Global Shutter (Sequential Trigger mode) Operation

Global Shutter (Normal Mode) Operation

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS [23:0] register. For setting value of SHS [23:0], see the table “List of Exposure Setting”. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [23:0] register. The number of lines per frame differs according to the operating mode.

Calculation Formula of Exposure Time

Exposure time [s] = (1 H period) × (Number of lines per frame - SHS) + 4.997 [μs][*1]

[*1]: Exposure time error (t_{OFFSET})

Register List of Shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
VMAX [23:0]	02h	D4h (30D4h)	[7:0]	000618h	Set the number of lines per frame (only in master mode)
		D5h (30D5h)	[7:0]		
		D6h (30D6h)	[7:0]		
GTWAIT [7:0]		E2h (30E2h)	[7:0]	18h	The setting refers to GTWAIT table and hexadecimal notation.
SHS [23:0]	04h	40h (3240h)	[7:0]	000018h	Sets the shutter sweep time. memory wait time (GTWAIT value) to (Number of lines per frame - 1)
		41h (3241h)	[7:0]		
		42h (3242h)	[7:0]		

List of Exposure Setting

SLVS output

Drive mode	memory wait time [H]	Number of lines per frame [DEC]	SHS Setting value [DEC]	Exposure Setting value [H]	AD 12bit, FREQ 0, 8 ch output (Maximum frame rate)	
					Frame rate [frame/s]	Actually exposure [ms]*3
All - pixel	8 (GTWAIT*1)	1532 (VMAX)	1531	1	121.1	0.010
			1530	2		0.016
			…	…		…
			9	1523		8.210
			8	1524		8.215
1080p - Full HD	6 (GTWAIT*1)	1125 (VMAX)	1124	1	120.0	0.012
			1123	2		0.019
			…	…		…
			7	1118		7.925
			6	1119		7.932
ROI Overlap ROI	GTWAIT*1 (All - pixel)	V_{TR}*2	V_{TR}-1	1	*3	0.010
			V_{TR}-2	2		0.016
			…	…		…
			9	V_{TR}-9		*4
			8	V_{TR}-8		

SLVS - EC output

Drive mode	memory wait time [H]	Number of lines per frame [DEC]	SHS Setting value[DEC]	Exposure Setting value[H]	AD 12bit, FREQ 0, 8 Lane output (Maximum frame rate)	
					Frame rate [frame/s]	Actually exposure [ms]*3
All - pixel	16 (GTWAIT*1)	1544 (VMAX)	1543	1	231.2	0.008
			1542	2		0.011
			…	…		…
			17	1527		4.283
			16	1528		4.285
ROI Overlap ROI	GTWAIT*1 (All - pixel)	V_{TR}*2	V_{TR}-1	1	*3	0.008
			V_{TR}-2	2		0.011
			…	…		…
			17	V_{TR}-17		*4
			16	V_{TR}-16		

*1 GTWAIT, refer to the table below. (Unit is XHS and decimal notation)
*2 V_{TR} and the frame rate, refer to the section “ROI mode” in “Readout Drive Mode”.
*3 INCK frequency is input by typical value, and t_{OFFSET} (4.997 [µs]) is included.
*4 Conform to the calculation formula of exposure time. (Number of lines per frame = V_{TR})

GTWAIT [H]		All - pixel, ROI						1 / 2 Subsampling						2 × 2 Vertical FD binning mode					
FREQ		FREQ = 0			FREQ = 1			FREQ = 0			FREQ = 1			FREQ = 0			FREQ = 1		
Output \ AD		8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit
SLVS	4 ch	8	8	4	4	4	4	12	12	8	8	8	4	12	12	8	8	8	4
	8 ch	12	12	8	8	8	4	20	16	16	12	8	8	20	16	16	12	8	8
SLVS - EC	1 Lane	8	4	4	4	4	4	8	8	8	4	4	4	8	8	8	4	4	4
	2 Lane	8	8	8	8	4	4	16	16	12	8	8	8	16	16	12	8	8	8
	4 Lane	16	16	12	8	8	8	28	24	16	16	12	12	28	24	16	16	12	12
	8 Lane	28	24	16	16	12	12	28	24	16	28	24	16	28	24	16	28	24	16

GTWAIT [H]		1080p - Full HD	
FREQ		FREQ = 0	
Output \ AD		10bit	12bit
SLVS	4 ch	6	
	8 ch		

GSDLY [H]		All - pixel, ROI						1 / 2 Subsampling						2 × 2 Vertical FD binning mode					
FREQ		FREQ = 0			FREQ = 1			FREQ = 0			FREQ = 1			FREQ = 0			FREQ = 1		
Output \ AD		8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit	8bit	10bit	12bit
SLVS	4 ch	8	8	8	8	8	8	12	8	8	8	8	8	12	8	8	8	8	8
	8 ch	12	8	8	8	8	8	16	12	12	12	8	8	16	12	12	12	8	8
SLVS - EC	1 Lane	8	8	8	8	4	4	8	8	8	8	8	8	8	8	8	8	8	8
	2 Lane	8	8	8	8	8	8	12	12	12	8	8	8	12	12	12	8	8	8
	4 Lane	16	12	12	8	8	8	20	20	12	12	12	12	20	20	12	12	12	12
	8 Lane	20	20	12	12	12	12	20	20	12	20	16	12	20	20	12	20	16	12

GSDLY [H]		1080p - Full HD	
FREQ		FREQ = 0	
Output \ AD		10bit	12bit
SLVS	4 ch	4	
	8 ch		

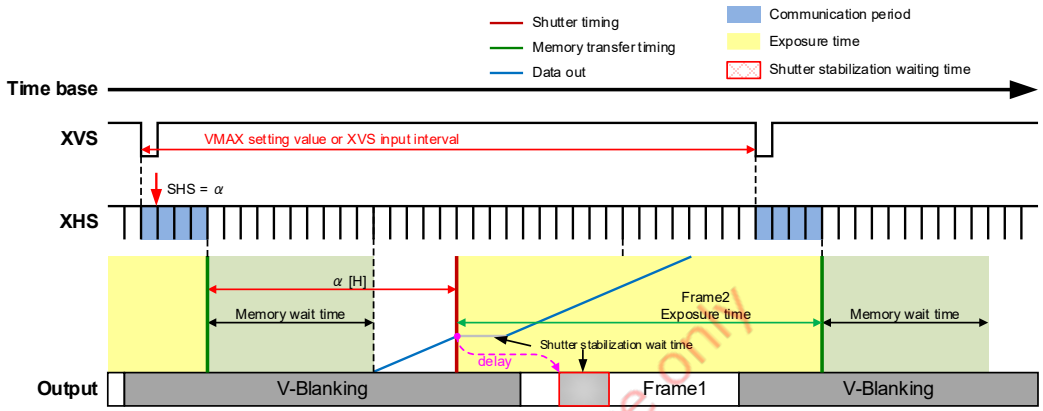


Image Drawing of Global Shutter (Normal Mode)

Global Shutter (Sequential Trigger Mode) Operation

The integration time can be controlled by varying the pulse width that is input to XTRIG1 pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to trigger mode, set 1 to the register TRIGEN. The XVS input signal is ignored during trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input (t_{TGPD}) and fall input (t_{TGES}) based on the previous trigger rise. When the trigger rise is input before the rise input prohibited period (t_{TGPD}), interrupt operation starts. This function is slave mode only. The number of lines per frame differs according to the operating mode. XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [H]*2) + 4.997 [µs]*1

*1: Exposure time error (t_{OFFSET})

*2: Low level pulse width is counted by XHS pulse.

Register List of shutter setting

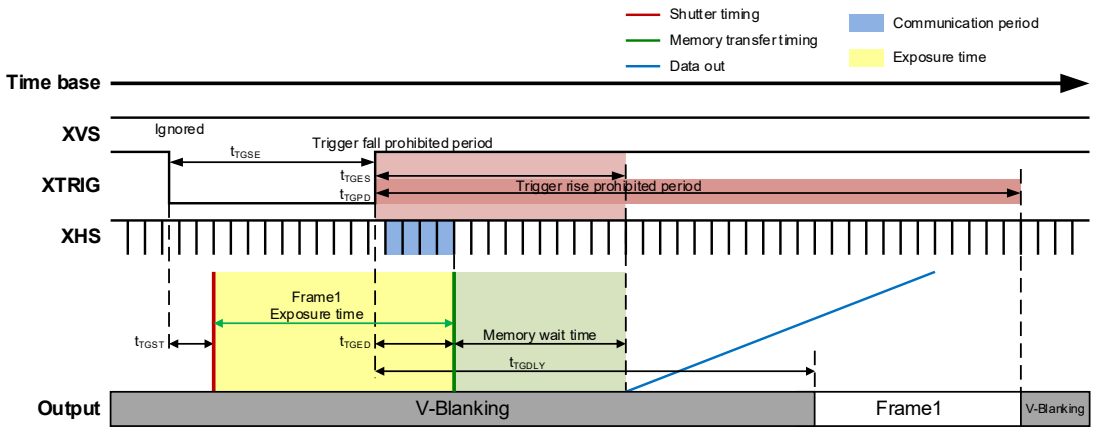
Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA	02h	0Ch (300Ch)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
VINT_EN	04h	32h (3232h)	[0]	1	Setting of Interrupt mode in Trigger Mode 0: V interrupt is disable 1: V interrupt is enable
TRIGEN	06h	00h (3400h)	[0]	0	Global shutter mode setting 0: Normal mode 1: Trigger mode

Parameter List of Global Shutter (Sequential Trigger Mode)

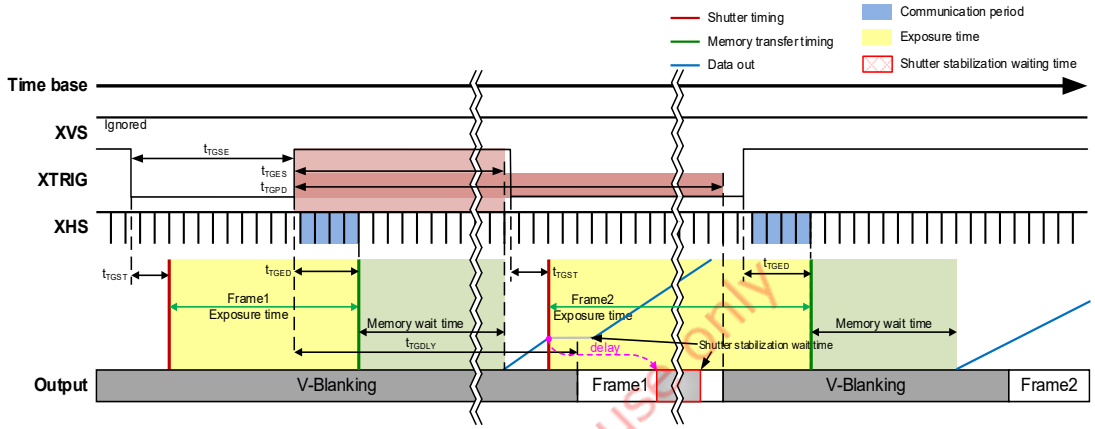
Item		Symbol	Min.	Typ.	Max.	Unit
Integration start delay		t_{TGST}	4	—	5	H
Integration end delay		t_{TGED}	4 + t_{OFFSET}	—	5 + t_{OFFSET}	H
Pulse width		t_{TGSE}	1	—	—	H
Next trigger fall prohibited period (All - pixel / 1080p - Full HD / ROI / 1 / 2 Subsampling / 2 × 2 Vertical FD binning mode)		t_{TGES}	5 + GTWAIT*1	—	—	H
Next trigger rise prohibited period (All - pixel / 1080p - Full HD / 1 / 2 Subsampling / 2 × 2 Vertical FD binning mode)		t_{TGPD}	VMAX	—	—	H
Next trigger rise prohibited period (ROI)			V_{TR}*2	—	—	
Data output delay (All - pixel / ROI)	SLVS	t_{TGDLY}	—	17 + GTWAIT*1	—	H
	SLVS - EC			16 + GTWAIT*1		
Data output delay (1080p - Full HD)			—	9 + GTWAIT*1	—	

*1 GTWAIT (Refer to preceding clause)

*2 V_{TR} (See the section “ROI mode” in “Readout Drive Mode”)



Single shutter Image Drawing of Global Shutter (Sequential Trigger Mode)



Multi shutter image Drawing of Global Shutter (Sequential Trigger Mode)

Interrupt Operation

In case of VINT_EN = 1h, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame 1 in the figure below), Frame 1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to t_{TGPD} in Parameter List of Global Shutter (Trigger Mode)
In case of VINT_EN = 0h, both of the rising edge and the falling edge of the trigger signal are ignored in t_{TGPD} (Prohibit period).

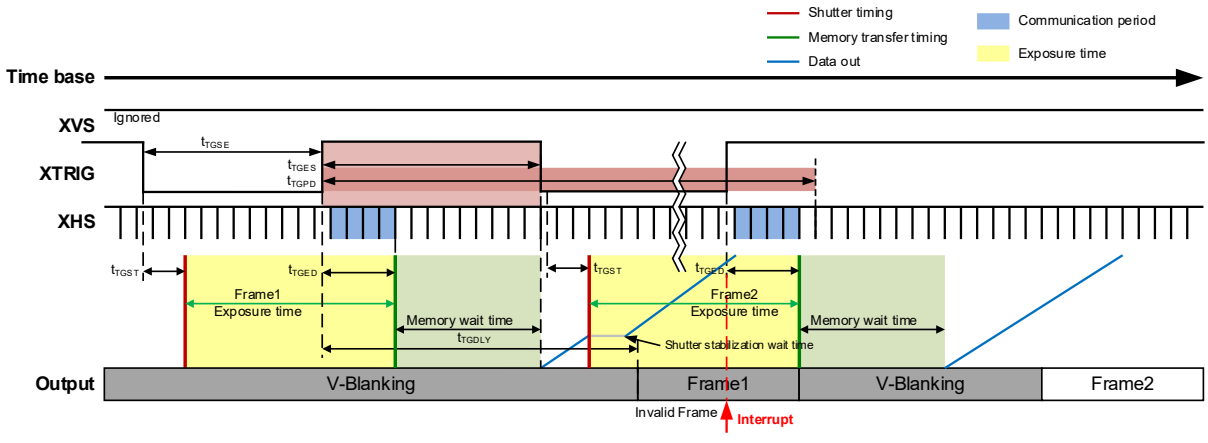


Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

Global Shutter (Fast Trigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG1 immediately.
This mode supports Master mode only.
XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence.

Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [µs]) + 4.997 [µs][*1]
[*1]: Exposure time error (t_{OFFSET})

Register List of shutter setting

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
XMSTA	02h	0Ch (300Ch)	[0]	1	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop
FASTTRIG	04h	30h (3230h)	[1]	0	Selection of trigger mode 0: Except for Fast trigger mode 1: Fast trigger mode
TRIGEN	06h	00h (3400h)	[0]	0	Global shutter mode setting 0: Normal mode 1: Trigger mode
SYNCSEL		3Ch (343Ch)	[5:4]	0h	XHS, XVS pin setting 0h: Normal Output 3h: Hi-Z

Parameter List of Global Shutter (Fast Trigger Mode)

Item		Symbol	Min.	Typ.	Max.	Unit
Integration start delay		t_{TGST}	—	—	0.13	µs
Integration end delay		t_{TGED}	—	—	0.13 + t_{OFFSET}	µs
Pulse width		t_{TGSE}	0.05	—	—	µs
Next trigger rise / fall prohibited period (All - pixel / 1 / 2 Subsampling)		t_{TGPD}	16 + VMAX	—	—	H
Next trigger rise / fall prohibited period (2 × 2 Vertical FD binning mode)			12 + VMAX	—	—	
Next trigger rise / fall prohibited period (1080p - Full HD)			8 + VMAX	—	—	
Next trigger rise / fall prohibited period (ROI)			16 + V_{TR}[*2]	—	—	
Data output delay (All - pixel / ROI)	SLVS	t_{TGDLY}	—	17 + GTWAIT[*1]	—	H
	SLVS - EC			16 + GTWAIT[*1]		
Data output delay (1080p - Full HD)			—	11 + GTWAIT[*1]	—	

[*1] GTWAIT (Refer to preceding clause)
[*2] V_{TR} (See the section “ROI mode” in “Readout Drive Mode”)

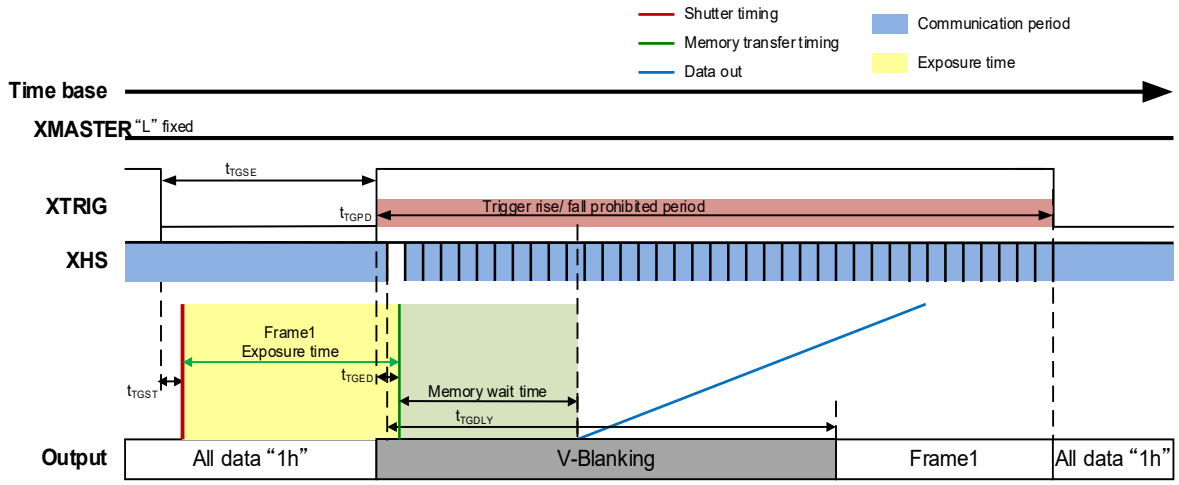


Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGEN. The sensor will transition to normal mode or trigger mode GTWAIT (H) after the register TRIGEN is set.
(The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to trigger mode after setting 1d to register TRIGEN. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a GTWAIT (H) period after the register TRIGEN is set. When TRIGEN is set during data read, read operation is stopped and that frame becomes an invalid frame.
* The communication is available till 9 H period only when sensor transition to the Trigger mode.

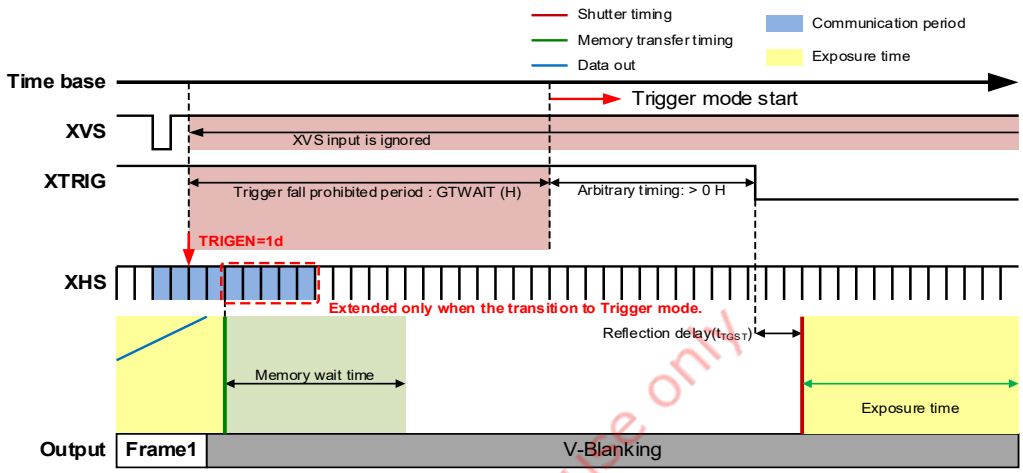


Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

Transition from Sequential Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting 0d to register TRIGEN. Start XVS input after transition to normal mode. Set TRIGEN after Next trigger rise prohibited period (t_{TGPD}) has passed. When TRIGEN is set before t_{TGPD}, read operation is stopped and that frame becomes an invalid frame.

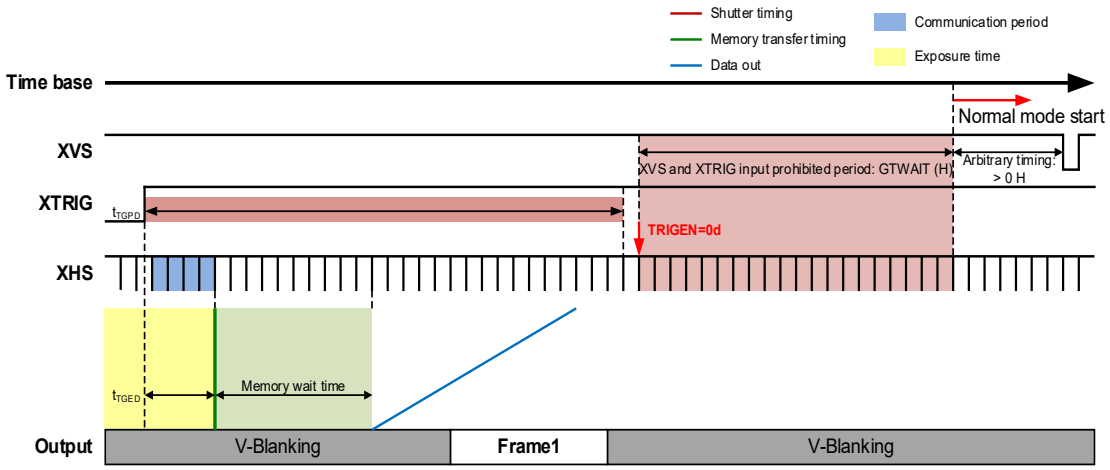


Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation. The pulse output from TOUT1 pin and TOUT2 pin. The rise timing and fall timing of pulse are set by Register. For the reference point (The timing when register value set to 0) to be set, see the table “List of Reference point". The pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the “List of Reference point". This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
TOUT1SEL [1:0]	06h	35h (3435h)	[1:0]	0h	TOUT1 pin setting 0h: Low fixed 3h: Pulse output
TOUT2SEL [1:0]			[3:2]	0h	TOUT2 pin setting 0h: Low fixed 3h: Pulse output
TRIG_TOUT1_SEL [3:0]		3Ah (343Ah)	[3:0]	0h	TOUT1 pin output selection 0h: Low fixed 1h: Pulse1 output
TRIG_TOUT2_SEL [3:0]			[7:4]	0h	TOUT2 pin output selection 0h: Low fixed 2h: Pulse2 output
PULSE1_EN_NOR		78h (3478h)	[0]	0	Pulse1 enable in normal mode 0: disable 1: enable
PULSE1_EN_TRIG			[1]	0	Pulse1 enable in trigger mode 0: disable 1: enable
PULSE1_POL			[2]	0	Pulse1 polarity selection 0: High active 1: Low active
PULSE1_UP [23:0]		79h (3479h)	[7:0]	000000h	Pulse1 active period start timing setting Designated in line units from reference point
		7Ah (347Ah)	[7:0]		
		7Bh (347Bh)	[7:0]		
PULSE1_DN [23:0]		7Ch (347Ch)	[7:0]	000000h	Pulse1 active period end timing setting Designated in line units from reference point
		7Dh (347Dh)	[7:0]		
		7Eh (347Eh)	[7:0]		
PULSE2_EN_NOR		80h (3480h)	[0]	0	Pulse2 enable in normal mode 0: disable 1: enable
PULSE2_EN_TRIG			[1]	0	Pulse2 enable in trigger mode 0: disable 1: enable
PULSE2_POL			[2]	0	Pulse2 polarity selection 0: High active 1: Low active
			[5]	0	Fixed to 1
PULSE2_UP [23:0]		81h (3481h)	[7:0]	000000h	Pulse2 active period start timing setting Designated in line units from reference point
		82h (3482h)	[7:0]		
		83h (3483h)	[7:0]		
PULSE2_DN [23:0]		84h (3484h)	[7:0]	000000h	Pulse2 active period end timing setting Designated in line units from reference point
		85h (3485h)	[7:0]		
		86h (3486h)	[7:0]		

List of Reference Point

	Normal mode	Trigger mode
Reference point of Pulse1	XVS fall edge in N frame	Fall edge of input trigger
Reference point of Pulse2	XVS fall edge in N +1 frame	Rise edge of input trigger

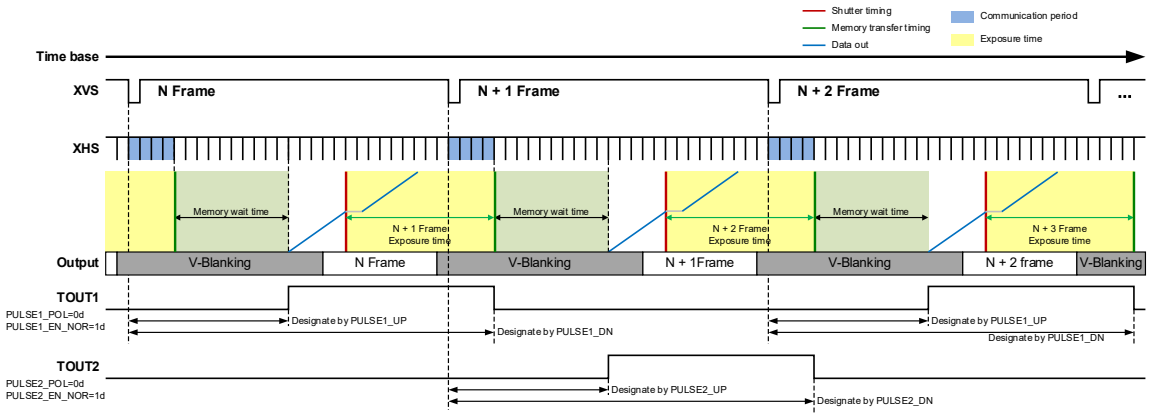


Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

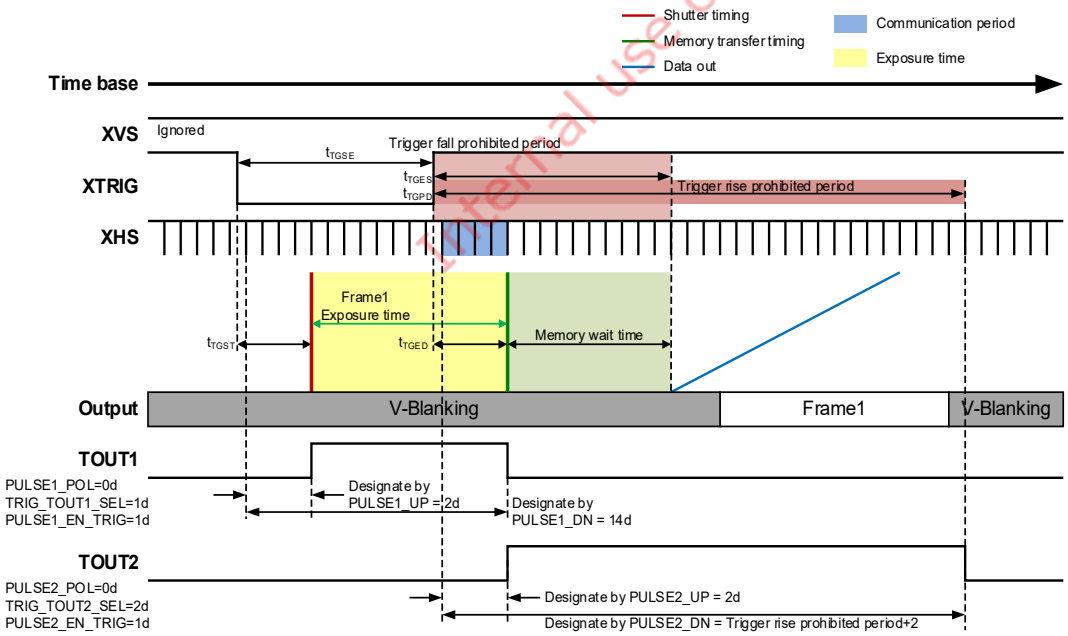


Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

Signal Output

Output Pin Settings

This sensor supports SLVS (4 ch / 8 ch switching) output and SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane) output. In addition, the data rate per channel / Lane is adjustable. The table below shows the output format settings. Set SLVS - EC via standby state.

Register List of Output Settings

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I²C	bit		
FREQ [1:0]	02h	DCh (30DCh)	[1:0]	0h	Frame rate adjust
FREQ_SYNC [7:0]	04h	26h (3226h)	[7:0]	83h	Refer to the register list in each Readout mode
STBSLVS [3:0]	06h	44h (3444h)	[3:0]	1h	The un-using SLVS channel go into standby
OPORTSEL [3:0]		45h (3445h)	[3:0]	1h	SLVS Output channel selection (Refer the list of output pins below)
LANESEL [2:0]	0Bh	04h (3904h)	[2:0]	0h	SLVS - EC Output Lane selection (Refer the list of output pins below)

Output Pins

Output pins	SLVS output		SLVS - EC output			
	4 ch	8 ch	1 Lane	2 Lane	4 Lane	8 Lane
DOP0 / DOM0	Hi-Z	Ch 7	Lane 1	Lane 1	Lane 1	Lane 1
DOP1 / DOM1	Hi-Z	Ch 5	Hi-Z	Lane 2	Lane 2	Lane 2
DOP2 / DOM2	Ch 3	Ch 3	Hi-Z	Hi-Z	Lane 3	Lane 3
DOP3 / DOM3	Ch 1	Ch 1	Hi-Z	Hi-Z	Lane 4	Lane 4
DOP4 / DOM4	Ch 2	Ch 2	Hi-Z	Hi-Z	Hi-Z	Lane 5
DOP5 / DOM5	Ch 4	Ch 4	Hi-Z	Hi-Z	Hi-Z	Lane 6
DOP6 / DOM6	Hi-Z	Ch 6	Hi-Z	Hi-Z	Hi-Z	Lane 7
DOP7 / DOM7	Hi-Z	Ch 8	Hi-Z	Hi-Z	Hi-Z	Lane 8
DCKP / DCKM	DCK	DCK	Hi-Z	Hi-Z	Hi-Z	Hi-Z

SLVS 4 ch / 8 ch output format is shown in the figure below.

When setting 4 ch, after four data of SAV is output in the order of CH1 to CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH4 respectively.

When setting 8 ch, after four data of SAV is output in the order of CH1 to CH8 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH8 respectively.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Readout Drive Mode".

Output Format of SLVS 4 ch / 8 ch

SLVS - EC 1 Lane / 2 Lane / 4 Lane / 8 Lane output format, see each drive timing chart in the section of "Readout Drive Mode".

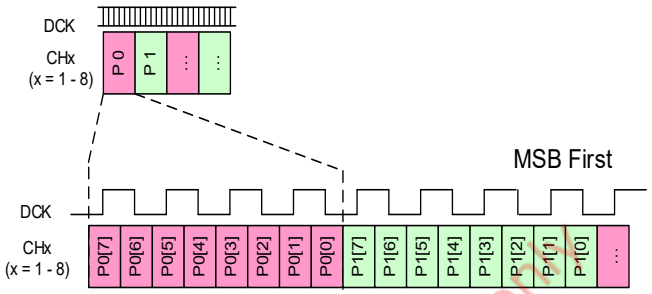
Output Pin Bit Width Selection

The output pin width can be selected from 8-bit, 10-bit or 12-bit output using register ADBIT, ODBIT. Sync code is output according to bit width setting of these register.

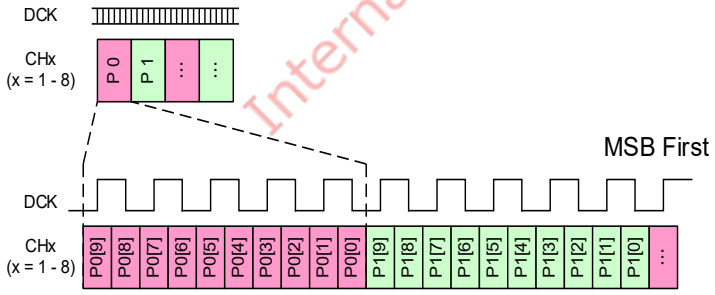
Register List of Bit Width Selection

Register	Register details			Initial value	Setting value	Remarks
	Chip ID	Address ( ): I²C	bit			
ADBIT	04h	00h (3200h)	[6:5]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	Set same value to both ADBIT and ODBIT
ODBIT	06h	30h (3430h)	[1:0]	0h	0h: 10 bit 1h: 12 bit 2h: 8 bit	

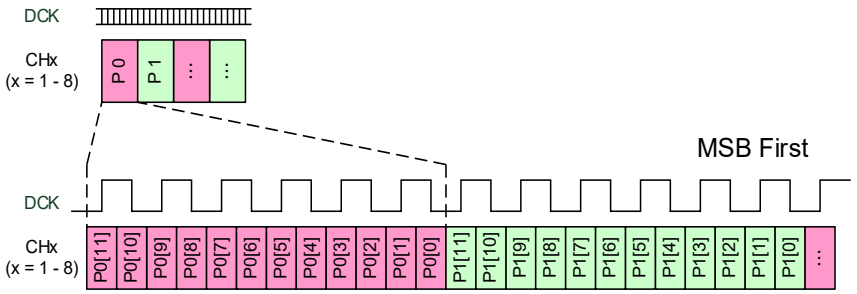
When SLVS output



Example of Data format in SLVS 8-bit output

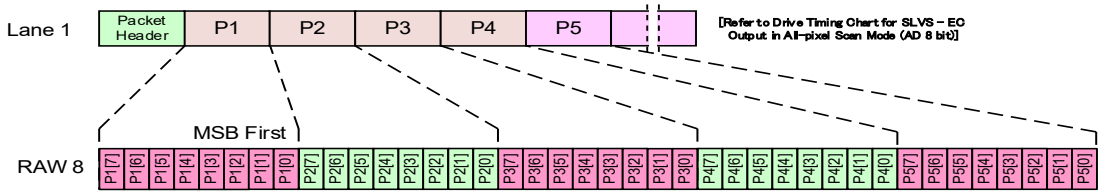


Example of Data format in SLVS 10-bit output

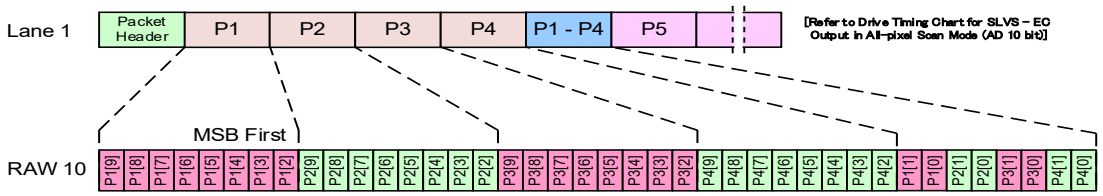


Example of Data format in SLVS 12-bit output

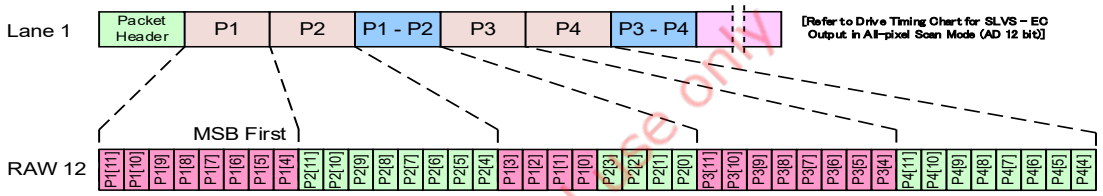
When SLVS - EC output



Example of Data format in SLVS - EC 8-bit output



Example of Data format in SLVS - EC 10-bit output



Example of Data format in SLVS - EC 12-bit output

Output Signal Range

The sensor output has either a 8-bit or 10-bit or 12-bit gradation, but SLVS output is not performed over the full range, and the maximum output value is the “FFh – 1” (8-bit output), the “3FFh - 1” (10-bit output) and the “FFFh - 1” (12-bit output). The minimum value is 001h. The output range for each output gradation is shown in the table below. The maximum level and the minimum level are output only in the sync code. See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes. SLVS - EC output can output with full range.

Output Gradation and Output Range (When SLVS output)

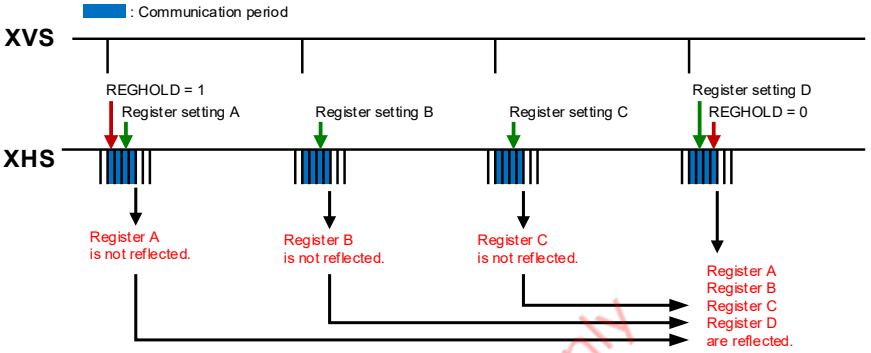
Output gradation	Output value	
	Min.	Max.
8 bit	01h	FEh
10 bit	001h	3FEh
12 bit	001h	FFEh

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

Register	Register details			Initial value	Setting value
	Chip ID	Address ( ): I^2C	bit		
REGHOLD	02h	34h (3034h)	[0]	0h	0h: Invalid 1h: Valid (Register hold)



Register Hold Setting

Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
ROI	→	All - pixel	Via the Standby state is unnecessary
All - pixel	→	ROI	
- Transition between modes other than the above - Change the input frequency of INCK[*1] - Change the register setting noted “S” in the reflection timing column of the Register Map			Via the standby state is necessary[*2]

[*1] When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

[*2] When changing the number of Lane of SLVS - EC, after setting Standby, perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Other Function

This sensor has the function as below. About detail, refer to each application note.

- Multi Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger mode
- Multi Frame ROI (Multi Exposure + ROI) mode
- Driving Low Power Consumption at longtime exposure
- Simple Thermometer
- Gradation Compression
- Dual ADC
- Dual Trigger
- Self Trigger
- Pattern Generator (Refer to Support Package)

Extension Function

Use these function after enough checks and evaluation.

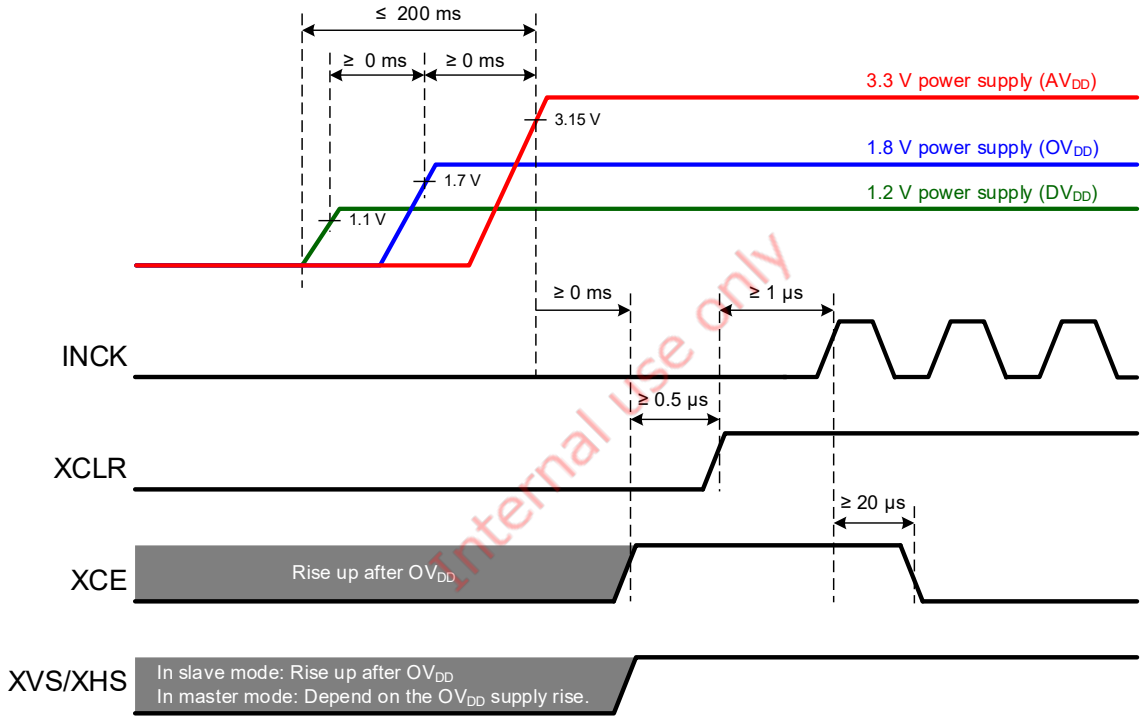
- Black Level Auto Adjust Off
- Short Exposure Mode

Power-on and Power-off Sequence

Power-on sequence

Follow the sequence below to turn On the power supplies.

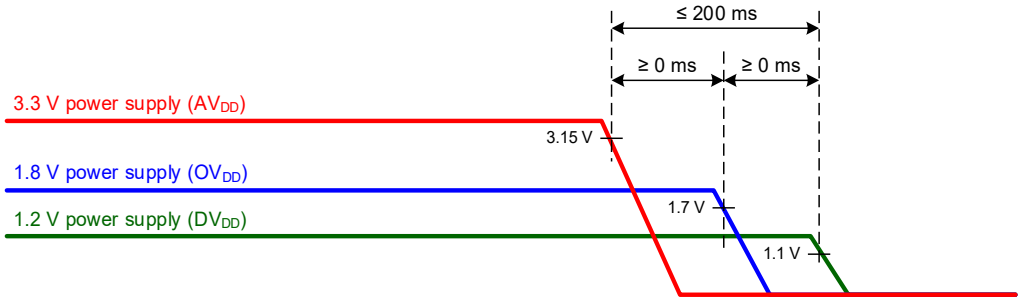
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms. Each digital input terminal (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE, OMODE and XVS, XHS) set 0V or Hi - Z.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after stabilizing the master clock (INCK).



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG1, XTRIG2, SLAMODE, OMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

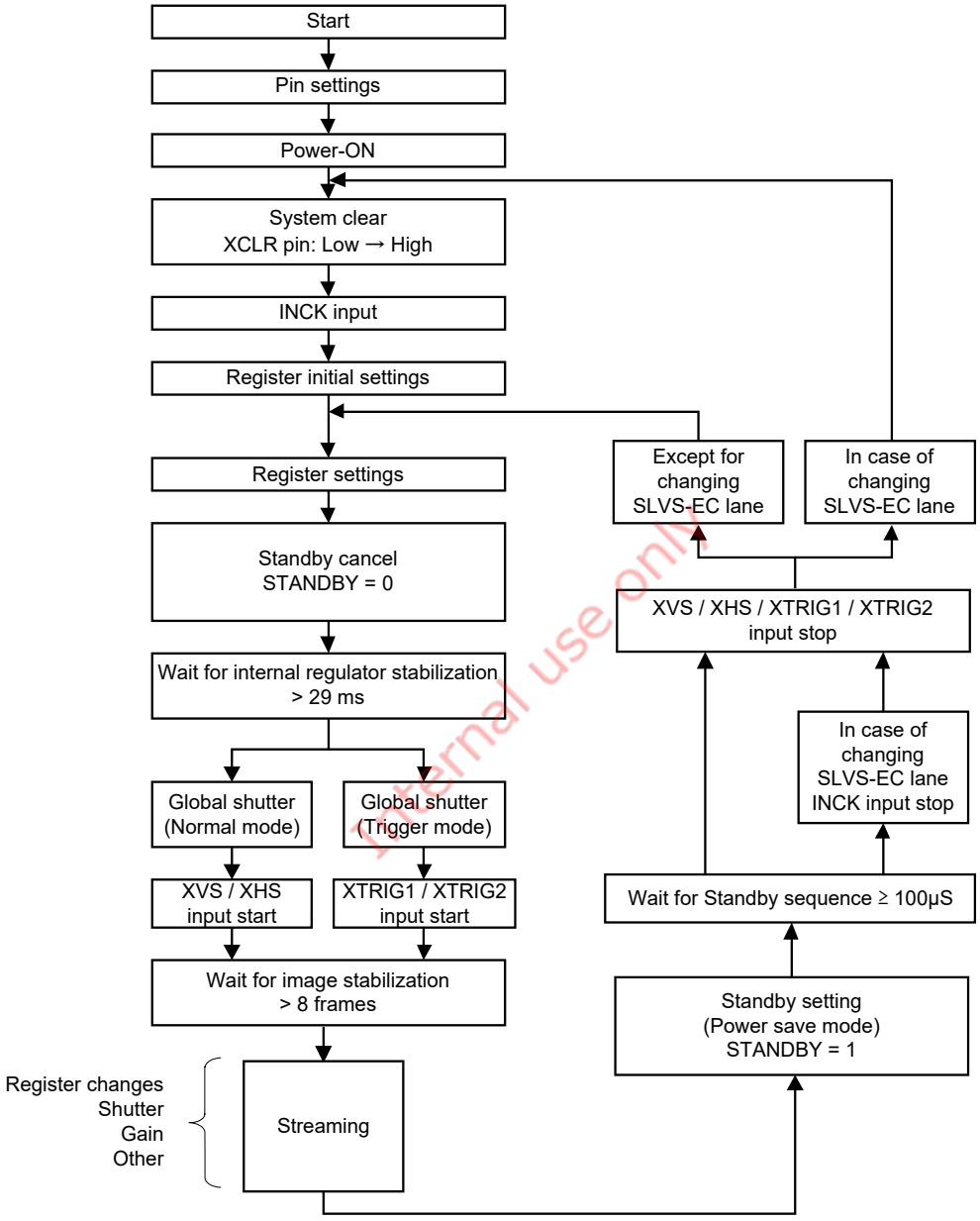


Power-off Sequence

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

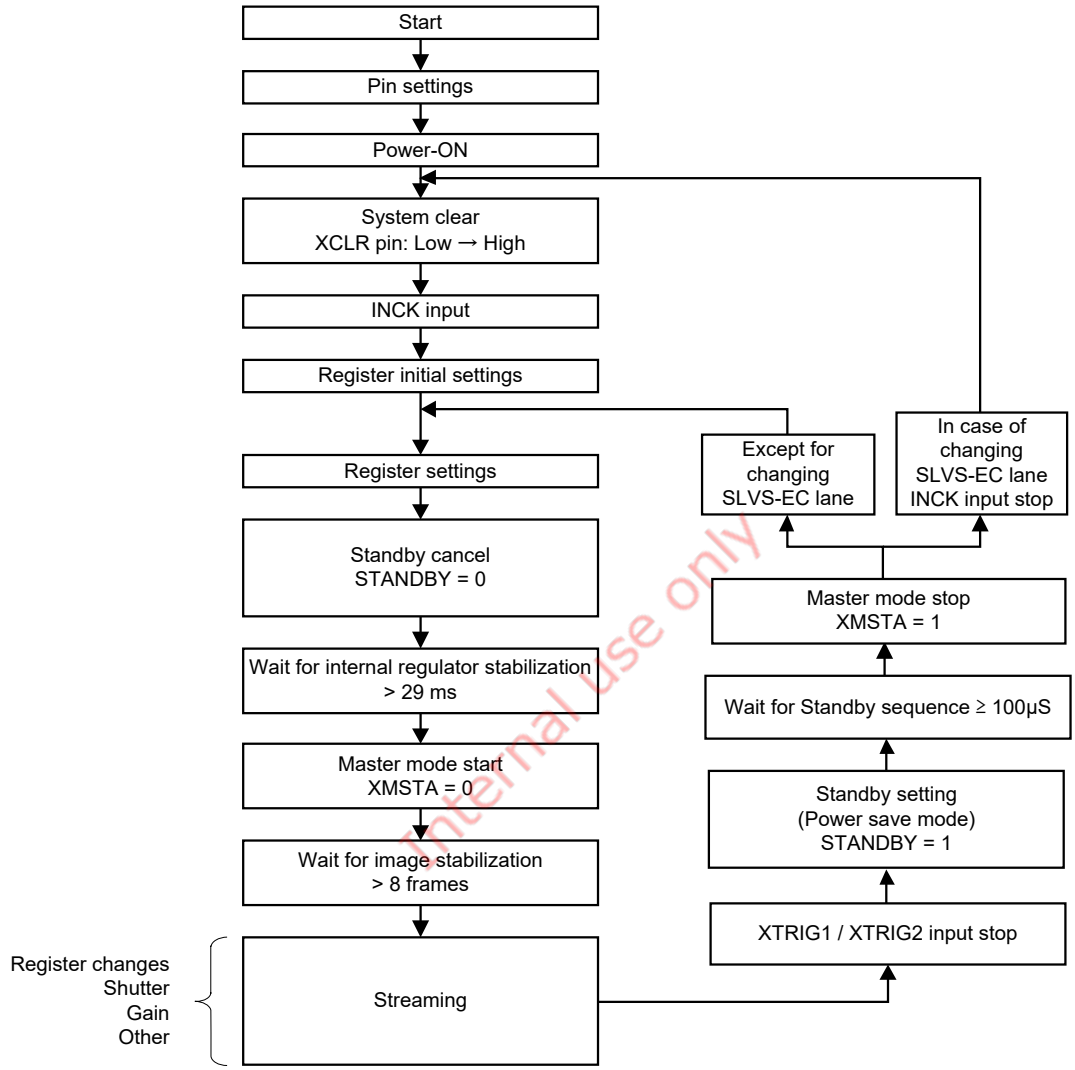
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". “Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Setting Flow in Sensor Master Mode

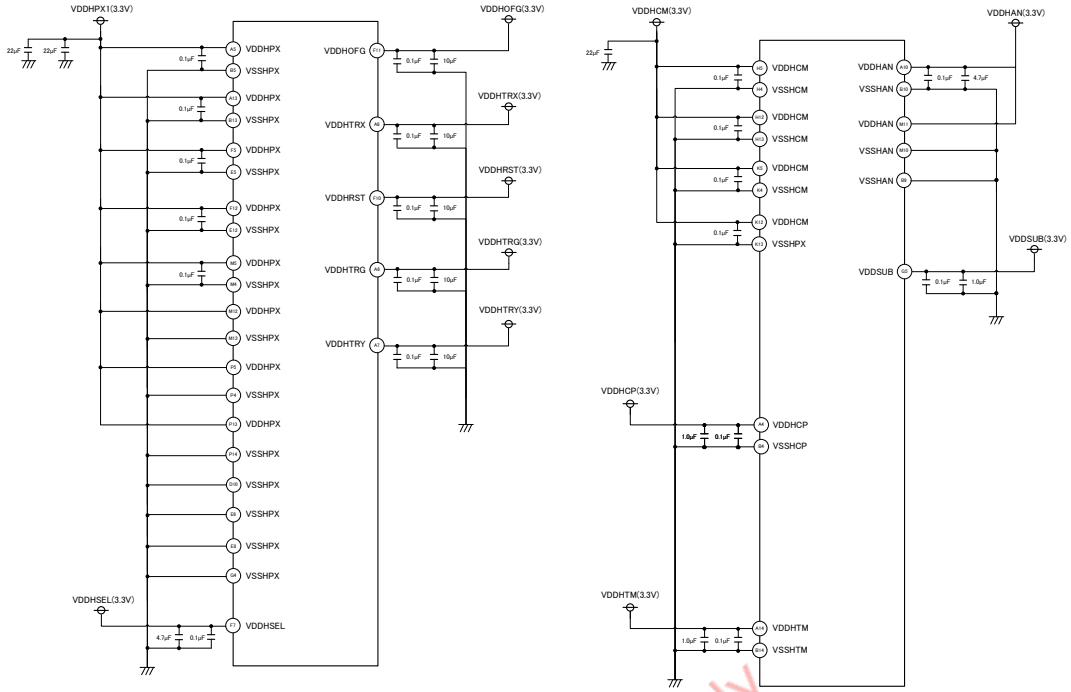
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

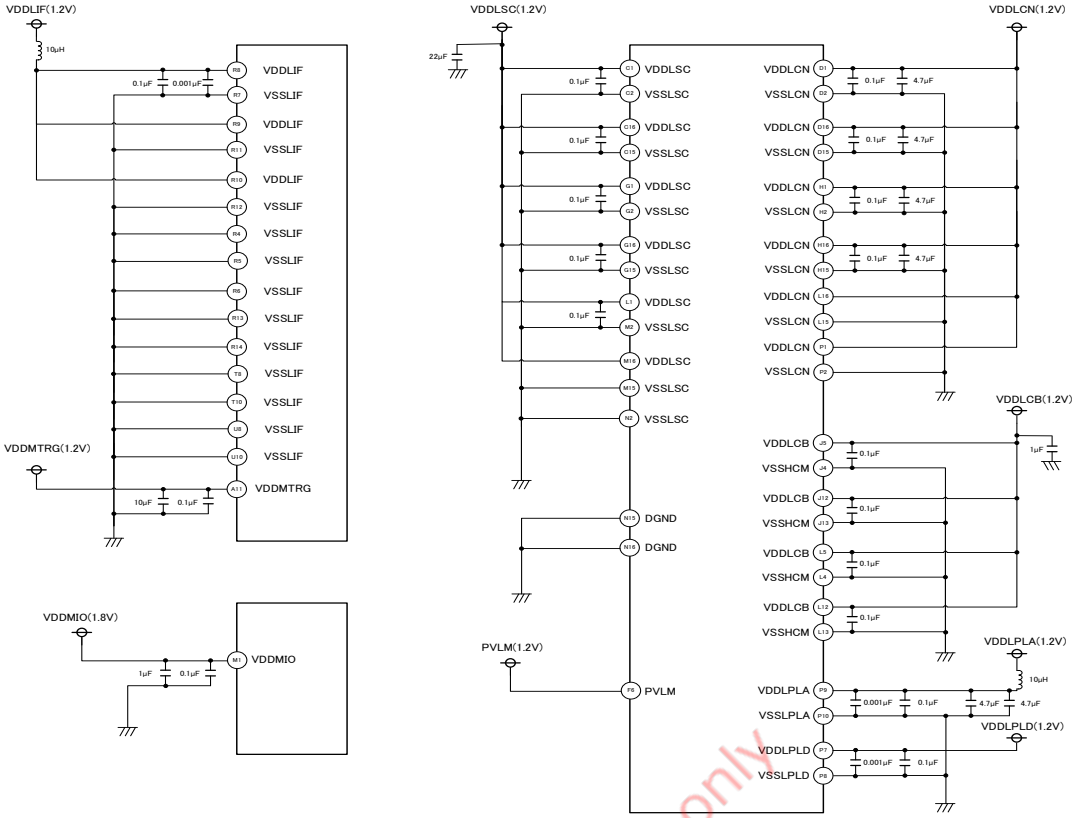
Peripheral Circuit

Analog Power Pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

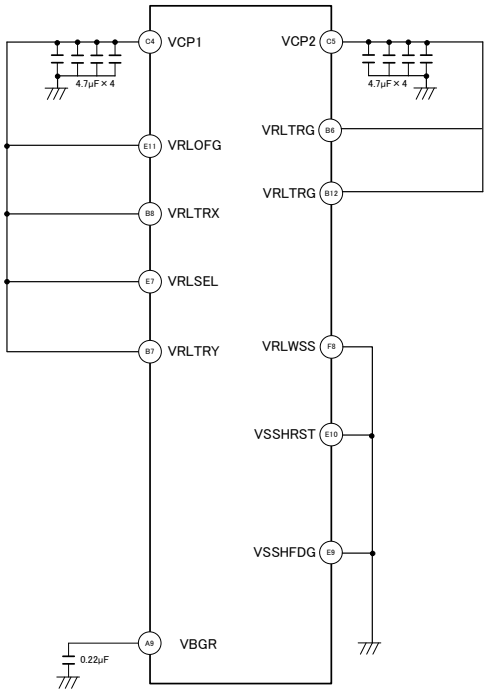
Digital Power Pins



Pin J5, J12, L5, and L12 are analog power pins. But these pins can be connected to the digital power pins. So, it describe on this page. These pins can be separated from the digital power pins.

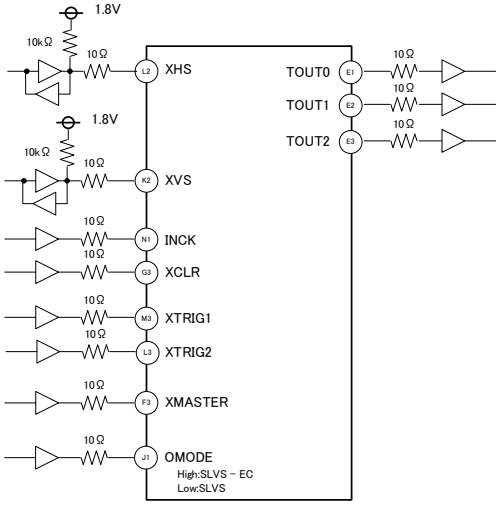
Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

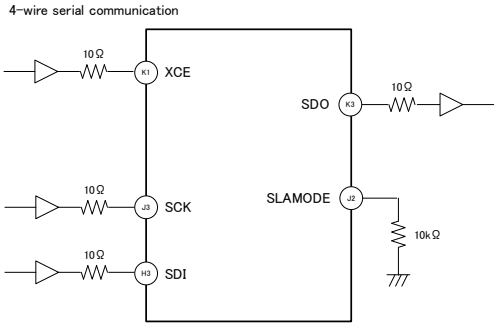
Analog Other Pins

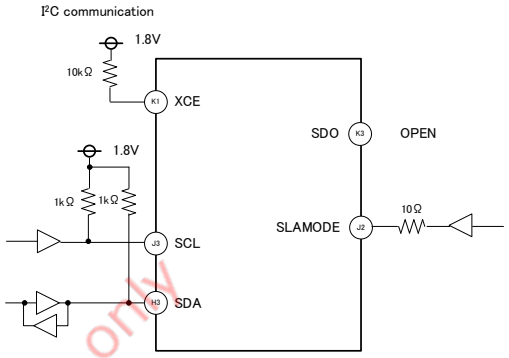


Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Digital I/O Pins

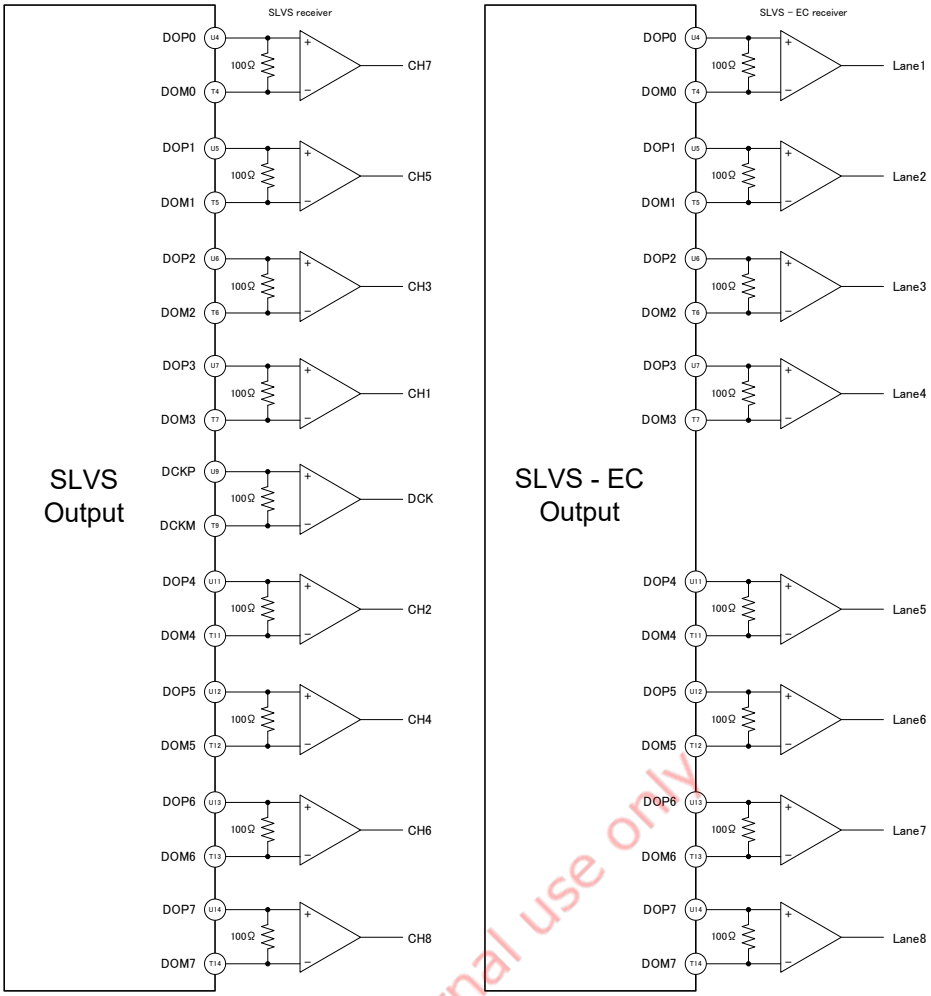






Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Output pins



Application circuits shown are typical examples illustrating the operation of the devices. Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

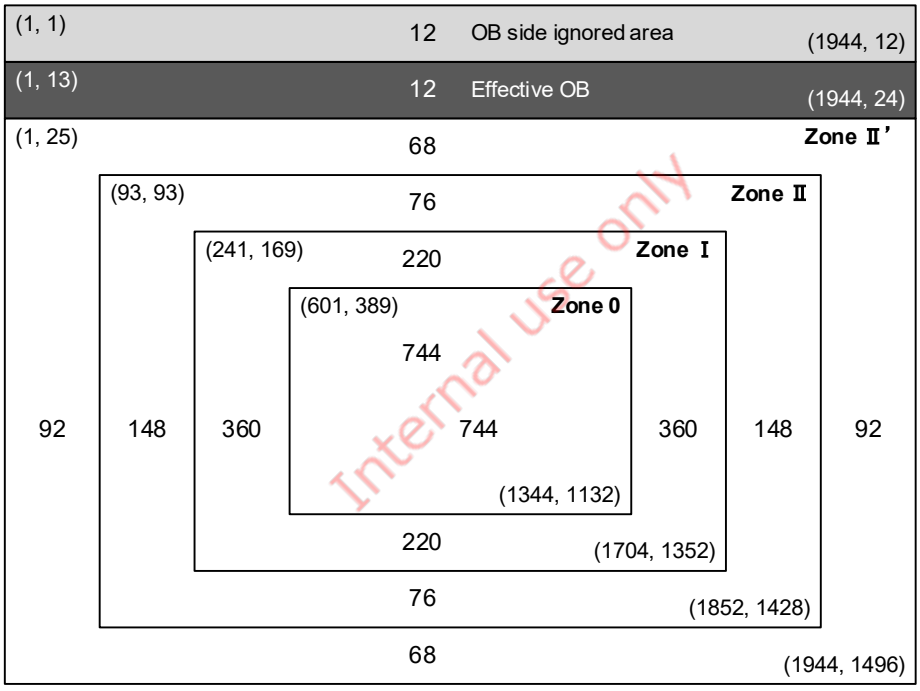
Spot Pixel Specifications

(Tj = 60 ˚C)

Type of distortion	Level	Maximum distorted pixels in each zone			Measurement method	Remarks
		0 to II'	Effective OB	Ineffective OB		
Black and white pixels at high light	30 % ≤ D	22	No evaluation criteria applied		1	
White pixels in the dark	5.6 mV ≤ D	532		No evaluation criteria applied	2	1/30 s storage
Black pixels at signal saturated	D ≤ 800 mV	0	No evaluation criteria applied		3	

Note) 1. Zone is specified based on all - pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Sport Pixel Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	13 pcs
10.0 mV or higher	9 pcs
24.0 mV or higher	5 pcs
50.0 mV or higher	3 pcs
72.0 mV or higher	2 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

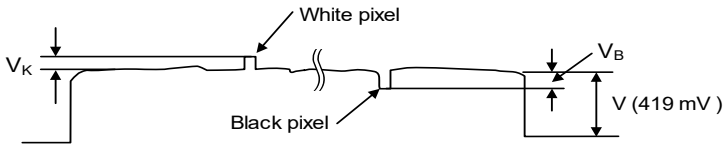
Material_No.03-0.0.10

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value V of the signal outputs is 419 mV, measure the local dip point (black pixel at high light, V_B) and peak point (white pixel at high light, V_K) in the signal output V, and substitute the value into the following formula.

   Spot pixel level D = ((V_B or V_K) / Average value of V) × 100 [%]



Signal output waveform

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

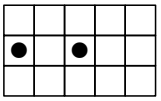
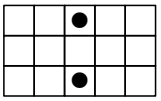
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

Signal output waveform

Spot Pixel Pattern Specification

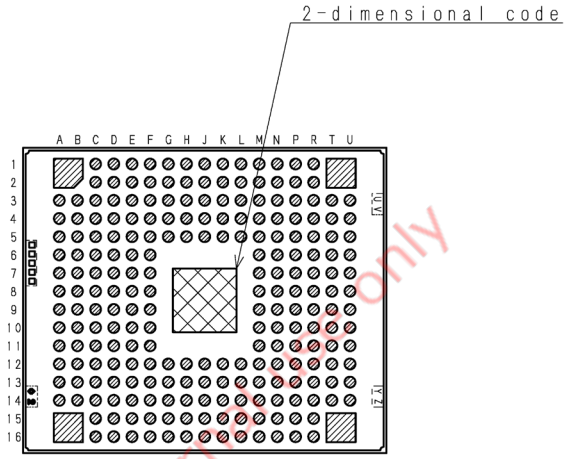
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern	Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1. “● ” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. In case of White Pixel, it is rejected in two or more.
4. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Note:Following characters enter into "Y", and "Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-B421LLJ(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

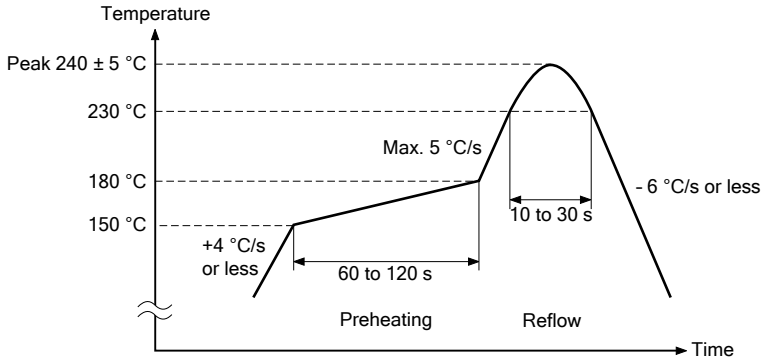
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.
(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

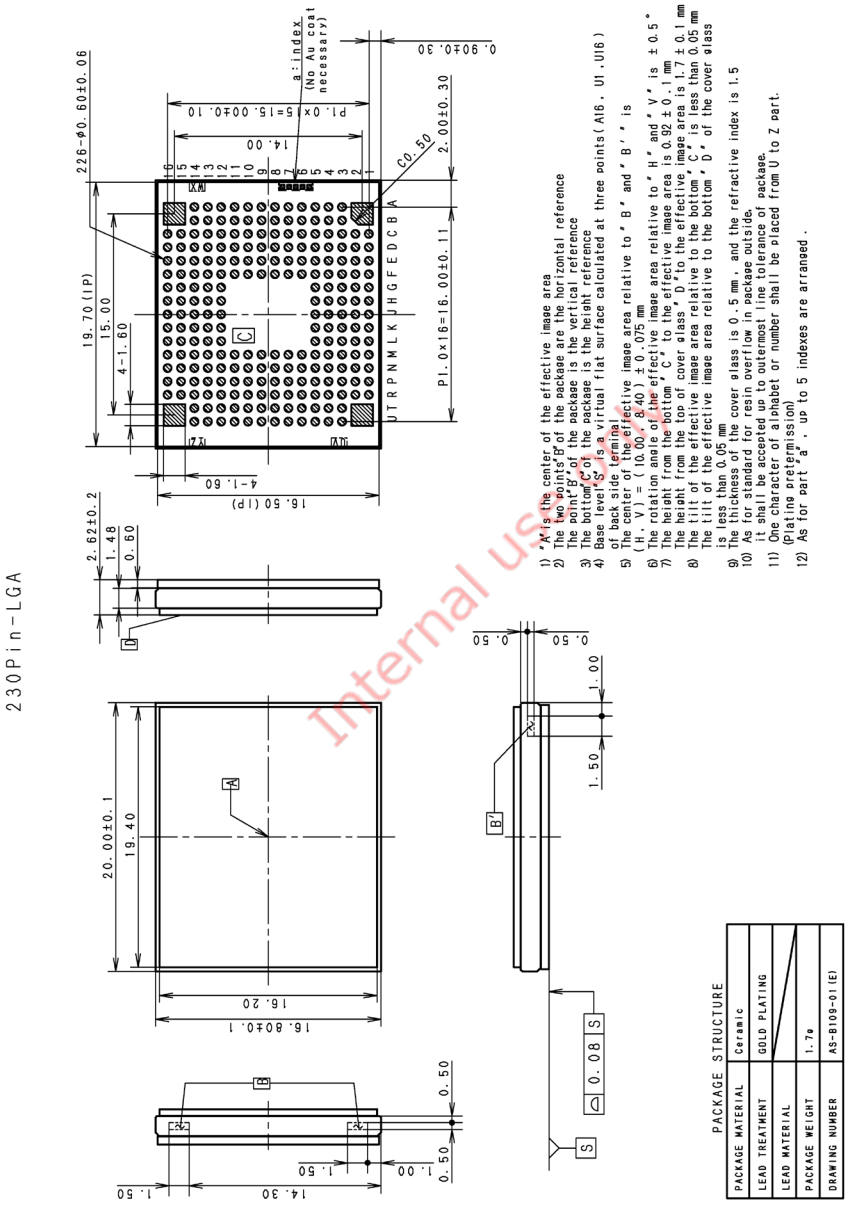
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.8

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

Pregius

* Pregius is a registered trademark or trademark of Sony Group Corporation or its affiliates. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony's low-noise CCD structure, and realizes high picture quality.

Revision History

Date of change	Revision	Page	Contain of Change
21 - Apr - 17	0.1	-	First edition
25 - Sep - 17	0.2	2	Correction: The number of pixels and Type in Image size
		12	Correction: Description of Pin No. E11 (VCP2 →VCP1) Description of Pin No. H12 (1.2V →3.3V)
		13	Correction: Description of Pin No. K5 (1.2V →3.3V)
		43	Correction: Address =00h default value of register
		63	Correction: The figure of SLVS - EC Frame Format (Normal frame)
		64	Correction: The figure of SLVS - EC Frame Format (Standby mode)
		69	Correction: Clock name in figure : DLCK → DCK
		67, 70, 75, 81, 87, 96, 98, 100, 102	Added: CID=04h Address=31h
		73	Correction: Drive Timing Chart (All - pixel Scan Mode)
		76	Correction: The number of pixels in the figure
		77	Correction: Clock name in figure : DLCK → DCK
		79, 80, 85, 86	Correction: The register address of ROI
		88	Correction: Restrictions on ROI mode : 1972 → 1472
		89	Correction: Formula of 1 Frame in the figure
		89, 90, 91	Correction: Drive Timing Chart (ROI Mode)
		93, 95	Correction: Description of “Frame rate on ROI mode”
		101, 103	Correction: Vertical blanking period
		111, 112, 114, 116	Update: The value of toffset
		111	Update: Exposure setting list
		113, 115	Correction: In description, XTRIG → XTIRG1 Added: In description, XTRIG2 pin is set Open (Hi-Z) or fixed to High after power-on sequence
		114	Correction: The figure of Interrupt Operation
		117	Correction: Trigger input prohibited period : 20H → GTWAIT (H)
		121	Correction: DCK1 → DCK in Output Format
		126	Added: *2 Note of changing the number of SLVS - EC Lane
		130, 131	Added: Figure of changing the number of SLVS - EC Lane
		132	Correction: VSSHPX which is paired with F5 pin: E6 → E5
		137	Update: Zone Definition
20 - Nov - 17	0.3	18	Added: Note of SLVS - EC
		23	Deleted: "Skew between the lane" on the table
		37	Added: I^2C communication Write operation
		67	Correction: bit length and Initial value of SYNCCODE_LEN
		74	Correction: 12bit Drive Timing Chart (All - pixel)
		76	Correction: 8bit Drive Timing Chart (All - pixel)
		81, 87	Correction: CID=03h Address=04h, 05h
		91	Correction: 12bit Drive Timing Chart (ROI)
		93	Correction: 8bit Drive Timing Chart (ROI)
		113	Update: Exposure setting list
		112, 113, 115, 117	Update: The value of toffset
		117	Correction: The value of tTGDLY on parameter list
		130	Correction: Description of Power-on sequence 4

Date of change	Revision	Page	Contain of Change
09 - Feb - 18	0.4	8, 17, 22, 25, 26, 28, 112, 113, 115, 117, 139, 140, 141	Update: TBD
		26	Correction: Description of Remarks (Dark signal, Dark signal shading)
		58, 59, 60, 61, 70, 73, 78, 80, 86, 94, 96, 99, 101, 103, 105	Correction: H of Total number of pixels Added: Note that the number is average
		69, 72, 77, 83, 89, 98, 100, 102, 104	Correction: The setting value of CID=04h Address=30h/31h
		77	Correction: Setting value of FREQ_SYNC
		80	Correction: Vertical value in the figure
		91, 92, 93	Correction: Drive Timing Chart (ROI Mode)
		95	Correction: Initial value of VOPB_VBLK_HWIDTH
		106	Correction: Regulator stabilization period
		115	Correction: The value of tTGDLY on parameter list (1080p – Full HD)
		117	Correction: The value of tTGPD on parameter list
		122	Added: Description of setting SLVS - EC to fit Sensor Setting Flow
		125	Correction: Data format figure in SLVS - EC output
		132, 133	Added: State to stop INCK at changing the SLVS - EC lane
		139	Update: Zone Definition
		142	Deleted: White pixel of Spot Pixel Pattern Added: Note 3
17 - Apr - 18	0.5	46	Correction: Register of CID=04h Address=32h bit=1
11 - Jun - 18	E18613	-	First Edition (Official Version)
		44	Correction: Reflection timing of CID=04h Address=04h
		50	Correction: Reflection timing of CID=07h Address=C0h/C1h
		57	Correction: Frame rate of Vertical / Horizontal 1/2 Subsampling mode Total average number of pixels (Average) of HD 1080p
		59	Correction: Frame rate of Vertical / Horizontal 1/2 Subsampling mode
		97	Correction: Setting value of VMAX of Vertical / Horizontal 1/2 Subsampling mode
		133	Correction: VSSHCP which is paired with A4 pin: B5 => B4
		142, 145	Update: TBD
26 - Jul - 18	E18613A87	55, 56	Correction: I^2C Address from CID=10h to 19h
		97	Correction: Frame rate
		143, 144	Update: Notes On Handling
25 - Feb - 19	E18613B92	76	Correction: Register List of 1080p - Full HD mode (Chip ID = 04, address = 25h)
7 - Aug - 19	E18613C98	32	Correction: prohibited period
		44	Correction: Spelling of H binning CLIP of HADD_ON_SEL
		46	Correction: Reflection timing for TRIGEN
		73 to 75, 84, 90 to 92	Correction: The figure of Drive Timing Chart
		100, 104	Delete: Unnecessary ruled line
		108	Correction: offset variable range of BLKLEVEL
6 - Aug - 21	E18613D18	145	Correction: Package Outline
		146	Correction: List of Trademark Logos and Definition Statements