SONY

Diagonal 8.9 mm (Type 1/1.8) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

# Preliminary

# IMX252LLR-C

Pregius

For the latest data sheet, please visit www.sunnywale.com

## Description

The IMX252LLR-C is a diagonal 8.9mm (Type 1/1.8) CMOS active pixel type solid-state image sensor with a square pixel array and 3.19 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: FA cameras, ITS cameras)

## Features

◆ CMOS active pixel type dots

◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit

◆ Global shutter function

◆ Input frequency
37.125 MHz / 74.25 MHz / 54MHz

◆ Number of recommended recording pixels: 2048 (H) × 1536 (V) approx. 3.15 M pixels
Readout mode
All-pixel scan mode
1080p-Full HD readout mode
Vertical / Horizontal 1 / 2 Subsampling mode
Vertical 2-pixel FD Binning mode
ROI mode
Vertical / Horizontal - Normal / Inverted readout mode

◆ Readout rate
Maximum frame rate in
All-pixel scan mode: 8 bit 216.2 frame/s, 10 bit:191.5 frame/s, 12 bit:118.5 frame/s

◆ Variable-speed shutter function (resolution 1 H units)

◆ 8-bit / 10-bit / 12-bit A/D converter

◆ CDS / PGA function
0 dB to 24 dB: Analog Gain (0.1 dB step)
24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)

◆ I/O interface
Low voltage LVDS (150 mVp-p) serial (4 ch / 8 ch / 16ch switching) DDR output

◆ Recommended lens F number: 2.8 or more (Close side)

◆ Recommended exit pupil distance: –100 mm to –∞

*There is a possible to change the registers on this document.

Exmor

## Device Structure

◆ CMOS image sensor

◆ Image size
Diagonal 8.9 mm (Type 1/1.8) Approx. 3.19 M pixels All-pixel
Diagonal 7.7 mm (Type 1/2.35) Approx. 2.11 M pixels 1080p-Full HD

◆ Total number of pixels
2064 (H) × 1554 (V) Approx. 3.21 M pixels

◆ Number of effective pixels
2064 (H) × 1544 (V) Approx. 3.19 M pixels

◆ Number of active pixels
2064 (H) × 1544 (V) Approx. 3.19 M pixels

◆ Number of recommended recording pixels
2048 (H) × 1536 (V) Approx. 3.15 M pixels All-pixel
1920 (H) × 1080 (V) Approx. 2.07 M pixels 1080p-Full HD

◆ Unit cell size
3.45 µm (H) × 3.45 µm (V)

◆ Optical black
Horizontal (H) direction: Front 0 pixels, rear 0 pixels
Vertical (V) direction: Front 10 pixels, rear 0 pixels

◆ Substrate material
Silicon

## Absolute Maximum Ratings

| Item | Symbol | Rating | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| Supply voltage (Analog 3.3 V) | $AV_{DD}$ | –0.3 | to | +4.0 | V | |
| Supply voltage (Interface 1.8 V) | $OV_{DD}$ | –0.3 | to | +3.3 | V | |
| Supply voltage (Digital 1.2 V) | $DV_{DD}$ | –0.3 | to | +2.0 | V | |
| Input voltage | VI | –0.3 | to | $OV_{DD}$ +0.3 | V | Not exceed 3.3 V |
| Output voltage | VO | –0.3 | to | $OV_{DD}$ +0.3 | V | Not exceed 3.3 V |
| Operating temperature | Topr | -30 | to | +75 | ˚C | |
| Storage temperature | Tstg | -40 | to | +85 | ˚C | |
| Performance guarantee temperature | Tspec | -10 | to | +60 | ˚C | |

## Recommended Operating Conditions

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage (Analog 3.3 V) | $AV_{DD}$ | 3.15 | 3.30 | 3.45 | V |
| Supply voltage (Interface 1.8 V) | $OV_{DD}$ | 1.70 | 1.80 | 1.90 | V |
| Supply voltage (Digital 1.2 V) | $DV_{DD}$ | 1.10 | 1.20 | 1.30 | V |

## USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

**Use Restrictions**

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

**Design for Safety**

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

**Export Control**

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

**No License Implied**

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

**Governing Law**

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

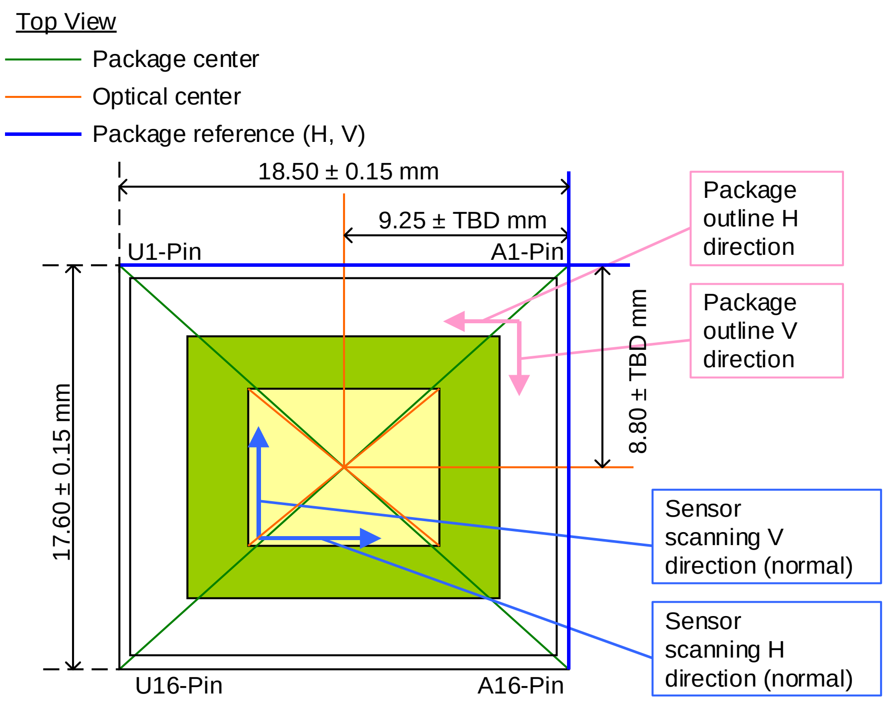
**Other Applicable Terms and Conditions**

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

General-0.0.8

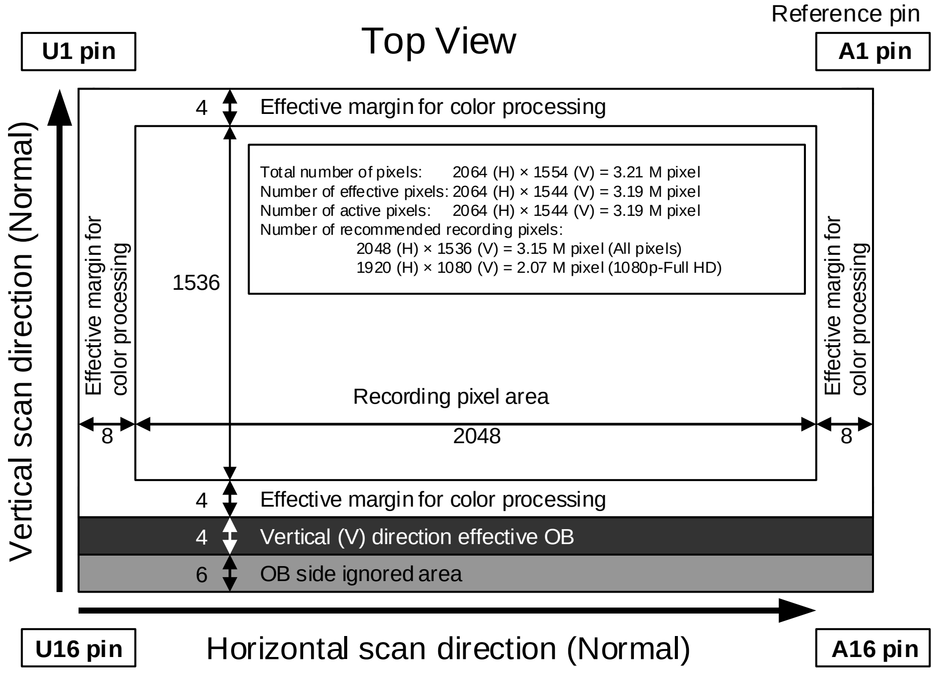
## CONTENTS

## Chip Center and Optical Center




Optical Center

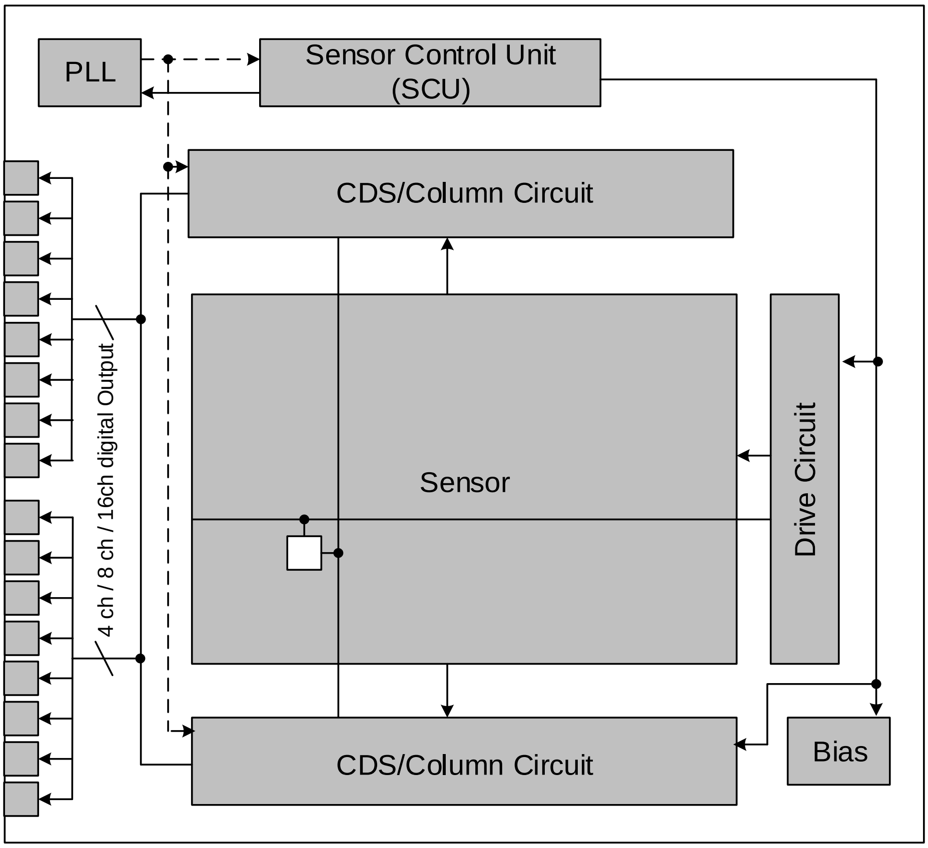
## Pixel Arrangement



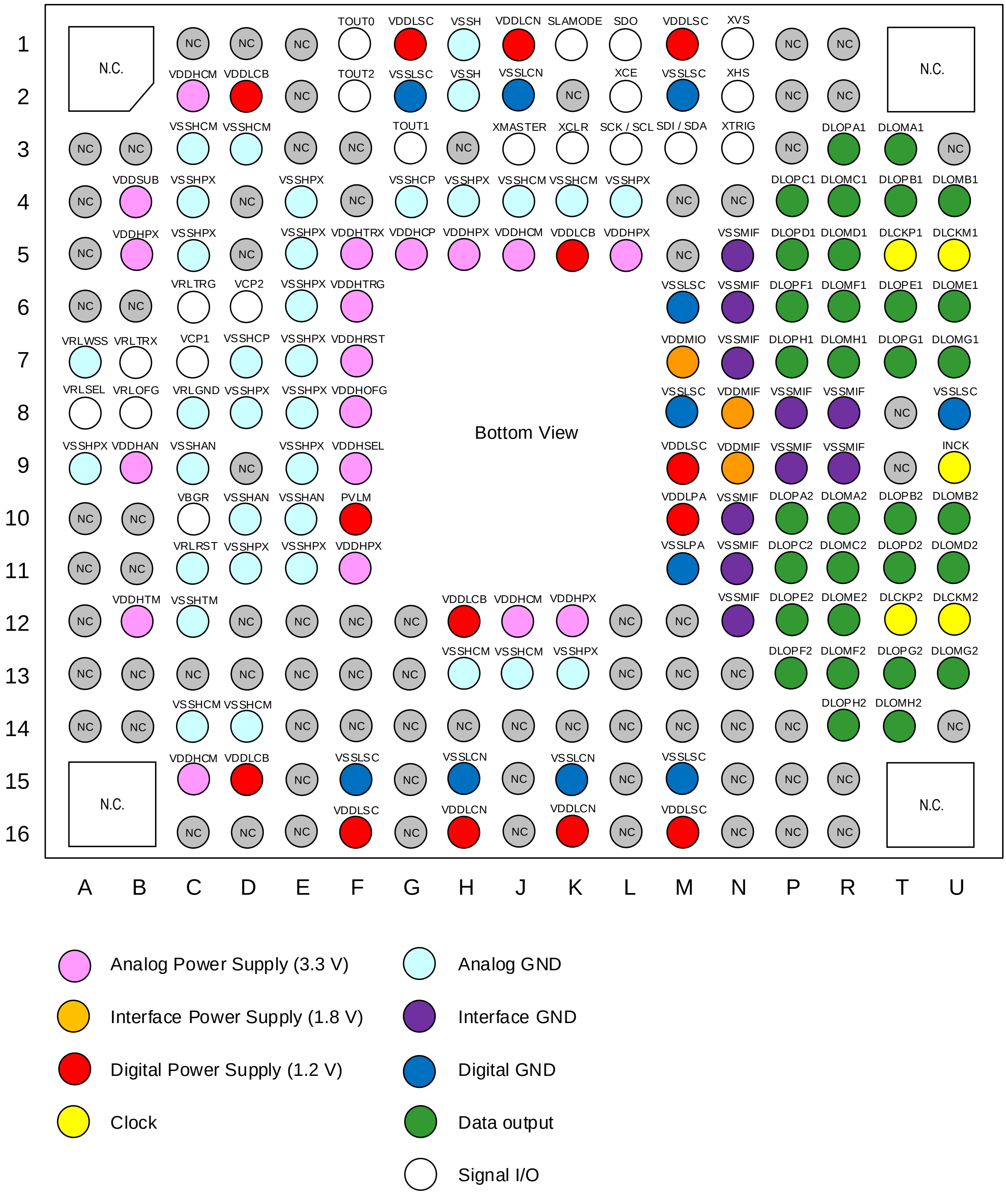

Pixel Arrangement

## Block Diagram and Pin Configuration

(Top View)




Block Diagram




Pin Configuration

## Pin Description

| No. | Pin No. | I/O | Analog / Digital | Symbol | Description |
|---|---|---|---|---|---|
| 1 | A1 | — | — | N.C | — |
| 2 | A3 | — | — | N.C | — |
| 3 | A4 | — | — | N.C | — |
| 4 | A5 | — | — | N.C | — |
| 5 | A6 | — | — | N.C | — |
| 6 | A7 | GND | A | VRLWSS | 3.3V GND |
| 7 | A8 | I | A | VRLSEL | Connect to VCP1 |
| 8 | A9 | GND | A | VSSHPX | 3.3V GND |
| 9 | A10 | — | — | N.C | — |
| 10 | A11 | — | — | N.C | — |
| 11 | A12 | — | — | N.C | — |
| 12 | A13 | — | — | N.C | — |
| 13 | A14 | — | — | N.C | — |
| 14 | A16 | — | — | N.C | — |
| 15 | B3 | — | — | N.C | — |
| 16 | B4 | Power | A | VDDSUB | 3.3V power supply |
| 17 | B5 | Power | A | VDDHPX | 3.3V power supply |
| 18 | B6 | — | — | N.C | — |
| 19 | B7 | I | A | VRLTRX | Connect to VCP1 |
| 20 | B8 | I | A | VRLOFG | Connect to VCP1 |
| 21 | B9 | Power | A | VDDHAN | 3.3V power supply |
| 22 | B10 | — | — | N.C | — |
| 23 | B11 | — | — | N.C | — |
| 24 | B12 | Power | A | VDDHTM | 3.3V power supply |
| 25 | B13 | — | — | N.C | — |
| 26 | B14 | — | — | N.C | — |
| 27 | C1 | — | — | N.C | — |
| 28 | C2 | Power | A | VDDHCM | 3.3V power supply |
| 29 | C3 | GND | A | VSSHCM | 3.3V GND |
| 30 | C4 | GND | A | VSSHPX | 3.3V GND |
| 31 | C5 | GND | A | VSSHPX | 3.3V GND |
| 32 | C6 | I | A | VRLTRG | Connect to VCP2 |
| 33 | C7 | O | A | VCP1 | Connect to VRLSEL, VRLTRX, VRLOFG (Connect to 4.7uF×2 to GND) |
| 34 | C8 | GND | A | VRLGND | 3.3V GND |
| 35 | C9 | GND | A | VSSHAN | 3.3V GND |
| 36 | C10 | O | A | VBGR | Connect to 0.22uF to GND |
| 37 | C11 | GND | A | VRLRST | 3.3V GND |
| 38 | C12 | GND | A | VSSHTM | 3.3V GND |
| 39 | C13 | - | - | N.C. | - |
| 40 | C14 | GND | A | VSSHCM | 3.3V GND |
| 41 | C15 | Power | A | VDDHCM | 3.3V power supply |
| 42 | C16 | - | - | N.C. | - |
| 43 | D1 | - | - | N.C. | - |
| 44 | D2 | Power | A | VDDLCB | 1.2V power supply |
| 45 | D3 | GND | A | VSSHCM | 3.3V GND |
| 46 | D4 | - | - | N.C. | - |
| 47 | D5 | - | - | N.C. | - |
| 48 | D6 | O | A | VCP2 | Connect to VRLTRG (Connect to 4.7uF×2 to GND) |
| 49 | D7 | GND | A | VSSHCP | 3.3V GND |
| 50 | D8 | GND | A | VSSHPX | 3.3V GND |
| 51 | D9 | - | - | N.C. | - |
| 52 | D10 | GND | A | VSSHAN | 3.3V GND |
| 53 | D11 | GND | A | VSSHPX | 3.3V GND |
| 54 | D12 | - | - | N.C. | - |
| 55 | D13 | - | - | N.C. | - |
| 56 | D14 | GND | A | VSSHCM | 3.3V GND |
| 57 | D15 | Power | A | VDDLCB | 1.2V power supply |
| 58 | D16 | - | - | N.C. | - |
| 59 | E1 | - | - | N.C. | - |
| 60 | E2 | - | - | N.C. | - |
| 61 | E3 | - | - | N.C. | - |

| No. | Pin No. | I/O | Analog / Digital | Symbol | Description |
|---|---|---|---|---|---|
| 62 | E4 | GND | A | VSSHPX | 3.3V GND |
| 63 | E5 | GND | A | VSSHPX | 3.3V GND |
| 64 | E6 | GND | A | VSSHPX | 3.3V GND |
| 65 | E7 | GND | A | VSSHPX | 3.3V GND |
| 66 | E8 | GND | A | VSSHPX | 3.3V GND |
| 67 | E9 | GND | A | VSSHPX | 3.3V GND |
| 68 | E10 | GND | A | VSSHAN | 3.3V GND |
| 69 | E11 | GND | A | VSSHPX | 3.3V GND |
| 70 | E12 | - | - | N.C. | - |
| 71 | E13 | - | - | N.C. | - |
| 72 | E14 | - | - | N.C. | - |
| 73 | E15 | - | - | N.C. | - |
| 74 | E16 | - | - | N.C. | - |
| 75 | F1 | O | D | TOUT0 | Pulse0 output pin |
| 76 | F2 | O | D | TOUT2 | Pulse2 output pin |
| 77 | F3 | - | - | N.C. | - |
| 78 | F4 | - | - | N.C. | - |
| 79 | F5 | Power | A | VDDHTRX | 3.3V power supply |
| 80 | F6 | Power | A | VDDHTRG | 3.3V power supply |
| 81 | F7 | Power | A | VDDHRST | 3.3V power supply |
| 82 | F8 | Power | A | VDDHOFG | 3.3V power supply |
| 83 | F9 | Power | A | VDDHSEL | 3.3V power supply |
| 84 | F10 | Power | A | PVLM | 1.2V power supply |
| 85 | F11 | Power | A | VDDHPX | 3.3V power supply |
| 86 | F12 | - | - | N.C. | - |
| 87 | F13 | - | - | N.C. | - |
| 88 | F14 | - | - | N.C. | - |
| 89 | F15 | GND | D | VSSLSC | 1.2V GND |
| 90 | F16 | Power | D | VDDLSC | 1.2V power supply |
| 91 | G1 | Power | D | VDDLSC | 1.2V power supply |
| 92 | G2 | GND | D | VSSLSC | 1.2V GND |
| 93 | G3 | O | D | TOUT1 | Pulse1 output pin |
| 94 | G4 | GND | A | VSSHCP | 3.3V GND |
| 95 | G5 | Power | A | VDDHCP | 3.3V power supply |
| 96 | G12 | - | - | N.C. | - |
| 97 | G13 | - | - | N.C. | - |
| 98 | G14 | - | - | N.C. | - |
| 99 | G15 | - | - | N.C. | - |
| 100 | G16 | - | - | N.C. | - |
| 101 | H1 | GND | D | VSSH | 3.3V GND |
| 102 | H2 | GND | D | VSSH | 3.3V GND |
| 103 | H3 | - | - | N.C. | - |
| 104 | H4 | GND | A | VSSHPX | 3.3V GND |
| 105 | H5 | Power | A | VDDHPX | 3.3V power supply |
| 106 | H12 | Power | A | VDDLCB | 1.2V power supply |
| 107 | H13 | GND | A | VSSHCM | 3.3V GND |
| 108 | H14 | - | - | N.C. | - |
| 109 | H15 | GND | D | VSSLCN | 1.2V GND |
| 110 | H16 | Power | D | VDDLCN | 1.2V power supply |
| 111 | J1 | Power | D | VDDLCN | 1.2V power supply |
| 112 | J2 | GND | D | VSSLCN | 1.2V GND |
| 113 | J3 | I | D | XMASTER | Master / Slave select<br>(Slave Mode : High, Master Mode : Low) |
| 114 | J4 | GND | A | VSSHCM | 3.3V GND |
| 115 | J5 | Power | A | VDDHCM | 3.3V power supply |
| 116 | J12 | Power | A | VDDHCM | 3.3V power supply |
| 117 | J13 | GND | A | VSSHCM | 3.3V GND |
| 118 | J14 | - | - | N.C. | - |
| 119 | J15 | - | - | N.C. | - |
| 120 | J16 | - | - | N.C. | - |
| 121 | K1 | I | D | SLAMODE | Slave address select (1A : High, 10 : Low) |
| 122 | K2 | - | - | N.C. | - |
| 123 | K3 | I | D | XCLR | System clear (Normal : Hight, Clear : Low) |
| 124 | K4 | GND | A | VSSHCM | 3.3V GND |
| 125 | K5 | Power | A | VDDLCB | 1.2V power supply |

| No. | Pin No. | I/O | Analog / Digital | Symbol | Description |
|---|---|---|---|---|---|
| 126 | K12 | Power | A | VDDHPX | 3.3V power supply |
| 127 | K13 | GND | A | VSSHPX | 3.3V GND |
| 128 | K14 | - | - | N.C. | - |
| 129 | K15 | GND | D | VSSLCN | 1.2V GND |
| 130 | K16 | Power | D | VDDLCN | 1.2V power supply |
| 131 | L1 | O | D | SDO | 4-wire : Serial communication I/F SDO pin<br>$I^2C$ : OPEN |
| 132 | L2 | I | D | XCE | 4-wire : Serial communication I/F XCE pin<br>$I^2C$ : Fixed to High |
| 133 | L3 | I | D | SCK / SCL | 4-wire : Serial communication I/F SCK pin<br>$I^2C$ : Serial clock line |
| 134 | L4 | GND | A | VSSHPX | 3.3V GND |
| 135 | L5 | Power | A | VDDHPX | 3.3V power supply |
| 136 | L12 | - | - | N.C. | - |
| 137 | L13 | - | - | N.C. | - |
| 138 | L14 | - | - | N.C. | - |
| 139 | L15 | - | - | N.C. | - |
| 140 | L16 | - | - | N.C. | - |
| 141 | M1 | Power | D | VDDLSC | 1.2V power supply |
| 142 | M2 | GND | D | VSSLSC | 1.2V GND |
| 143 | M3 | I/O | D | SDI / SDA | 4-wire : Serial communication I/F SDI pin<br>$I^2C$ : Serial data line |
| 144 | M4 | - | - | N.C. | - |
| 145 | M5 | - | - | N.C. | - |
| 146 | M6 | GND | D | VSSLSC | 1.2V GND |
| 147 | M7 | Power | D | VDDMIO | 1.8V power supply |
| 148 | M8 | GND | D | VSSLSC | 1.2V GND |
| 149 | M9 | Power | D | VDDLSC | 1.2V power supply |
| 150 | M10 | Power | D | VDDLPA | 1.2V power supply |
| 151 | M11 | GND | D | VSSLPA | 1.2V GND |
| 152 | M12 | - | - | N.C. | - |
| 153 | M13 | - | - | N.C. | - |
| 154 | M14 | - | - | N.C. | - |
| 155 | M15 | GND | D | VSSLSC | 1.2V GND |
| 156 | M16 | Power | D | VDDLSC | 1.2V power supply |
| 157 | N1 | I/O | D | XVS | Vertical sync signal |
| 158 | N2 | I/O | D | XHS | Horizontal sync signal |
| 159 | N3 | I | D | XTRIG | Trigger input |
| 160 | N4 | - | - | N.C. | - |
| 161 | N5 | GND | D | VSSMIF | 1.8V GND |
| 162 | N6 | GND | D | VSSMIF | 1.8V GND |
| 163 | N7 | GND | D | VSSMIF | 1.8V GND |
| 164 | N8 | Power | D | VDDMIF | 1.8V power supply |
| 165 | N9 | Power | D | VDDMIF | 1.8V power supply |
| 166 | N10 | GND | D | VSSMIF | 1.8V GND |
| 167 | N11 | GND | D | VSSMIF | 1.8V GND |
| 168 | N12 | GND | D | VSSMIF | 1.8V GND |
| 169 | N13 | - | - | N.C. | - |
| 170 | N14 | - | - | N.C. | - |
| 171 | N15 | - | - | N.C. | - |
| 172 | N16 | - | - | N.C. | - |
| 173 | P1 | - | - | N.C. | - |
| 174 | P2 | - | - | N.C. | - |
| 175 | P3 | - | - | N.C. | - |
| 176 | P4 | O | D | DLOPC1 | Low boltage LVDS serial output (Data) |
| 177 | P5 | O | D | DLOPD1 | Low boltage LVDS serial output (Data) |
| 178 | P6 | O | D | DLOPF1 | Low boltage LVDS serial output (Data) |
| 179 | P7 | O | D | DLOPH1 | Low boltage LVDS serial output (Data) |
| 180 | P8 | GND | D | VSSMIF | 1.8V GND |
| 181 | P9 | GND | D | VSSMIF | 1.8V GND |
| 182 | P10 | O | D | DLOPA2 | Low boltage LVDS serial output (Data) |
| 183 | P11 | O | D | DLOPC2 | Low boltage LVDS serial output (Data) |
| 184 | P12 | O | D | DLOPE2 | Low boltage LVDS serial output (Data) |
| 185 | P13 | O | D | DLOPF2 | Low boltage LVDS serial output (Data) |
| 186 | P14 | - | - | N.C. | - |

| No. | Pin No. | I/O | Analog / Digital | Symbol | Description |
|---|---|---|---|---|---|
| 187 | P15 | - | - | N.C. | - |
| 188 | P16 | - | - | N.C. | - |
| 189 | R1 | - | - | N.C. | - |
| 190 | R2 | - | - | N.C. | - |
| 191 | R3 | O | D | DLOPA1 | Low boltage LVDS serial output (Data) |
| 192 | R4 | O | D | DLOMC1 | Low boltage LVDS serial output (Data) |
| 193 | R5 | O | D | DLOMD1 | Low boltage LVDS serial output (Data) |
| 194 | R6 | O | D | DLOMF1 | Low boltage LVDS serial output (Data) |
| 195 | R7 | O | D | DLOMH1 | Low boltage LVDS serial output (Data) |
| 196 | R8 | GND | D | VSSMIF | 1.8V GND |
| 197 | R9 | GND | D | VSSMIF | 1.8V GND |
| 198 | R10 | O | D | DLOMA2 | Low boltage LVDS serial output (Data) |
| 199 | R11 | O | D | DLOMC2 | Low boltage LVDS serial output (Data) |
| 200 | R12 | O | D | DLOME2 | Low boltage LVDS serial output (Data) |
| 201 | R13 | O | D | DLOMF2 | Low boltage LVDS serial output (Data) |
| 202 | R14 | O | D | DLOPH2 | Low boltage LVDS serial output (Data) |
| 203 | R15 | - | - | N.C. | - |
| 204 | R16 | - | - | N.C. | - |
| 205 | T3 | O | D | DLOMA1 | Low boltage LVDS serial output (Data) |
| 206 | T4 | O | D | DLOPB1 | Low boltage LVDS serial output (Data) |
| 207 | T5 | O | D | DLCKP1 | Low boltage LVDS serial output (Clock) |
| 208 | T6 | O | D | DLOPE1 | Low boltage LVDS serial output (Data) |
| 209 | T7 | O | D | DLOPG1 | Low boltage LVDS serial output (Data) |
| 210 | T8 | - | - | N.C. | - |
| 211 | T9 | - | - | N.C. | - |
| 212 | T10 | O | D | DLOPB2 | Low boltage LVDS serial output (Data) |
| 213 | T11 | O | D | DLOPD2 | Low boltage LVDS serial output (Data) |
| 214 | T12 | O | D | DLCKP2 | Low boltage LVDS serial output (Clock) |
| 215 | T13 | O | D | DLOPG2 | Low boltage LVDS serial output (Data) |
| 216 | T14 | O | D | DLOMH2 | Low boltage LVDS serial output (Data) |
| 217 | U1 | - | - | N.C. | - |
| 218 | U3 | - | - | N.C. | - |
| 219 | U4 | O | D | DLOMB1 | Low boltage LVDS serial output (Data) |
| 220 | U5 | O | D | DLCKM1 | Low boltage LVDS serial output (Clock) |
| 221 | U6 | O | D | DLOME1 | Low boltage LVDS serial output (Data) |
| 222 | U7 | O | D | DLOMG1 | Low boltage LVDS serial output (Data) |
| 223 | U8 | GND | D | VSSLSC | 1.2V GND |
| 224 | U9 | I | D | INCK | Master clock input |
| 225 | U10 | O | D | DLOMB2 | Low boltage LVDS serial output (Data) |
| 226 | U11 | O | D | DLOMD2 | Low boltage LVDS serial output (Data) |
| 227 | U12 | O | D | DLCKM2 | Low boltage LVDS serial output (Clock) |
| 228 | U13 | O | D | DLOMG2 | Low boltage LVDS serial output (Data) |
| 229 | U14 | - | - | N.C. | - |
| 230 | U16 | - | - | N.C. | - |

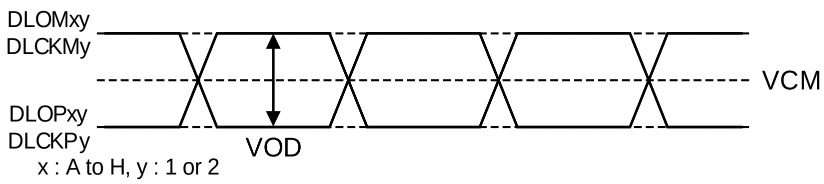
* N.C. pins in the table above should be left open on the board.

# Electrical Characteristics

## DC Characteristics

| Item | | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| Supply voltage | Analog | $V_{DD}$Hx | $AV_{DD}$ | — | 3.15 | 3.30 | 3.45 | V |
| | Interface | $V_{DD}$Mx | $OV_{DD}$ | — | 1.70 | 1.80 | 1.90 | V |
| | Digital | $V_{DD}$Lx | $DV_{DD}$ | — | 1.10 | 1.20 | 1.30 | V |
| Digital input voltage | | XHS<br>XVS<br>XCLR<br>INCK<br>XMASTER<br>SLAMODE<br>SCK<br>SDI<br>XCE<br>XTRIG | VIH | XVS / XHS<br>in Slave mode | 0.8 × $OV_{DD}$ | — | — | V |
| | | | VIL | | — | — | 0.2 × $OV_{DD}$ | V |
| Digital output voltage | | DLOPxy<br>DLOMxy<br>DCKPy<br>DCKMy<br>x : A to H<br>y : 1 or 2 | VCM | Low voltage LVDS<br>(termination<br>resistance: 100 Ω) | — | $OV_{DD}$/2 | — | V |
| | | | VOD | | TBD | 150 | TBD | mV |
| | | XHS<br>XVS<br>SDO<br>TOUT1<br>TOUT2 | VOH | XVS / XHS<br>in Master mode | $OV_{DD}$ -0.4 | — | — | V |
| | | | VOL | | — | — | 0.4 | V |

**LVDS output**




## Power Consumption

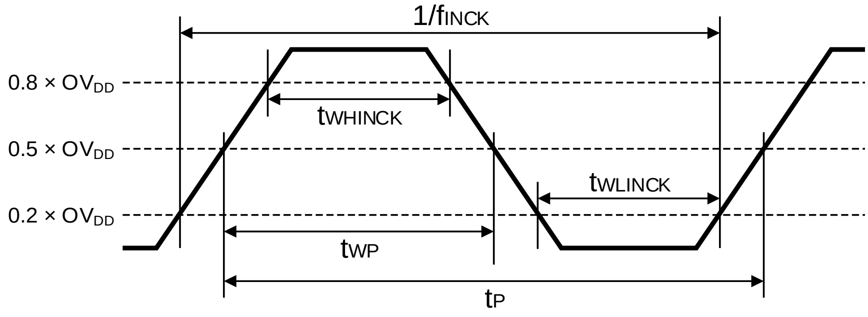
| Item | Pins | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating current<br>Serial LVDS TBDch<br>TBDbit TBD frame/s | $V_{DD}$H | $IAV_{DD}$ | TBD | TBD | mA |
| | $V_{DD}$M | $IOV_{DD}$ | TBD | TBD | mA |
| | $V_{DD}$L | $IDV_{DD}$ | TBD | TBD | mA |
| Standby current | $V_{DD}$H | $IAV_{DD}$_STB | — | TBD | mA |
| | $V_{DD}$M | $IOV_{DD}$_STB | — | TBD | mA |
| | $V_{DD}$L | $IDV_{DD}$_STB | — | TBD | mA |

Operating current:
(Typical value condition) : Supply voltage: 3.30 V / 1.80 V / 1.20 V, Tj = 25 ˚C
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C
Worst state of internal circuit operating current consumption.

Standby current:
(Maximum value condition) : Supply voltage: 3.45 V / 1.90 V / 1.30 V, Tj = 60 ˚C, INCK = 0 V,
The device in the light-obstructed state.

## AC Characteristics

### Master Clock (INCK) Waveform Diagram

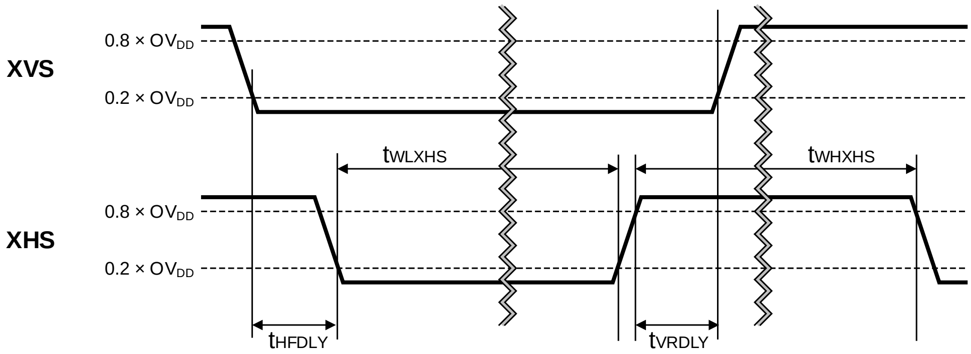



Duty Ratio = $t_{WP}$ / $t_P$ × 100

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| INCK clock frequency | $f_{INCK}$ | $f_{INCK}$ × 0.96 | $f_{INCK}$ | $f_{INCK}$ × 1.02 | MHz | $f_{INCK}$ = 37.125 MHz, 74.25 MHz, 54MHz |
| INCK Low level pulse width | $t_{WLINCK}$ | 4 | — | — | ns | |
| INCK High level pulse width | $t_{WHINCK}$ | 4 | — | — | ns | |
| INCK clock duty | — | 45.0 | 50.0 | 55.0 | % | Define with 0.5 × $OV_{DD}$ |

* The INCK fluctuation affects the frame rate.

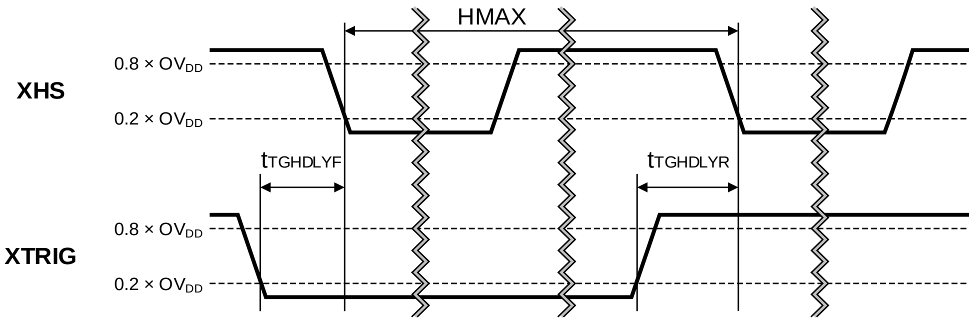
### XVS / XHS Input Characteristics in Slave Mode (XMASTER = High)




| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| XHS Low level pulse width | $t_{WLXHS}$ | $4/f_{INCK}$ | — | — | ns |
| XHS High level pulse width | $t_{WHXHS}$ | $4/f_{INCK}$ | — | — | ns |
| XVS - XHS fall width | $t_{HFDLY}$ | $1/f_{INCK}$ | — | — | ns |
| XHS - XVS rise width | $t_{VRDLY}$ | $1/f_{INCK}$ | — | — | ns |

Synchronization cannot be performed from XVS and XHS signal in mater mode. Detect the sync code.

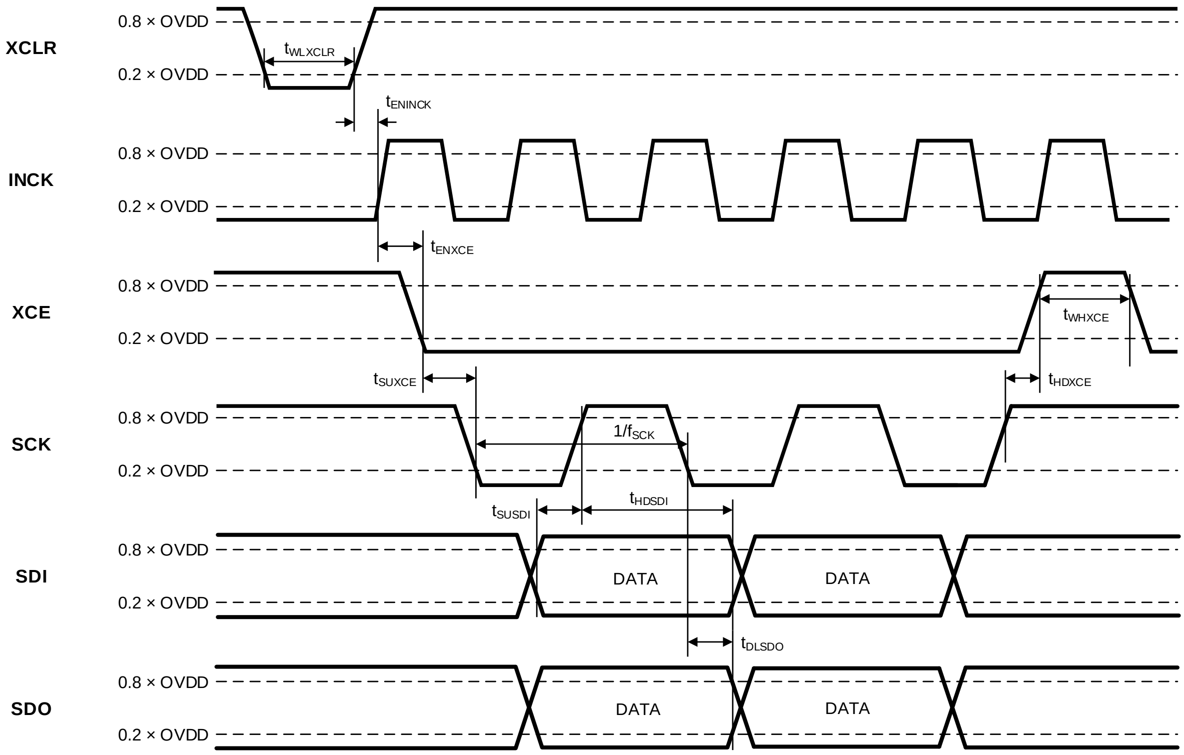
### XTRIG Input Characteristics in Slave Mode (XMASTER = High) only




| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| XTRIG fall - XHS fall width | $t_{TGHDLYF}$ | 10 | — | HMAX-10 | INCK |
| XTRIG rise - XHS fall width | $t_{TGHDLYR}$ | 10 | — | HMAX-10 | INCK |

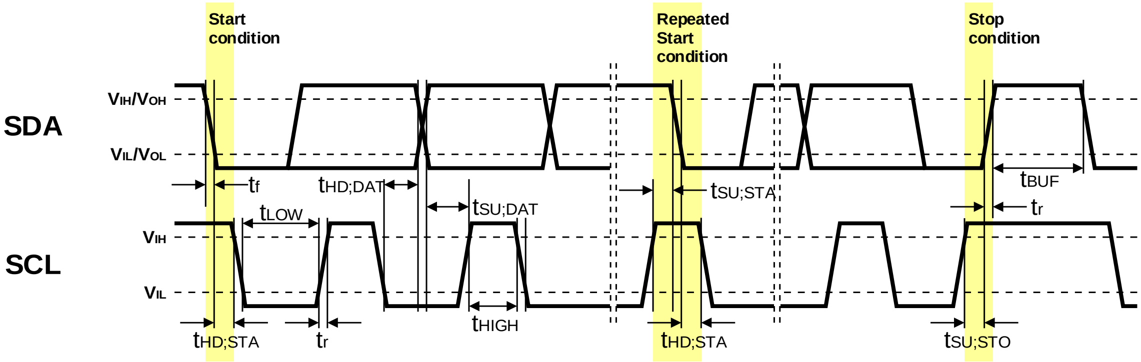
## Serial Communication

### 4-wire




| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| SCK clock frequency | $f_{SCK}$ | — | — | 13.5 | MHz | |
| XCLR Low level pulse width | $t_{WLXCLR}$ | $4/f_{INCK}$ | — | — | ns | |
| INCK effective margin | $t_{ENINCK}$ | 1 | — | — | µs | |
| XCE effective margin | $t_{ENXCE}$ | 20 | — | — | µs | |
| XCE input setup time | $t_{SUXCE}$ | 20 | — | — | ns | |
| XCE input hold time | $t_{HDXCE}$ | 20 | — | — | ns | |
| XCE High level pulse width | $t_{WHXCE}$ | 20 | — | — | ns | |
| SDI input setup time | $t_{SUSDI}$ | 10 | — | — | ns | |
| SDI input hold time | $t_{HDSDI}$ | 10 | — | — | ns | |
| SDO output delay time | $t_{DLSDO}$ | 0 | — | 25 | ns | Output load capacitance: 20 pF |

# $I^2C$



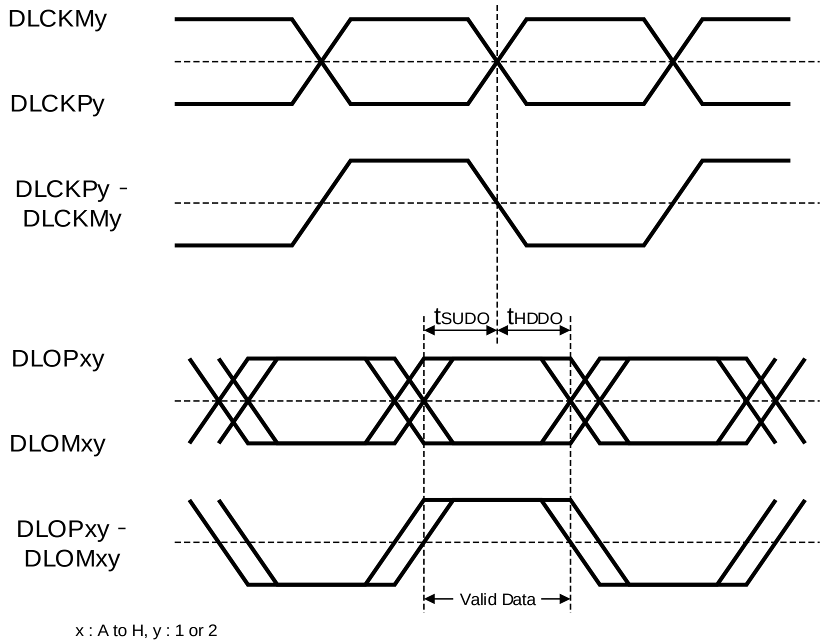

## $I^2C$ Specification

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Low level input voltage | $V_{IL}$ | -0.3 | — | $0.3 \times OV_{DD}$ | V | |
| High level input voltage | $V_{IH}$ | $0.7 \times OV_{DD}$ | — | 1.9 | V | |
| Low level output voltage | $V_{OL}$ | 0 | — | $0.2 \times OV_{DD}$ | V | $OV_{DD}$ < 2 V, Sink 3 mA |
| High level output voltage | $V_{OH}$ | $0.8 \times OV_{DD}$ | — | — | V | |
| Output fall time | tof | — | — | 250 | ns | Load 10 pF – 400 pF, $0.7 \times OV_{DD} – 0.3 \times OV_{DD}$ |
| Input current | Ii | -10 | — | 10 | µA | $0.1 \times OV_{DD} – 0.9 \times OV_{DD}$ |
| Capacitance for SCK (/SCL) , SDI (/SDA) | Ci | — | — | 10 | pF | |

## $I^2C$ AC Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | — | 400 | kHz |
| Hold time (Start Condition) | $t_{HDSTA}$ | 0.6 | — | — | µs |
| Low period of the SCL clock | $t_{LOW}$ | 1.3 | — | — | µs |
| High period of the SCL clock | $t_{HIGH}$ | 0.6 | — | — | µs |
| Set-up time (Repeated Start Condition) | $t_{SUSTA}$ | 0.6 | — | — | µs |
| Data hold time | $t_{HDDAT}$ | 0 | — | 0.9 | µs |
| Data set-up time | $t_{SUDAT}$ | 100 | — | — | ns |
| Rise time of both SDA and SCL signals | $t_R$ | — | — | 300 | ns |
| Fall time of both SDA and SCL signals | $t_F$ | — | — | 300 | ns |
| Set-up time (Stop Condition) | $t_{SUSTO}$ | 0.6 | — | — | µs |
| Bus free time between a Stop and Start Condition | $t_{BUF}$ | 1.3 | — | — | µs |

**DLCKPy / DLCKMy, DLOPxy / DLOMxy**

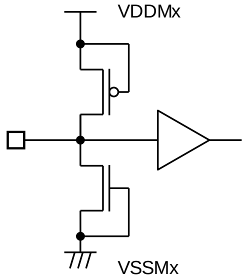
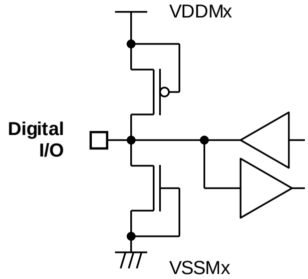
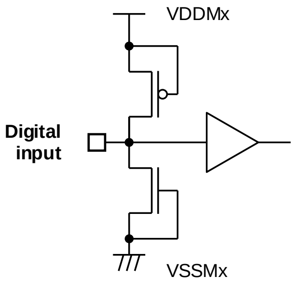
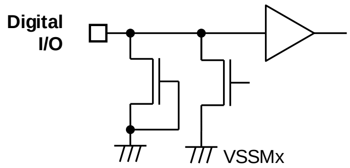
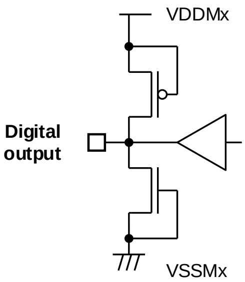
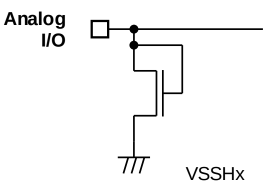
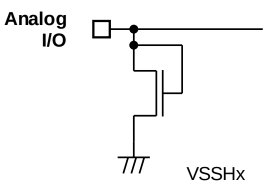
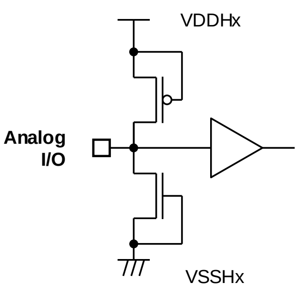
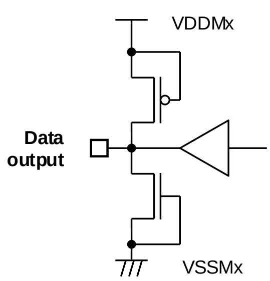



(Output load capacitance: 8 pF)

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| DLCK clock duty | — | TBD | 50 | TBD | % | DCK freq = 297 MHz (Max.) |
| DLO setup time | $t_{SUDO}$ | TBD | — | — | ps | Data Rate 297 MHz DDR |
| DLO hold time | $t_{HDDO}$ | TBD | — | — | ps | Data Rate 297 MHz DDR |

## I/O Equivalent Circuit Diagram

□ : External pin

<table>
<tr><th>Symbol</th><th>Equivalent circuit</th><th>Symbol</th><th>Equivalent circuit</th></tr>
<tr><td>INCK</td><td>
</td><td>XVS<br>XHS</td><td>
</td></tr>
<tr><td>XCLR<br>XCE<br>XMASTER<br>XTRIG<br>SLAMODE</td><td>
</td><td>SDI / SDA<br>SCK / SCL</td><td>
</td></tr>
<tr><td>SDO</td><td>
</td><td></td><td></td></tr>
<tr><td>VCP1<br>VCP2</td><td>
</td><td>VRLOFG<br>VRLTRX<br>VRLSEL<br>VRLTRG</td><td>
</td></tr>
<tr><td>VBGR</td><td>
</td><td>DLOPxy<br>DLOMxy<br>DCKPy<br>DCKMy<br>x : A to H<br>y : 1 or 2</td><td>
</td></tr>
</table>

## Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

TBD

## Image Sensor Characteristics

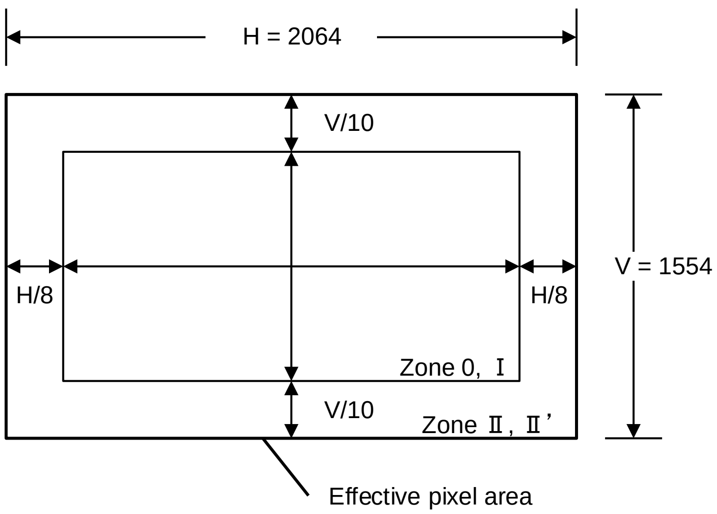
($AV_{DD}$ = 3.3 V, $OV_{DD}$ = 1.8 V, $DV_{DD}$ = 1.2 V, All-pixel scan mode, AD: 12 bit, Tj = 60 ˚C, Gain = 0 dB)

| Item | Symbol | Min. | Typ. | Max. | Unit | Measurement method | Remarks |
|---|---|---|---|---|---|---|---|
| Sensitivity | S | TBD (TBD ) | TBD (TBD ) | — | Digit (mV) | 1 | 1/30 s storage |
| Saturation signal | Vsat2D | TBD (TBD*1) | — | — | Digit (mV) | 2 | Zone 0 to II' |
| Video signal shading | SH01 | — | — | TBD | % | 3 | Zone 0, I |
| | SH2D | — | — | TBD | % | | Zone 0 to II' |
| Dark signal | Vdt | — | — | TBD (TBD ) | Digit (mV) | 4 | 1/30 s storage |
| Dark signal shading | ΔVdt | — | — | TBD (TBD ) | Digit (mV) | 5 | 1/30 s storage |
| PLS (Parasitic Light Sensitivity) | Sm | — | — | TBD | dB | 6 | Zone II' |

Note) 1. Converted value into mV using 1Digit = 0.2445 mV for 12-bit output, 1Digit = 0.9779 mV for 10-bit output and 1Digit = 0.9779 mV for 8-bit output.
2. The video signal shading is the measured value in the wafer status and does not include characteristics of the seal glass.

*1 In case of 8bit, Vsat2D becomes 1/4 of it at 12bit.

## Zone Definition of Video Signal Shading



# Image Sensor Characteristics Measurement Method

## Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the signal output of the measurement system.

## Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/$m^2$, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard image condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard image condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -100 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

## Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the signal outputs (V) at the center of the screen, and substitute the values into the following formula.

   $S = (V) \times 100/30$ [mV]

2. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal outputs, TBD mV, measure the average values of the signal outputs.

3. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the signal outputs is TBD mV. Then measure the maximum value (Vmax [mV]) and the minimum value (Vmin [mV]) of the signal outputs, and substitute the values into the following formula.

   $SH = (Vmax – Vmin) / TBD \times 100$ [%]

4. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

5. Dark signal shading
   After the measurement item 4, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   $\Delta Vdt = Vdmax – Vdmin$ [mV]

6. PLS
   Set the measurement condition to the standard imaging condition II, the output signal Vave measured by standard image condition. Then, adjust the luminous intensity to 500 times the intensity with average value of the signal output, Vave. When the charge drain is executed be the electronic shutter and the condition that not be readout from photo diode to analog memory, readout by dropping to 1/113 frame rate.

   $Sm = 20 \times \log ((Vsm/Vave) \times (1/500) \times (1/113))$ [dB]

# Setting Registers Using Serial Communication

## Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

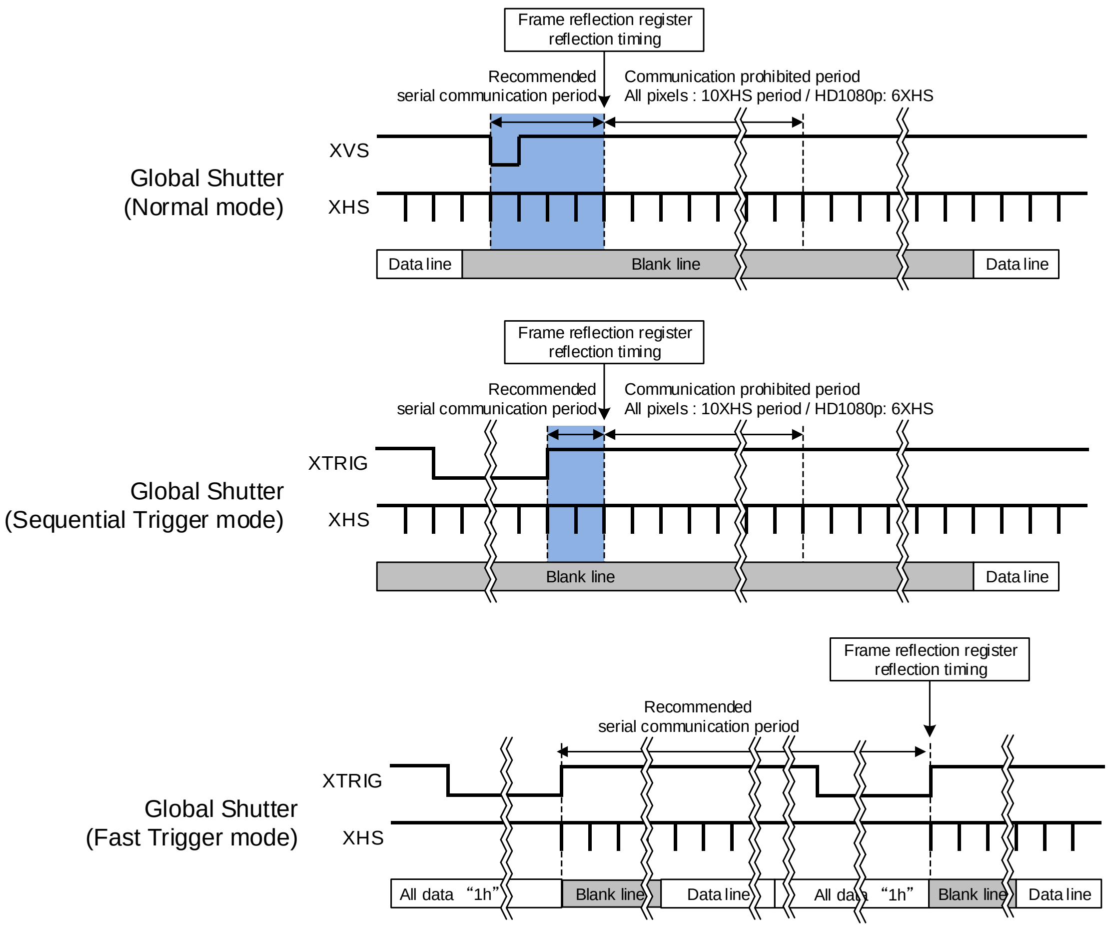
| Chip ID | Start address | Data | Data | Data | … |
|---|---|---|---|---|---|
| (8 bit) | (8 bit) | (8 bit) | (8 bit) | (8 bit) | (8 bit) |

Type and Description

| Type | Description |
|---|---|
| Chip ID | Chip ID: 02 Write: 02h / Read: 82h |
| | Chip ID: 03 Write: 03h / Read: 83h |
| | Chip ID: 04 Write: 04h / Read: 84h |
| | Chip ID: 05 Write: 05h / Read: 85h |
| | Chip ID: 06 Write: 06h / Read: 86h |
| | Chip ID: 07 Write: 07h / Read: 87h |
| | Chip ID: 08 Write: 08h / Read: 88h |
| | Chip ID: 09 Write: 09h / Read: 89h |
| | Chip ID: 0A Write: 0Ah / Read: 8Ah |
| | Chip ID: 0B Write: 0Bh / Read: 8Bh |
| | Chip ID: 0C Write: 0Ch / Read: 8Ch |
| | Chip ID: 0D Write: 0Dh / Read: 8Dh |
| | Chip ID: 0E Write: 0Eh / Read: 8Eh |
| | Chip ID: 0F Write: 0Fh / Read: 8Fh |
| | Chip ID: 10 Write: 10h / Read: 90h |
| | Chip ID: 11 Write: 11h / Read: 91h |
| | Chip ID: 12 Write: 12h / Read: 92h |
| Address | Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address. |
| Data | Input the setting values according to the Register Map. |

## Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within communication period. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers, set them in sensor standby state.)



## Register Write and Read (4-wire)

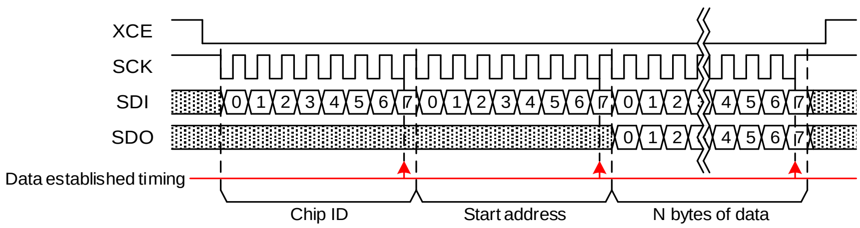
◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h to 12h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

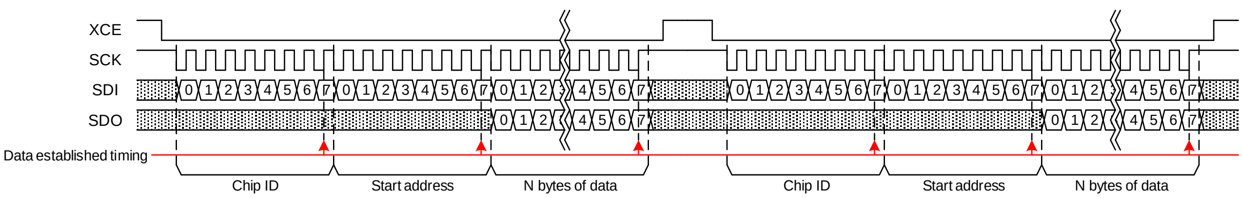
◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h to 92h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



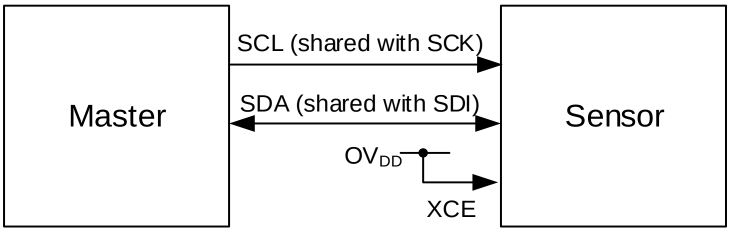

Serial Communication (Continuous Addresses)




Serial Communication (Discontinuous Addresses)

## Description of Setting Registers ($I^2C$)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.




Pin connection of serial communication

SLAVE Address (SLAMODE = 0)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | R / W |

SLAVE Address (SLAMODE = 1)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | R / W |

* R/W is data direction bit

R/W

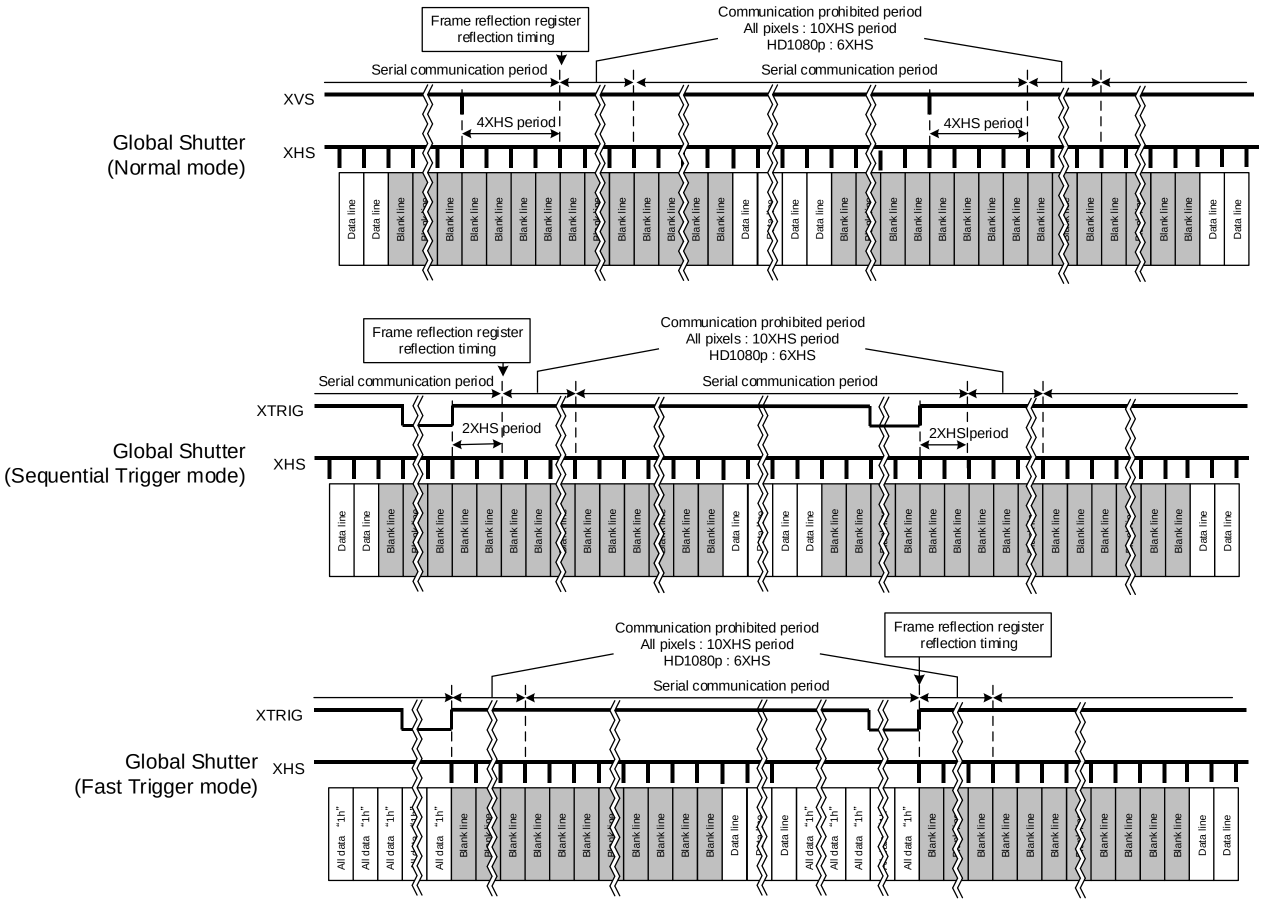
| R / W bit | Data direction |
|---|---|
| 0 | Write (Master → Sensor) |
| 1 | Read (Sensor → Master) |

$I^2C$ pin description

| Symbol | Pin No. | Description |
|---|---|---|
| SCL (common to SCK) | L3 | Serial clock input |
| SDA (common to SDI) | M3 | Serial data communication |

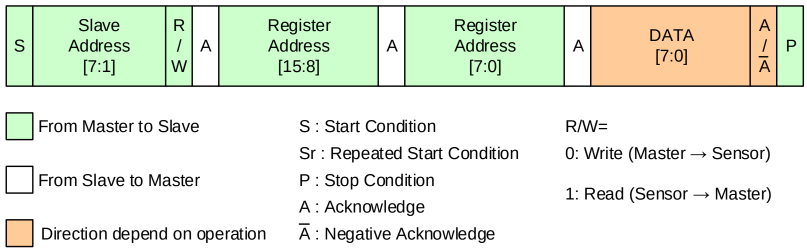
## Register Communication Timing ($I^2C$)

In $I^2C$ communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 4H after.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA set them in sensor standby state.)
Using REG_HOLD function is recommended for register setting using $I^2C$ communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”.



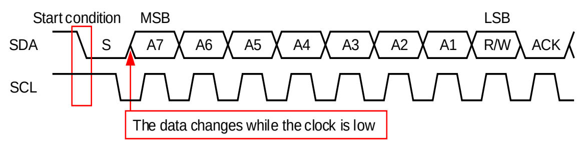
## I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

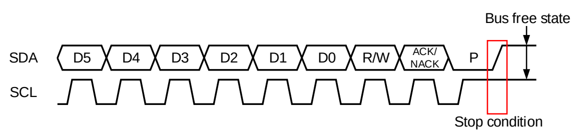



Communication protocol

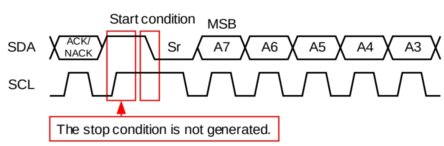
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.




Start Condition

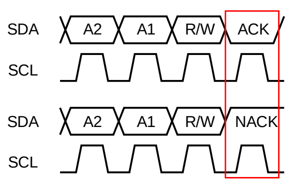



Stop Condition




Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



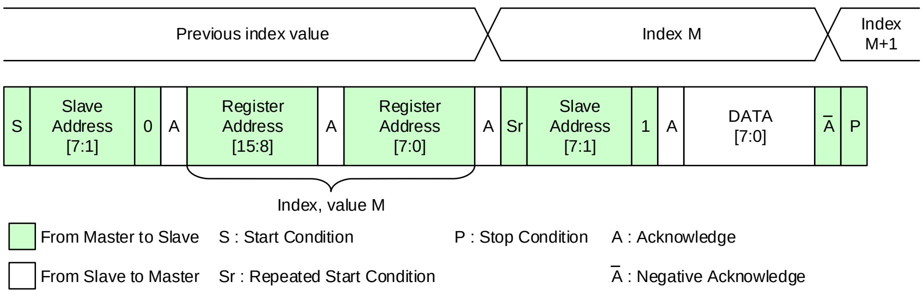

Acknowledge and Negative Acknowledge

## I²C Serial Communication Read/Write Operation

This sensor supports the following four read operations and two write operations.

### Single Read from Random Location

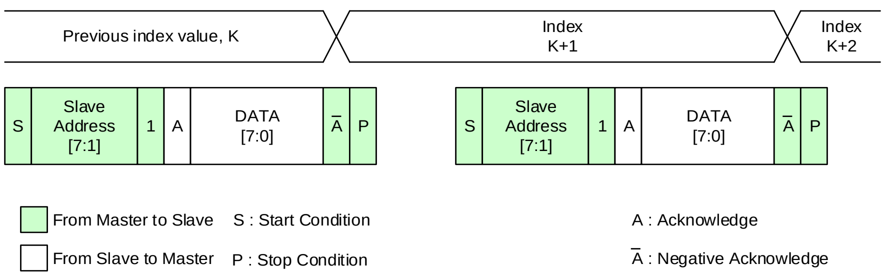
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.




Single Read from Random Location

### Single Read from Current Location

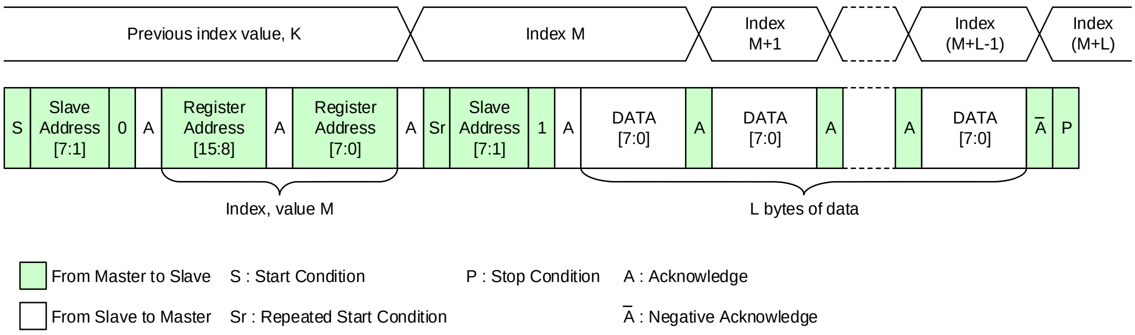
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.




Single Read from Current Location

### Sequential Read Starting from Random Location

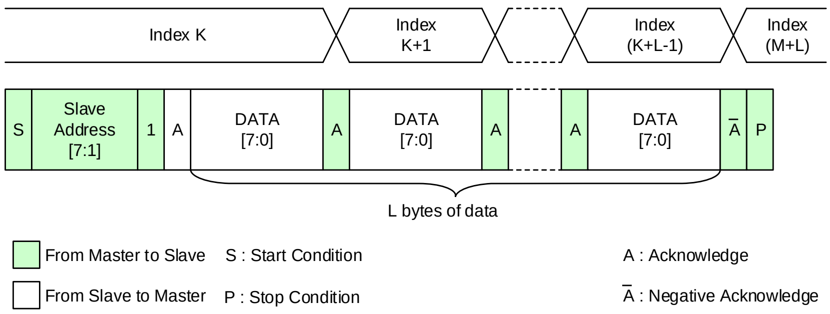
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.




Sequential Read Starting from Random Location

### Sequential Read Starting from Current Location

When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.




Sequential Read Starting from Current Location

## Register Map (There is a possible to change the registers on this document)

This sensor has a total of 4352 bytes of registers, composed of registers with address 00h to FFh that correspond to Chip ID = 02h to 12h. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 4352 bytes.

There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers below, set them in sensor standby state.

・STBLVDS
・ADBIT
・ODBIT
・OPORTSEL
・INCKSEL0
・INCKSEL1
・INCKSEL2
・INCKSEL3

For the register that is writing "*" to the setting value in description, change the value from the default value after the reset.

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors.

### Chip ID = 02 (Write: Chip ID = 02h, Read: Chip ID = 82h, $I^2C$ : 30**h)

Please refer to the register map for the register that has not been described.

| Address 4-wire | Address $I^2C$ | bit | Register Name | Description | Default value after reset By register | Default value after reset By address | Reflection timing |
|---|---|---|---|---|---|---|---|
| 00h | 3000h | 0 | STANDBY [0] | Standby mode<br>0: Normal operation 1: Standby | 1 | 01h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 05h | 3005h | 0 | | Fixed to 0 | 0 | 00h | — |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4<br>5<br>6<br>7 | STBLVDS | LVDS channels that not using be standby<br>0h: 16 ch active<br>1h: 8 ch active<br>2h: 4 ch active<br>Others: Setting prohibited | 0h | | Immediately |
| 08h | 3008h | 0 | REGHOLD [0] | Register hold<br>(Function not to update V reflection registers)<br>0: Invalid 1: Valid | 0 | 00h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 0A | 300Ah | 0 | XMSTA [0] | Setting of master mode operation<br>0: Master mode operation start<br>1: Master mode operation stop | 1 | 01h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 0Bh | 300Bh | 0 | TRIGEN [0] | Global shutter mode setting<br>0: Normal mode 1: Trigger mode | 0 | 00h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |

| Address | | bit | Register Name | Description | Default value after reset | | Reflection timing |
|---|---|---|---|---|---|---|---|
| 4-wire | $I^2C$ | | | | By register | By address | |
| 0Ch | 300Ch | 0 | ADBIT [1:0] | AD conversion bits setting<br>0h : 10 bit 1h : 12 bit 2h : 8bit<br>3h : Setting prohibited | 0h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 0Dh | 300Dh | 0 | WINMODE [3:0] | Drive mode setting of V direction<br>0h : All-pixel mode<br>1h : 1/2 Subsampling mode<br>2h : FD Binning mode<br>Ch : Full-HD<br>Others: Setting prohibited | 0 | 00h | Immediately |
| | | 1 | | | 0 | | |
| | | 2 | | | 0 | | |
| | | 3 | | | 0 | | |
| | | 4 | HMODE[0] | Drive mode setting of H direction<br>0 : All-pixel<br>1 : 1/2 Subsampling mode | 0 | | V |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 0Eh | 300Eh | 0 | VREVERSE [0] | Vertical (V) direction readout inversion control<br>0: Normal 1: Inverted | 0 | 00h | Immediately |
| | | 1 | HREVERSE [0] | Horizontal (H) direction readout inversion control<br>0: Normal 1: Inverted | 0 | | V |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 10h | 3010h | 0 | VMAX [19:0] | LSB | 0082Eh | 2Eh | V |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 11h | 3011h | 0 | | When sensor master mode vertical span setting.<br>(Number of operation lines count from 1) | | 08h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 12h | 3012h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | MSB | | | |
| | | 4 | | Fixed to 0 | 0 | | |
| | | 5 | | Fixed to 0 | 0 | | |
| | | 6 | | Fixed to 0 | 0 | | |
| | | 7 | | Fixed to 0 | 0 | | |

| Address 4-wire | Address I²C | bit | Register Name | Description | Default value after reset By register | Default value after reset By address | Reflection timing |
|---|---|---|---|---|---|---|---|
| 14h | 3014h | 0 | HMAX [15:0] | LSB | 015Eh | 5Eh | V |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | When sensor master mode horizontal span setting. (Number of operation clocks count from 1) | | | |
| | | 7 | | | | | |
| 15h | 3015h | 0 | | | | 01h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | MSB | | | |
| 16h | 3016h | 0 | ODBIT [1:0] | Number of output bit setting<br>0h : 10 bit 1h : 12 bit 2h : 8bit<br>3h ; Setting prohibited | 0h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 19h | 3019h | 0 | CKSEL [0] | The value is set according to drive mode.<br>When All-pixel, ROI, 1/2 Subsampling, FD Binning: 0<br>When 1080p-Full HD: 1 | 0 | 00h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 1Bh | 301Bh | 0 | FREQ [1:0] | Set to data rate.<br>0h : Normal<br>1h : Data rate 1/2 | 0h | 00h | V |
| | | 1 | | | | | |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 1Ch | 301Ch | 0 | | Fixed to 0 | 0 | 90h | — |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | OPORTSEL [3:0] | Output channel selection<br>1h : 8 ch 3h : 4 ch 9h : 16ch<br>Others: Setting prohibited | 9h | | Immediately |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 26h | 3026h | 0 | TOUT1SEL[1:0] | TOUT1 pin setting<br>0h: Low fixed 3h: Pulse output | 0h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | TOUT2SEL [1:0] | TOUT2 pin setting<br>0h: Low fixed 3h: Pulse output | 0h | | Immediately |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |

| Address | | bit | Register Name | Description | Default value after reset | | Reflection timing |
|---|---|---|---|---|---|---|---|
| 4-wire | $I^2C$ | | | | By register | By address | |
| 29h | 3029h | 0 | TRIG_TOUT1_SEL [2:0] | TOUT1 pin setting<br>0h: Low fixed 1h: Pulse1 output | 0h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | TRIG_TOUT2_SEL [2:0] | TOUT2 pin setting<br>0h: Low fixed 2h: Pulse2 output | 0h | | Immediately |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | Fixed to 0 | 0 | | — |
| 36h | 3036h | 0 | | Fixed to 0 | 0 | C0h | — |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | SYNCSEL | XHS, XVS pin setting<br>0h : Normal Output<br>3h : Hi-Z | 0h | | Immediately |
| | | 5 | | | | | |
| | | 6 | | Fixed to 1 | 1 | | — |
| | | 7 | | Fixed to 1 | 1 | | — |
| 6Dh | 306Dh | 0 | PULSE1_EN_NOR [0] | Pulse1 output in normal mode<br>0: Disable 1: Enable | 0 | 00h | Immediately |
| | | 1 | PULSE1_EN_TRIG [0] | Pulse1 output in trigger mode<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 2 | PULSE1_POL | Pulse1 polarity selection<br>0: High active 1: Low active | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 70h | 3070h | 0 | PULSE1_UP [19:0] | LSB<br>Pulse1 active period start timing setting<br>Designated in line units from reference point<br>(For details, see the "Pulse Output Function")<br>MSB | 00000h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 71h | 3071h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 72h | 3072h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |

| Address | | bit | Register Name | Description | Default value after reset | | Reflection timing |
|---|---|---|---|---|---|---|---|
| 4-wire | $I^2C$ | | | | By register | By address | |
| 74h | 3074h | 0 | PULSE1_DN [19:0] | LSB<br>Pulse1 active period end timing setting<br>Designated in line units from readout start<br>(For details, see the "Pulse Output Function")<br>MSB | 00000h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 75h | 3075h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 76h | 3076h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 79h | 3079h | 0 | PULSE2_EN_NOR [0] | Pulse2 output in normal mode<br>0: Disable 1: Enable | 0 | 00h | Immediately |
| | | 1 | PULSE2_EN_TRIG [0] | Pulse2 output in trigger mode<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 2 | PULSE2_POL [0] | Pulse2 polarity selection<br>0: High active 1: Low active | 0 | | Immediately |
| | | 3 | | Fixed to 1 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 7Ch | 307Ch | 0 | PULSE2_UP [19:0] | LSB<br>Pulse2 active period start timing setting<br>Designated in line units from reference point<br>(For details, see the "Pulse Output Function")<br>MSB | 00000h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 7Dh | 307Dh | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 7Eh | 307Eh | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |

| Address (4-wire) | Address (I²C) | bit | Register Name | Description | Default value after reset (By register) | Default value after reset (By address) | Reflection timing |
|---|---|---|---|---|---|---|---|
| 80h | 3080h | 0 | PULSE2_DN [19:0] | LSB<br>Pulse2 active period end timing setting<br>Designated in line units from reference point<br>(For details, see the “Pulse Output Function”)<br>MSB | 00000h | 00h | Immediately |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 81h | 3081h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 82h | 3082h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 89h | 3089h | [7:0] | INCKSEL0 [7:0] | Set according to INCK frequency and drive mode. | 20h | 20h | Immediately |
| 8Ah | 308Ah | [7:0] | INCKSEL1 [7:0] | Set according to INCK frequency and drive mode. | 00h | 00h | Immediately |
| 8Bh | 308Bh | [7:0] | INCKSEL2 [7:0] | Set according to INCK frequency and drive mode. | 20h | 20h | Immediately |
| 8Ch | 308Ch | [7:0] | INCKSEL3 [7:0] | Set according to INCK frequency and drive mode. | 00h | 00h | Immediately |
| 8Dh | 308Dh | 0 | SHS [19:0] | LSB<br>Storage time adjustment<br>Designated in line unit<br>MSB | 0000Ah | 0Ah | V |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 8Eh | 308Eh | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 8Fh | 308Fh | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 9Eh | 309Eh | [7:0] | GTWAIT [7:0] | The value is set according to drive mode.<br>When All-pixel, ROI, 1/2 Subsampling, FD Binning: 0Ah<br>When 1080p-Full HD: 06h | 0Ah | 0Ah | Immediately |

| Address | | bit | Register Name | Description | Default value after reset | | Reflection timing |
|---|---|---|---|---|---|---|---|
| 4-wire | $I^2C$ | | | | By register | By address | |
| A0h | 30A0h | [7:0] | GSDLY [7:0] | The value is set according to drive mode.<br>When All-pixel, ROI,<br>1/2 Subsampling, FD Binning: 08h<br>When 1080p-Full HD: 04h | 08h | 08h | Immediately |
| AAh | 30AAh | 0 | VINT_EN | Setting of Interrupt mode in Trigger Mode<br>0 : V interrupt is disable<br>1 : V interrupt is enable | 1 | 01h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| AEh | 30AEh | 0 | LOWLAGTRG | Selection of trigger mode<br>0 : Sequential trigger mode<br>1 : Fast trigger mode | 0 | 00h | Immediately |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| AFh | 30AFh | [7:0] | | The value is set according to drive mode.<br>When All-pixel, ROI,<br>1/2 Subsampling, FD Binning: 0Eh<br>When 1080p-Full HD: 0Ah | 06h | 06h | — |

**Chip ID = 03 (Write: Chip ID = 03h, Read: Chip ID = 83h, $I^2C$ : 31**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 04 (Write: Chip ID = 04h, Read: Chip ID = 84h, I²C : 32**h)**

Please refer to the register map for the register that has not been described.

| Address 4-wire | Address I²C | bit | Register Name | Description | Default value after reset By register | Default value after reset By address | Reflection timing |
|---|---|---|---|---|---|---|---|
| 04h | 3204h | 0 | GAIN [8:0] | LSB<br>Gain setting<br>0 dB (000d) ~ 48 dB (480d)<br>0.1 dB Step<br>MSB | 000h | 00h | V |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 05h | 3205h | 0 | | | | 00h | |
| | | 1 | | Fixed to 0 | 0 | | — |
| | | 2 | | Fixed to 0 | 0 | | — |
| | | 3 | | Fixed to 0 | 0 | | — |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |
| 54h | 3254h | 0 | BLKLEVEL [11:0] | LSB<br>Black level offset value setting<br>Recommended value:<br>8bit : 00Fh<br>10bit : 03Ch<br>12bit : 0F0h<br>MSB | 03Ch | 3Ch | V |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | | | | |
| | | 5 | | | | | |
| | | 6 | | | | | |
| | | 7 | | | | | |
| 55h | 3255h | 0 | | | | 00h | |
| | | 1 | | | | | |
| | | 2 | | | | | |
| | | 3 | | | | | |
| | | 4 | | Fixed to 0 | 0 | | — |
| | | 5 | | Fixed to 0 | 0 | | — |
| | | 6 | | Fixed to 0 | 0 | | — |
| | | 7 | | Fixed to 0 | 0 | | — |

### Chip ID = 05 (Write: Chip ID = 05h, Read: Chip ID = 85h, $I^2C$ : 33**h)

Please refer to the register map for the register that has not been described.

| Address 4-wire | Address I²C | bit | Register Name | Description | Default value after reset By register | Default value after reset By address | Reflection timing |
|---|---|---|---|---|---|---|---|
| 00h | 3300h | 0 | FID0_ROIH1ON [0] | The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | 00h | V |
| | | 1 | FID0_ROIV1ON [0] | The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 2 | FID0_ROIH2ON [0] | The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 3 | FID0_ROIV2ON [0] | The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 4 | FID0_ROIH3ON [0] | The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 5 | FID0_ROIV3ON [0] | The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 6 | FID0_ROIH4ON [0] | The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 7 | FID0_ROIV4ON [0] | The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| 01h | 3301h | 0 | FID0_ROIH5ON [0] | The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | 00h | V |
| | | 1 | FID0_ROIV5ON [0] | The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 2 | FID0_ROIH6ON [0] | The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 3 | FID0_ROIV6ON [0] | The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 4 | FID0_ROIH7ON [0] | The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 5 | FID0_ROIV7ON [0] | The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| | | 6 | FID0_ROIH8ON [0] | The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8)<br>0: Disable 1: Enable | 0 | | V |
| | | 7 | FID0_ROIV8ON [0] | The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8)<br>0: Disable 1: Enable | 0 | | Immediately |
| 10h | 3310h | [7:0] | FID0_ROIPH1 [12:0] | Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | 0000h | 00h | V |
| 11h | 3311h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 12h | 3312h | [7:0] | FID0_ROIPV1 [11:0] | Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8)<br>*Set the value of multiple of 4 | 000h | 00h | Immediately |
| 13h | 3313h | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 14h | 3314h | [7:0] | FID0_ROIWH1 [12:0] | Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | 0000h | 00h | V |
| 15h | 3315h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |

| Address 4-wire | Address I²C | bit | Register Name | Description | Default value after reset By register | Default value after reset By address | Reflection timing |
|---|---|---|---|---|---|---|---|
| 16h | 3316h | [7:0] | FID0_ROIWV1 [11:0] | Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 17h | 3317h | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 18h | 3318h | [7:0] | FID0_ROIPH2 [12:0] | Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 19h | 3319h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 1Ah | 331Ah | [7:0] | FID0_ROIPV2 [11:0] | Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 1Bh | 331Bh | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 1Ch | 331Ch | [7:0] | FID0_ROIWH2 [12:0] | Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 1Dh | 331Dh | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 1Eh | 331Eh | [7:0] | FID0_ROIWV2 [11:0] | Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 1Fh | 331Fh | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 20h | 3320h | [7:0] | FID0_ROIPH3 [12:0] | Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 21h | 3321h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 22h | 3322h | [7:0] | FID0_ROIPV3 [11:0] | Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 23h | 3323h | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 24h | 3324h | [7:0] | FID0_ROIWH3 [12:0] | Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 25h | 3325h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 26h | 3326h | [7:0] | FID0_ROIWV3 [11:0] | Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 27h | 3327h | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 28h | 3328h | [7:0] | FID0_ROIPH4 [12:0] | Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 29h | 3329h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 2Ah | 332Ah | [7:0] | FID0_ROIPV4 [11:0] | Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 2Bh | 332Bh | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 2Ch | 332Ch | [7:0] | FID0_ROIWH4 [12:0] | Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 2Dh | 332Dh | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 2Eh | 332Eh | [7:0] | FID0_ROIWV4 [11:0] | Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 2Fh | 332Fh | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 30h | 3330h | [7:0] | FID0_ROIPH5 [12:0] | Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 31h | 3331h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |
| 32h | 3332h | [7:0] | FID0_ROIPV5 [11:0] | Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 33h | 3333h | [3:0] | | | | 00h | |
| | | [7:4] | | Fixed to 0h | 0h | | — |
| 34h | 3334h | [7:0] | FID0_ROIWH5 [12:0] | Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 35h | 3335h | [4:0] | | | | 00h | |
| | | [7:5] | | Fixed to 0h | 0h | | — |

| Address |  | bit | Register Name | Description | Default value after reset |  | Reflection timing |
|---|---|---|---|---|---|---|---|
| 4-wire | $I^2C$ |  |  |  | By register | By address |  |
| 36h | 3336h | [7:0] | FID0_ROIWV5 [11:0] | Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 37h | 3337h | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 38h | 3338h | [7:0] | FID0_ROIPH6 [12:0] | Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 39h | 3339h | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 3Ah | 333Ah | [7:0] | FID0_ROIPV6 [11:0] | Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 3Bh | 333Bh | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 3Ch | 333Ch | [7:0] | FID0_ROIWH6 [12:0] | Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 3Dh | 333Dh | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 3Eh | 333Eh | [7:0] | FID0_ROIWV6 [11:0] | Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 3Fh | 333Fh | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 40h | 3340h | [7:0] | FID0_ROIPH7 [12:0] | Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 41h | 3341h | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 42h | 3342h | [7:0] | FID0_ROIPV7 [11:0] | Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 43h | 3343h | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 44h | 3344h | [7:0] | FID0_ROIWH7 [12:0] | Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 45h | 3345h | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 46h | 3346h | [7:0] | FID0_ROIWV7 [11:0] | Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 47h | 3347h | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 48h | 3348h | [7:0] | FID0_ROIPH8 [12:0] | Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 49h | 3349h | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 4Ah | 334Ah | [7:0] | FID0_ROIPV8 [11:0] | Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 4Bh | 334Bh | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |
| 4Ch | 334Ch | [7:0] | FID0_ROIWH8 [12:0] | Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) *Set the value of multiple of 4 | 0000h | 00h | V |
| 4Dh | 334Dh | [4:0] |  |  |  | 00h |  |
|  |  | [7:5] |  | Fixed to 0h | 0h |  | — |
| 4Eh | 334Fh | [7:0] | FID0_ROIWV8 [11:0] | Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) *Set the value of multiple of 4 | 000h | 00h | Immediately |
| 4Fh | 334Fh | [3:0] |  |  |  | 00h |  |
|  |  | [7:4] |  | Fixed to 0h | 0h |  | — |

### Chip ID = 06 (Write: Chip ID = 06h, Read: Chip ID = 86h, $I^2C$ : 34**h)

Please refer to the register map for the register that has not been described.

### Chip ID = 07 (Write: Chip ID = 07h, Read: Chip ID = 87h, $I^2C$ : 35**h)

Please refer to the register map for the register that has not been described.

**Chip ID = 08 (Write: Chip ID = 08h, Read: Chip ID = 88h, $I^2C$ : 36**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 09 (Write: Chip ID = 09h, Read: Chip ID = 89h, $I^2C$ : 37**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0A (Write: Chip ID = 0Ah, Read: Chip ID = 8Ah, $I^2C$ : 38**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0B (Write: Chip ID = 0Bh, Read: Chip ID = 8Bh, $I^2C$ : 39**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0C (Write: Chip ID = 0Ch, Read: Chip ID = 8Ch, $I^2C$ : 3A**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0D (Write: Chip ID = 0Dh, Read: Chip ID = 8Dh, $I^2C$ : 3B**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0E (Write: Chip ID = 0Eh, Read: Chip ID = 8Eh, $I^2C$ : 3C**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 0F (Write: Chip ID = 0Fh, Read: Chip ID = 8Fh, $I^2C$ : 3D**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 10 (Write: Chip ID = 10h, Read: Chip ID = 90h, $I^2C$ : 3E**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 11 (Write: Chip ID = 11h, Read: Chip ID = 91h, $I^2C$ : 3F**h)**

Please refer to the register map for the register that has not been described.

**Chip ID = 12 (Write: Chip ID = 12h, Read: Chip ID = 92h, $I^2C$ : 40**h)**

Please refer to the register map for the register that has not been described.

## Readout Drive Modes

The table below lists the operating modes available with this sensor. (Each value is the max frame rate of the each number of ch.)

FREQ(CID = 02h, Address = 1Bh, [1:0]) = 0h

| Drive mode | Frame rate [frame/s] | Data rate [Gbps] | Serial LVDS ch[*1] | A/D conversion | Number of recording pixels | | Total number of pixels[*2] | | Number of INCK in 1H | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | H | V | H | V | INCK: 37.125 MHz | INCK: 74.25 MHz | INCK: 54 MHz |
| All pixel | 216.2 | 9.504 | 16 | 8 | 2048 | 1536 | 3472 | 1582 | 108.5 | 217.0 | 157.8 |
| | 151.4 | 4.752 | 8 | | | | 2480 | | 155.0 | 310.0 | 225.5 |
| | 81.4 | 2.376 | 4 | | | | 2304 | | 288.0 | 576.0 | 418.9 |
| | 191.5 | 9.504 | 16 | 10 | | | 3136 | | 122.5 | 245.0 | 178.2 |
| | 123.5 | 4.752 | 8 | | | | 2432 | | 190.0 | 380.0 | 276.4 |
| | 66.1 | 2.376 | 4 | | | | 2272 | | 355.0 | 710.0 | 516.4 |
| | 118.5 | 9.504 | 16 | 12 | | | 4224 | | 198.0 | 396.0 | 288.0 |
| | 105.7 | 4.752 | 8 | | | | 2368 | | 222.0 | 444.0 | 322.9 |
| | 55.4 | 2.376 | 4 | | | | 2256 | | 423.0 | 846.0 | 615.3 |
| All pixel (Vertical / Horizontal 1/2 subsampling) | 422.4 | 9.504 | 16 | 8 | 1024 | 768 | 3472 | 810 | 108.5 | 217.0 | 157.8 |
| | 420.4 | 4.752 | 8 | | | | 1744 | | 109.0 | 218.0 | 158.5 |
| | 286.4 | 2.376 | 4 | | | | 1280 | | 160.0 | 320.0 | 232.7 |
| | 374.1 | 9.504 | 16 | 10 | | | 3136 | | 122.5 | 245.0 | 178.2 |
| | 374.1 | 4.752 | 8 | | | | 1568 | | 122.5 | 245.0 | 178.2 |
| | 235.0 | 2.376 | 4 | | | | 1248 | | 195.0 | 390.0 | 283.6 |
| | 231.4 | 9.504 | 16 | 12 | | | 4224 | | 198.0 | 396.0 | 288.0 |
| | 231.4 | 4.752 | 8 | | | | 2112 | | 198.0 | 396.0 | 288.0 |
| | 201.0 | 2.376 | 4 | | | | 1216 | | 228.0 | 456.0 | 331.6 |
| Vertical FD Binning | 422.4 | 9.504 | 16 | 8 | 2048 | 772 | 3472 | 810 | 108.5 | 217.0 | 157.8 |
| | 295.7 | 4.752 | 8 | | | | 2480 | | 155.0 | 310.0 | 225.5 |
| | 159.1 | 2.376 | 4 | | | | 2304 | | 288.0 | 576.0 | 418.9 |
| | 374.1 | 9.504 | 16 | 10 | | | 3136 | | 122.5 | 245.0 | 178.2 |
| | 241.2 | 4.752 | 8 | | | | 2432 | | 190.0 | 380.0 | 276.4 |
| | 129.1 | 2.376 | 4 | | | | 2272 | | 355.0 | 710.0 | 516.4 |
| | 231.4 | 9.504 | 16 | 12 | | | 4224 | | 198.0 | 396.0 | 288.0 |
| | 206.4 | 4.752 | 8 | | | | 2368 | | 222.0 | 444.0 | 322.9 |
| | 108.3 | 2.376 | 4 | | | | 2256 | | 423.0 | 846.0 | 615.3 |

| Drive mode | Frame rate [frame/s] | Data rate [Gbps] | Serial LVDS ch[*1] | A/D conversion | Number of recording pixels | | Total number of pixels[*2] | | Number of INCK in 1H | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | H | V | H | V | INCK: 37.125 MHz | INCK: 74.25 MHz | INCK: 54 MHz |
| HD1080p | 120 | 3.564 | 8 | 10 | 1920 | 1080 | 2640 | 1125 | 275.0 | 550.0 | 400.0 |
| | 60 | 1.782 | 4 | | | | | | 550.0 | 1100.0 | 800.0 |
| | 120 | 3.564 | 8 | 12 | | | 2200 | | 275.0 | 550.0 | 400.0 |
| | 60 | 1.782 | 4 | | | | | | 550.0 | 1100.0 | 800.0 |
| ROI | *4 | 9.504 | 16 | 8 | *3 | *3 | 3472 | *4 | 108.5 | 217.0 | 157.8 |
| | *4 | 4.752 | 8 | | | | 2480 | | 155.0 | 310.0 | 225.5 |
| | *4 | 2.376 | 4 | | | | 2304 | | 288.0 | 576.0 | 418.9 |
| | *4 | 9.504 | 16 | 10 | | | 3136 | | 122.5 | 245.0 | 178.2 |
| | *4 | 4.752 | 8 | | | | 2432 | | 190.0 | 380.0 | 276.4 |
| | *4 | 2.376 | 4 | | | | 2272 | | 355.0 | 710.0 | 516.4 |
| | *4 | 9.504 | 16 | 12 | | | 4224 | | 198.0 | 396.0 | 288.0 |
| | *4 | 4.752 | 8 | | | | 2368 | | 222.0 | 444.0 | 322.9 |
| | *4 | 2.376 | 4 | | | | 2256 | | 423.0 | 846.0 | 615.3 |

*1 The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.
Example) In All-pixel 216.2 [frame/s] mode: 9.504 [Gbps] / 16 = 594 [Mbps]

*2 For the setting value to register HMAX / VMAX, see the section of each drive mode settings

*3 Designated cropping area (ROI)

*4 See the section of “ROI mode”

FREQ(CID = 02h, Address = 1Bh, [1:0]) = 1h

| Drive mode | Frame rate [frame/s] | Data rate [Gbps] | Serial LVDS ch*1 | A/D conversion | Number of recording pixels | | Total number of pixels*2 | | Number of INCK in 1H | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | H | V | H | V | INCK: 37.125 MHz | INCK: 74.25 MHz | INCK: 54 MHz |
| All pixel | 145.7 | 4.752 | 16 | 8 | 2048 | 1536 | 2576 | 1582 | 161.0 | 322.0 | 234.2 |
| | 79.8 | 2.376 | 8 | | | | 2352 | | 294.0 | 588.0 | 427.6 |
| | 41.9 | 1.188 | 4 | | | | 2240 | | 560.0 | 1120.0 | 814.5 |
| | 120.3 | 4.752 | 16 | 10 | | | 2496 | | 195.0 | 390.0 | 283.6 |
| | 64.7 | 2.376 | 8 | | | | 2320 | | 362.5 | 725.0 | 527.3 |
| | 33.7 | 1.188 | 4 | | | | 2224 | | 695.0 | 1390.0 | 1010.9 |
| | 102.9 | 4.752 | 16 | 12 | | | 2432 | | 228.0 | 456.0 | 331.6 |
| | 54.7 | 2.376 | 8 | | | | 2288 | | 429.0 | 858.0 | 624.0 |
| | 28.3 | 1.188 | 4 | | | | 2208 | | 828.0 | 1656.0 | 1204.4 |
| All pixel (Vertical / Horizontal 1/2 subsampling) | 420.4 | 4.752 | 16 | 8 | 1024 | 768 | 1744 | 810 | 109.0 | 218.0 | 158.5 |
| | 276.1 | 2.376 | 8 | | | | 1328 | | 166.0 | 332.0 | 241.5 |
| | 150.7 | 1.188 | 4 | | | | 1216 | | 304.0 | 608.0 | 442.2 |
| | 374.1 | 4.752 | 16 | 10 | | | 1568 | | 122.5 | 245.0 | 178.2 |
| | 229.1 | 2.376 | 8 | | | | 1280 | | 200.0 | 400.0 | 290.9 |
| | 122.2 | 1.188 | 4 | | | | 1200 | | 375.0 | 750.0 | 545.5 |
| | 231.4 | 4.752 | 16 | 12 | | | 2112 | | 198.0 | 396.0 | 288.0 |
| | 195.8 | 2.376 | 8 | | | | 1248 | | 234.0 | 468.0 | 340.4 |
| | 103.2 | 1.188 | 4 | | | | 1184 | | 444.0 | 888.0 | 645.8 |
| HD1080p | 60 | 1.782 | 8 | 10 | 1920 | 1080 | 2640 | 1125 | 550.0 | 1100.0 | 800.0 |
| | 30 | 0.891 | 4 | | | | | | 1100.0 | 2200.0 | 1600.0 |
| | 60 | 1.782 | 8 | 12 | | | 2200 | | 550.0 | 1100.0 | 800.0 |
| | 30 | 0.891 | 4 | | | | | | 1100.0 | 2200.0 | 1600.0 |
| ROI | *4 | 4.752 | 16 | 8 | *3 | *3 | 2576 | *4 | 161.0 | 322.0 | 234.2 |
| | *4 | 2.376 | 8 | | | | 2352 | | 294.0 | 588.0 | 427.6 |
| | *4 | 1.188 | 4 | | | | 2240 | | 560.0 | 1120.0 | 814.5 |
| | *4 | 4.752 | 16 | 10 | | | 2496 | | 195.0 | 390.0 | 283.6 |
| | *4 | 2.376 | 8 | | | | 2320 | | 362.5 | 725.0 | 527.3 |
| | *4 | 1.188 | 4 | | | | 2224 | | 695.0 | 1390.0 | 1010.9 |
| | *4 | 4.752 | 16 | 12 | | | 2432 | | 228.0 | 456.0 | 331.6 |
| | *4 | 2.376 | 8 | | | | 2288 | | 429.0 | 858.0 | 624.0 |
| | *4 | 1.188 | 4 | | | | 2208 | | 828.0 | 1656.0 | 1204.4 |

*1 The data rate of each output channel is value that is obtained by total data rate divided by the number of channels.
Example) In All-pixel 145.7 [frame/s] mode: 4.752 [Gbps] / 16 = 297 [Mbps]

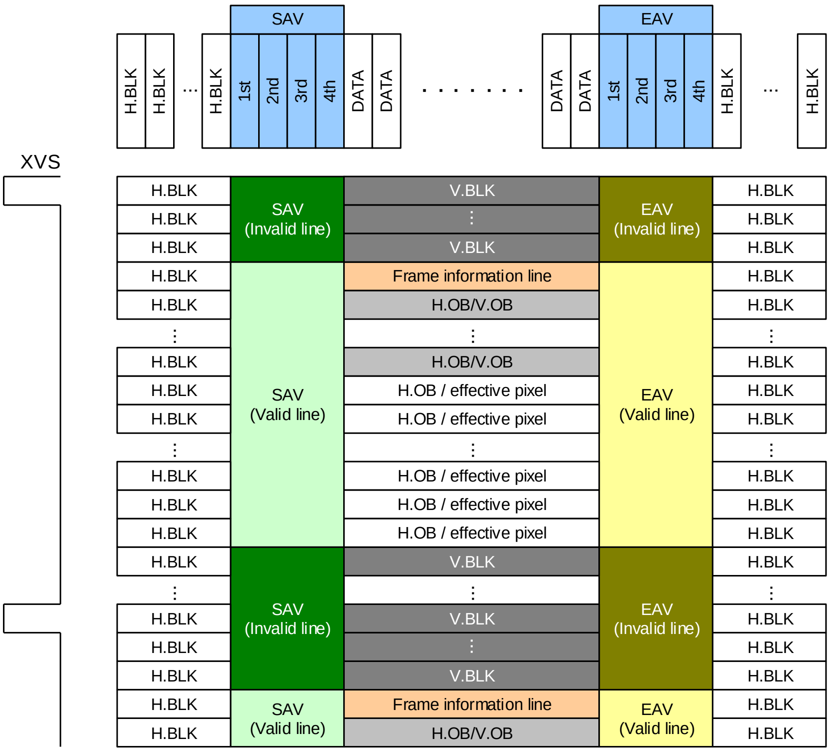
*2 For the setting value to register HMAX / VMAX, see the section of each drive mode settings

*3 Designated cropping area (ROI)

*4 See the section of “ROI mode”

## Sync code

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



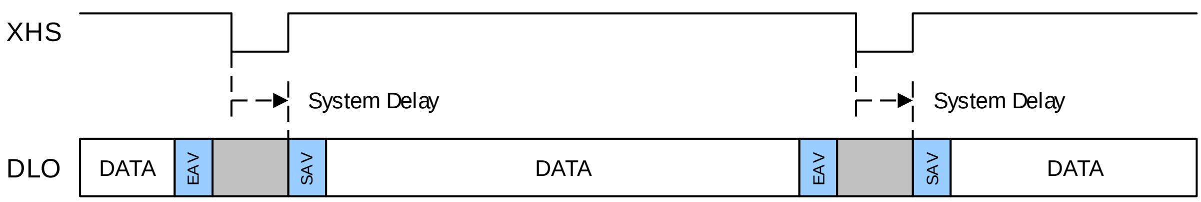

Sync Code Output Timing

### List of Sync Code

| Sync code | 1st code | | | 2nd code | | | 3rd code | | | 4th code | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 8 bit | 10 bit | 12 bit | 8 bit | 10 bit | 12 bit | 8 bit | 10 bit | 12 bit | 8 bit | 10 bit | 12 bit |
| SAV (Valid line) | FFh | 3FFh | FFFh | 00h | 000h | 000h | 00h | 000h | 000h | 80h | 200h | 800h |
| EAV (Valid line) | FFh | 3FFh | FFFh | 00h | 000h | 000h | 00h | 000h | 000h | 9Dh | 274h | 9D0h |
| SAV (Invalid line) | FFh | 3FFh | FFFh | 00h | 000h | 000h | 00h | 000h | 000h | ABh | 2ACh | AB0h |
| EAV (Invalid line) | FFh | 3FFh | FFFh | 00h | 000h | 000h | 00h | 000h | 000h | B6h | 2D8h | B60h |

### Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



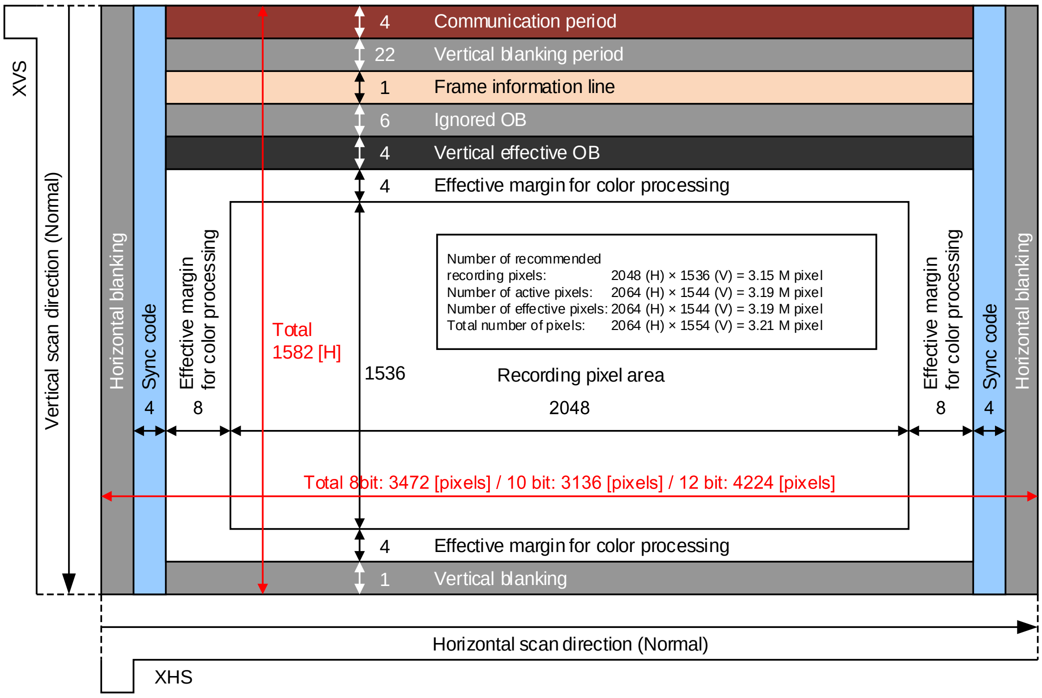
# Image Data Output Format

## All-pixel scan

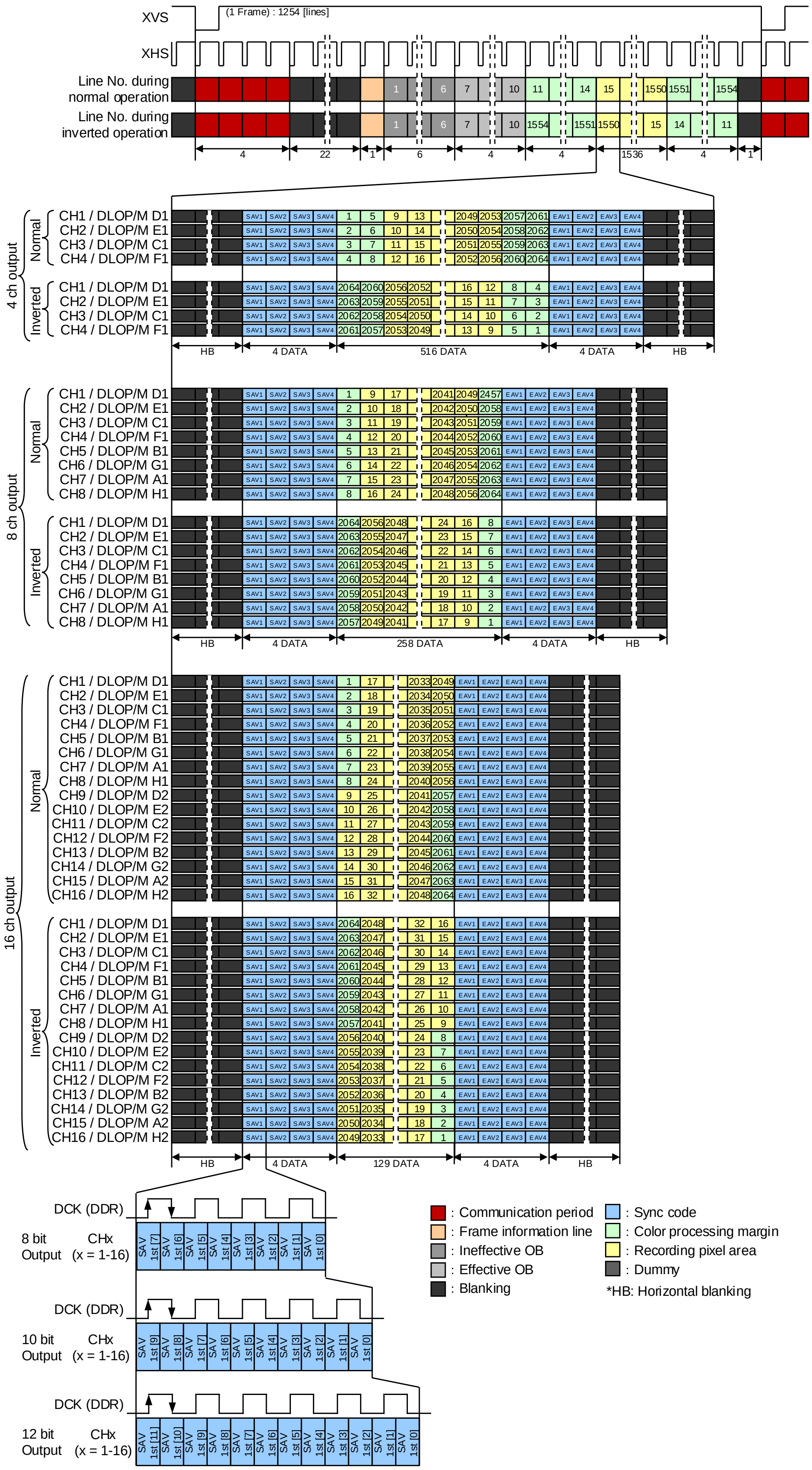
### Register List of All-pixel scan mode

Please refer to the register map for the register that has not been described.

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | 216.2 [frame/s] | 151.4 [frame/s] | 81.4 [frame/s] | 191.5 [frame/s] | 123.5 [frame/s] | 66.1 [frame/s] | 118.5 [frame/s] | 105.7 [frame/s] | 55.4 [frame/s] | FREQ = 0h |
| | | | | 145.7 [frame/s] | 79.8 [frame/s] | 41.9 [frame/s] | 120.3 [frame/s] | 64.7 [frame/s] | 33.7 [frame/s] | 102.9 [frame/s] | 54.7 [frame/s] | 28.3 [frame/s] | FREQ = 1h |
| Chip ID = 02h | | | | | | | | | | | | | |
| 05h | [7:4] | STBLVDS | 0h | 0h | N/A | N/A | 0h | N/A | N/A | 0h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 2h | N/A | N/A | 2h | N/A | N/A | 2h | 4 ch LVDS |
| 0Ch | [1:0] | ADBIT | 0h | 2h | | | 0h | | | 1h | | | 0: 10 bit<br>1: 12 bit<br>2: 8bit |
| 0Dh | [3:0] | WINMODE | 0h | 0h | | | | | | | | | All-pixel mode |
| 0Dh | [4] | HMODE | 0 | 0 | | | | | | | | | All-pixel |
| 10h | [7:0] | VMAX | 82Eh | 62Eh | | | | | | | | | 1582 line |
| 11h | [7:0] | | | | | | | | | | | | |
| 12h | [3:0] | | | | | | | | | | | | |
| 14h | [7:0] | HMAX | 15Eh | 0D9h | 136h | 240h | 0F5h | 17Ch | 2C6h | 18Ch | 1BCh | 34Eh | FREQ = 0h |
| 15h | [7:0] | | | 142h | 24Ch | 460h | 186h | 2D5h | 56Eh | 1C8h | 35Ah | 678h | FREQ = 1h |
| 16h | [1:0] | ODBIT | 0h | 2h | | | 0h | | | 1h | | | 0: 10 bit<br>1: 12 bit<br>2: 8bit |
| 19h | [0] | CKSEL | 0 | 0 | | | | | | | | | |
| 1Bh | [1:0] | FREQ | 0h | 0h / 1h | | | | | | | | | |
| 1Ch | [7:4] | OPORTSEL | 9h | 9h | N/A | N/A | 9h | N/A | N/A | 9h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 3h | N/A | N/A | 3h | N/A | N/A | 3h | 4 ch LVDS |
| 89h | [7:0] | INCKSEL0 | 20h | INCK = 37.125 MHz : 10h<br>INCK = 54 MHz : 16h<br>INCK = 74.25 MHz : 10h | | | | | | | | | |
| 8Ah | [7:0] | INCKSEL1 | 00h | INCK = 37.125 MHz: 02h<br>INCK = 54 MHz : 00h<br>INCK = 74.25 MHz: 00h | | | | | | | | | |
| 8Bh | [7:0] | INCKSEL2 | 20h | INCK = 37.125 MHz : 10h<br>INCK = 54 MHz : 16h<br>INCK = 74.25 MHz : 10h | | | | | | | | | |
| 8Ch | [7:0] | INCKSEL3 | 00h | INCK = 37.125 MHz: 02h<br>INCK = 54 MHz : 00h<br>INCK = 74.25 MHz: 00h | | | | | | | | | |
| 9Eh | [7:0] | GTWAIT | 0Ah | 0Ah | | | | | | | | | |
| A0h | [7:0] | GSDLY | 08h | 08h | | | | | | | | | |
| Chip ID = 04h | | | | | | | | | | | | | |
| 54h | [7:0] | BLKLEVEL | 03Ch | 00Fh | | | 03Ch | | | 0F0h | | | Recommended value |
| 55h | [3:0] | | | | | | | | | | | | |




Pixel Array Image Drawing in All-pixel scan Mode (FREQ=0, 16ch LVDS)



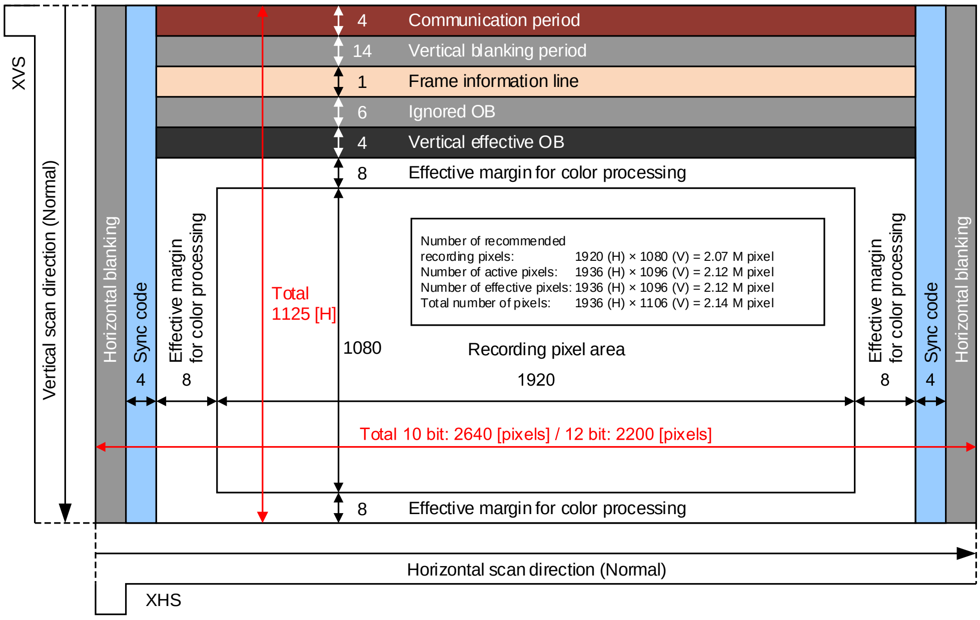

Drive Timing Chart for Serial Output in All-pixel Scan Mode

## 1080p-Full HD mode

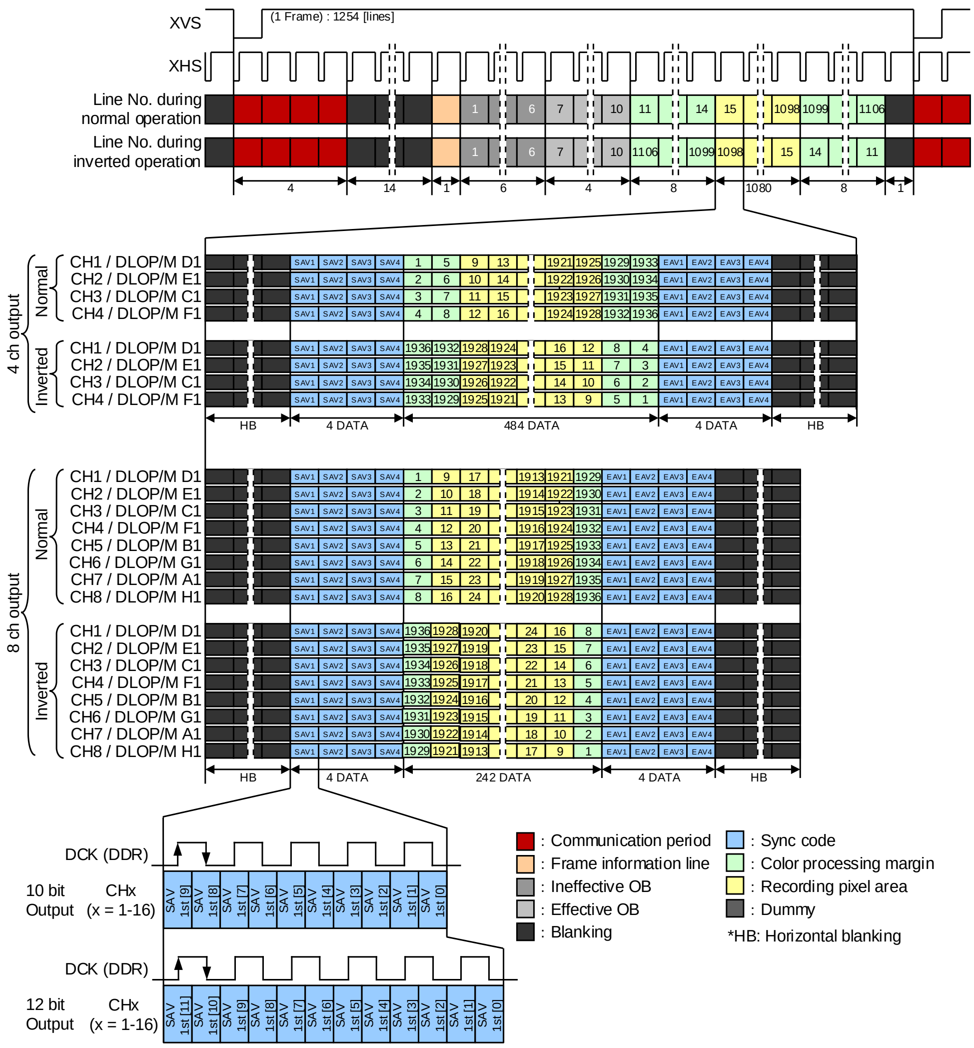
### Register List of 1080p-Full HD mode

Please refer to the register map for the register that has not been described.

| Address | bit | Register name | Initial Value | Setting value | | | | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | AD = 10 bit | | AD = 12 bit | | |
| | | | | 120 [frame/s] | 60 [frame/s] | 120 [frame/s] | 60 [frame/s] | FREQ = 0h |
| | | | | 60 [frame/s] | 30 [frame/s] | 60 [frame/s] | 30 [frame/s] | FREQ = 1h |
| Chip ID = 02h | | | | | | | | |
| 05h | [7:4] | STBLVDS | 0h | 1h | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | 2h | N/A | 2h | 4 ch LVDS |
| 0Ch | [1:0] | ADBIT | 0h | 0h | | 1h | | 0: 10 bit<br>1: 12 bit |
| 0Dh | [3:0] | WINMODE | 0h | Ch | | | | 1080p-FULL HD mode |
| 0Dh | [4] | HMODE | 0 | 0 | | | | All-pixel |
| 10h | [7:0] | VMAX | 82Eh | 465h | | | | 1125 line |
| 11h | [7:0] | | | | | | | |
| 12h | [3:0] | | | | | | | |
| 14h | [7:0] | HMAX | 15Eh | 226h | 44Ch | 226h | 44Ch | FREQ = 0h |
| 15h | [7:0] | | | 44Ch | 898h | 44Ch | 898h | FREQ = 1h |
| 16h | [1:0] | ODBIT | 0h | 0h | | 1h | | 0: 10 bit<br>1: 12 bit |
| 19h | [0] | CKSEL | 0 | 1 | | | | |
| 1Bh | [1:0] | FREQ | 0h | 0h / 1h | | | | |
| 1Ch | [7:4] | OPORTSEL | 9h | 1h | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | 3h | N/A | 3h | 4 ch LVDS |
| 89h | [7:0] | INCKSEL0 | 20h | INCK = 37.125 MHz : 18h<br>INCK = 74.25 MHz : 0Ch | | | | |
| 8Ah | [7:0] | INCKSEL1 | 00h | INCK = 37.125 MHz: 00h<br>INCK = 74.25 MHz: 00h | | | | |
| 8Bh | [7:0] | INCKSEL2 | 20h | INCK = 37.125 MHz : 10h<br>INCK = 74.25 MHz : 10h | | | | |
| 8Ch | [7:0] | INCKSEL3 | 00h | INCK = 37.125 MHz: 02h<br>INCK = 74.25 MHz: 00h | | | | |
| 9Eh | [7:0] | GTWAIT | 0Ah | 06h | | | | |
| A0h | [7:0] | GSDLY | 08h | 04h | | | | |
| Chip ID = 04h | | | | | | | | |
| 54h | [7:0] | BLKLEVEL | 03Ch | 03Ch | | 0F0h | | Recommended value |
| 55h | [3:0] | | | | | | | |




Pixel Array Image Drawing in 1080p-Full HD Mode (FREQ=0, 8ch LVDS)




Drive Timing Chart for Serial Output in 1080p-Full HD Mode

## ROI mode

This Sensor has ROI function that signals are cut out and read out in multi arbitrary positions.
Cropping position can set maximum 64 areas that specified by horizontal 8 points and vertical 8 points, regarding effective pixel start position as origin (0, 0) in all pixel scan mode. Cropping is available from All-pixel scan mode and horizontal period are fixed to the value for this mode.
These cropped areas by horizontal cropping setting (ROI (1, y) to ROI (8, y)) are output with left justified and that extends the horizontal blanking period. In vertical cropping area (ROI (x, 1) to ROI (x, 8)), the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.
One invalid frame is generated when the ROI area changing size or cropping address.
ROI image is shown in the figure below.
In case of Vertical / Horizontal 1/2 subsampling mode, IMX252 doesn't support ROI mode.

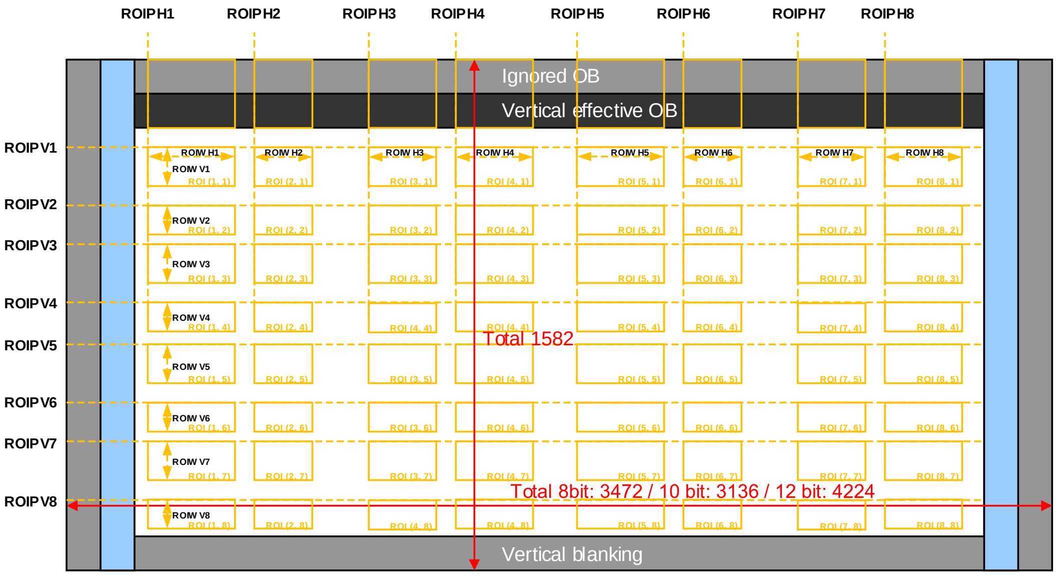
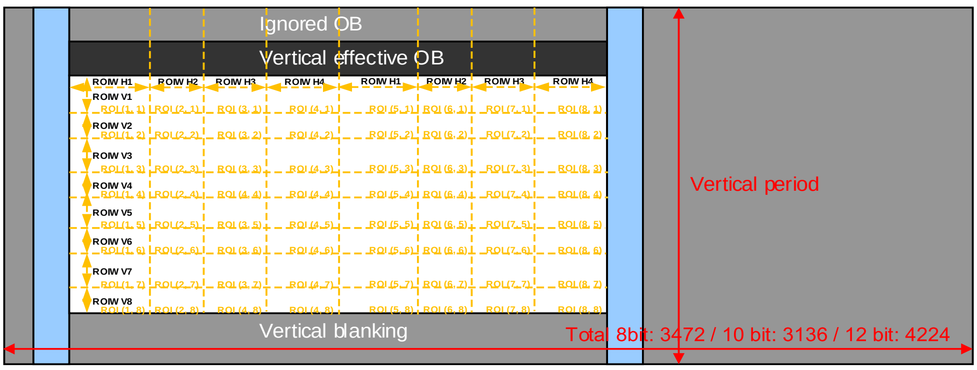



Image Drawing of Designated Areas in ROI Mode (FREQ=0, 16ch LVDS)




Details of Image Drawing (FREQ=0, 16ch L VDS)

## Register List of ROI mode

Please set All-pixel scan mode to the settings other than the following.

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | *1 [frame/s] | *2 [frame/s] | *3 [frame/s] | *4 [frame/s] | *5 [frame/s] | *6 [frame/s] | *7 [frame/s] | *8 [frame/s] | *9 [frame/s] | |
| Chip ID = 02h | | | | | | | | | | | | | |
| 05h | [7:4] | STBLVDS | 0h | 0h | N/A | N/A | 0h | N/A | N/A | 0h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 2h | N/A | N/A | 2h | N/A | N/A | 2h | 4 ch LVDS |
| 0Ch | [1:0] | ADBIT | 0h | 2h | | | 0h | | | 1h | | | 0: 10 bit<br>1: 12 bit<br>2: 8bit |
| 0Dh | [3:0] | WINMODE | 0h | 8h | | | | | | | | | All-pixel mode |
| 0Dh | [4] | HMODE | 0 | 0 | | | | | | | | | All-pixel |
| 10h | [7:0] | VMAX | 82Eh | *1 | *2 | *3 | *4 | *5 | *6 | *7 | *8 | *9 | |
| 11h | [7:0] | | | | | | | | | | | | |
| 12h | [3:0] | | | | | | | | | | | | |
| 14h | [7:0] | HMAX | 15Eh | 0D9h | 136h | 240h | 0F5h | 17Ch | 2C6h | 18Ch | 1BCh | 34Eh | FREQ = 0h |
| 15h | [7:0] | | | 142h | 24Ch | 460h | 186h | 2D5h | 56Eh | 1C8h | 35Ah | 678h | FREQ = 1h |
| 16h | [1:0] | ODBIT | 0h | 2h | | | 0h | | | 1h | | | 0: 10 bit<br>1: 12 bit<br>2: 8bit |
| 19h | [0] | CKSEL | 0 | 0 | | | | | | | | | |
| 1Bh | [1:0] | FREQ | 0h | 0h / 1h | | | | | | | | | |
| 1Ch | [7:4] | OPORTSEL | 9h | 9h | N/A | N/A | 9h | N/A | N/A | 9h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 3h | N/A | N/A | 3h | N/A | N/A | 3h | 4 ch LVDS |
| 89h | [7:0] | INCKSEL0 | 20h | INCK = 37.125 MHz : 10h<br>INCK = 54 MHz : 16h<br>INCK = 74.25 MHz : 10h | | | | | | | | | |
| 8Ah | [7:0] | INCKSEL1 | 00h | INCK = 37.125 MHz: 02h<br>INCK = 54 MHz : 00h<br>INCK = 74.25 MHz: 00h | | | | | | | | | |
| 8Bh | [7:0] | INCKSEL2 | 20h | INCK = 37.125 MHz : 10h<br>INCK = 54 MHz : 16h<br>INCK = 74.25 MHz : 10h | | | | | | | | | |
| 8Ch | [7:0] | INCKSEL3 | 00h | INCK = 37.125 MHz: 02h<br>INCK = 54 MHz : 00h<br>INCK = 74.25 MHz: 00h | | | | | | | | | |
| 9Eh | [7:0] | GTWAIT | 0Ah | 0Ah | | | | | | | | | |
| A0h | [7:0] | GSDLY | 08h | 08h | | | | | | | | | |
| Chip ID = 04h | | | | | | | | | | | | | |
| 54h | [7:0] | BLKLEVEL | 03Ch | 00Fh | | | 03Ch | | | 0F0h | | | Recommended value |
| 55h | [3:0] | | | | | | | | | | | | |

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | *1 [frame/s] | *2 [frame/s] | *3 [frame/s] | *4 [frame/s] | *5 [frame/s] | *6 [frame/s] | *7 [frame/s] | *8 [frame/s] | *9 [frame/s] | |
| Chip ID = 05h | | | | | | | | | | | | | |
| 00h | [0] | FID0_ROIH1ON | 0 | The horizontal setting of FID0 ROI area (1, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [1] | FID0_ROIV1ON | 0 | The vertical setting of FID0 ROI area (x, 1) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [2] | FID0_ROIH2ON | 0 | The horizontal setting of FID0 ROI area (2, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [3] | FID0_ROIV2ON | 0 | The vertical setting of FID0 ROI area (x, 2) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [4] | FID0_ROIH3ON | 0 | The horizontal setting of FID0 ROI area (3, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [5] | FID0_ROIV3ON | 0 | The vertical setting of FID0 ROI area (x, 3) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [6] | FID0_ROIH4ON | 0 | The horizontal setting of FID0 ROI area (4, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [7] | FID0_ROIV4ON | 0 | The vertical setting of FID0 ROI area (x, 4) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| 02h | [0] | FID0_ROIH5ON | 0 | The horizontal setting of FID0 ROI area (5, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [1] | FID0_ROIV5ON | 0 | The vertical setting of FID0 ROI area (x, 5) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [2] | FID0_ROIH6ON | 0 | The horizontal setting of FID0 ROI area (6, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [3] | FID0_ROIV6ON | 0 | The vertical setting of FID0 ROI area (x, 6) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [4] | FID0_ROIH7ON | 0 | The horizontal setting of FID0 ROI area (7, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [5] | FID0_ROIV7ON | 0 | The vertical setting of FID0 ROI area (x, 7) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [6] | FID0_ROIH8ON | 0 | The horizontal setting of FID0 ROI area (8, y) (y = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| | [7] | FID0_ROIV8ON | 0 | The vertical setting of FID0 ROI area (x, 8) (x = 1 to 8)<br>0: Disable 1: Enable | | | | | | | | | |
| 10h | [7:0] | FID0_ROIPH1 | 0000h | Designation of horizontal cropping position for FID0 on area (1, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 11h | [4:0] | | | | | | | | | | | | |
| 12h | [7:0] | FID0_ROIPV1 | 000h | Designation of vertical cropping position for FID0 on area (x, 1) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 13h | [3:0] | | | | | | | | | | | | |
| 14h | [7:0] | FID0_ROIWH1 | 0000h | Designation of horizontal cropping size for FID0 on area (1, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 15h | [4:0] | | | | | | | | | | | | |
| 16h | [7:0] | FID0_ROIWV1 | 000h | Designation of vertical cropping size for FID0 on area (x, 1) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 17h | [3:0] | | | | | | | | | | | | |
| 18h | [7:0] | FID0_ROIPH2 | 0000h | Designation of horizontal cropping position for FID0 on area (2, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 19h | [4:0] | | | | | | | | | | | | |
| 1Ah | [7:0] | FID0_ROIPV2 | 000h | Designation of vertical cropping position for FID0 on area (x, 2) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 1Bh | [3:0] | | | | | | | | | | | | |
| 1Ch | [7:0] | FID0_ROIWH2 | 0000h | Designation of horizontal cropping size for FID0 on area (2, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 1Dh | [4:0] | | | | | | | | | | | | |
| 1Eh | [7:0] | FID0_ROIWV2 | 000h | Designation of vertical cropping size for FID0 on area (x, 2) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 1Fh | [3:0] | | | | | | | | | | | | |
| 20h | [7:0] | FID0_ROIPH3 | 0000h | Designation of horizontal cropping position for FID0 on area (3, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 21h | [4:0] | | | | | | | | | | | | |
| 22h | [7:0] | FID0_ROIPV3 | 000h | Designation of vertical cropping position for FID0 on area (x, 3) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 23h | [3:0] | | | | | | | | | | | | |
| 24h | [7:0] | FID0_ROIWH3 | 0000h | Designation of horizontal cropping size for FID0 on area (3, y) (y = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 25h | [4:0] | | | | | | | | | | | | |
| 26h | [7:0] | FID0_ROIWV3 | 000h | Designation of vertical cropping size for FID0 on area (x, 3) (x = 1 to 8)<br>*Set the value of multiple of 4 | | | | | | | | | |
| 27h | [3:0] | | | | | | | | | | | | |

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | *1 [frame/s] | *2 [frame/s] | *3 [frame/s] | *4 [frame/s] | *5 [frame/s] | *6 [frame/s] | *7 [frame/s] | *8 [frame/s] | *9 [frame/s] | |
| 28h | [7:0] | FID0_ROIPH4 | 0000h | Designation of horizontal cropping position for FID0 on area (4, y) (y = 1 to 8) | | | | | | | | | |
| 29h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 2Ah | [7:0] | FID0_ROIPV4 | 000h | Designation of vertical cropping position for FID0 on area (x, 4) (x = 1 to 8) | | | | | | | | | |
| 2Bh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 2Ch | [7:0] | FID0_ROIWH4 | 0000h | Designation of horizontal cropping size for FID0 on area (4, y) (y = 1 to 8) | | | | | | | | | |
| 2Dh | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 2Eh | [7:0] | FID0_ROIWV4 | 000h | Designation of vertical cropping size for FID0 on area (x, 4) (x = 1 to 8) | | | | | | | | | |
| 2Fh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 30h | [7:0] | FID0_ROIPH5 | 0000h | Designation of horizontal cropping position for FID0 on area (5, y) (y = 1 to 8) | | | | | | | | | |
| 31h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 32h | [7:0] | FID0_ROIPV5 | 000h | Designation of vertical cropping position for FID0 on area (x, 5) (x = 1 to 8) | | | | | | | | | |
| 33h | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 34h | [7:0] | FID0_ROIWH5 | 0000h | Designation of horizontal cropping size for FID0 on area (5, y) (y = 1 to 8) | | | | | | | | | |
| 35h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 36h | [7:0] | FID0_ROIWV5 | 000h | Designation of vertical cropping size for FID0 on area (x, 5) (x = 1 to 8) | | | | | | | | | |
| 37h | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 38h | [7:0] | FID0_ROIPH6 | 0000h | Designation of horizontal cropping position for FID0 on area (6, y) (y = 1 to 8) | | | | | | | | | |
| 39h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 3Ah | [7:0] | FID0_ROIPV6 | 000h | Designation of vertical cropping position for FID0 on area (x, 6) (x = 1 to 8) | | | | | | | | | |
| 3Bh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 3Ch | [7:0] | FID0_ROIWH6 | 0000h | Designation of horizontal cropping size for FID0 on area (6, y) (y = 1 to 8) | | | | | | | | | |
| 3Dh | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 3Eh | [7:0] | FID0_ROIWV6 | 000h | Designation of vertical cropping size for FID0 on area (x, 6) (x = 1 to 8) | | | | | | | | | |
| 3Fh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 40h | [7:0] | FID0_ROIPH7 | 0000h | Designation of horizontal cropping position for FID0 on area (7, y) (y = 1 to 8) | | | | | | | | | |
| 41h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 42h | [7:0] | FID0_ROIPV7 | 000h | Designation of vertical cropping position for FID0 on area (x, 7) (x = 1 to 8) | | | | | | | | | |
| 43h | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 44h | [7:0] | FID0_ROIWH7 | 0000h | Designation of horizontal cropping size for FID0 on area (7, y) (y = 1 to 8) | | | | | | | | | |
| 45h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 46h | [7:0] | FID0_ROIWV7 | 000h | Designation of vertical cropping size for FID0 on area (x, 7) (x = 1 to 8) | | | | | | | | | |
| 47h | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 48h | [7:0] | FID0_ROIPH8 | 0000h | Designation of horizontal cropping position for FID0 on area (8, y) (y = 1 to 8) | | | | | | | | | |
| 49h | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 4Ah | [7:0] | ROIPV8 | 000h | Designation of vertical cropping position for FID0 on area (x, 8) (x = 1 to 8) | | | | | | | | | |
| 4Bh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 4Ch | [7:0] | FID0_ROIWH8 | 0000h | Designation of horizontal cropping size for FID0 on area (8, y) (y = 1 to 8) | | | | | | | | | |
| 4Dh | [4:0] | | | *Set the value of multiple of 4 | | | | | | | | | |
| 4Eh | [7:0] | FID0_ROIWV8 | 000h | Designation of vertical cropping size for FID0 on area (x, 8) (x = 1 to 8) | | | | | | | | | |
| 4Fh | [3:0] | | | *Set the value of multiple of 4 | | | | | | | | | |

**Restrictions on ROI mode**

The register settings should satisfy following conditions:

* Do not designate area like be overlap.
  ROIPH1 + ROIWH1 < ROIPH2
  ROIPH2 + ROIWH2 < ROIPH3
  ROIPH3 + ROIWH3 < ROIPH4
…
  ROIPH8 + ROIWH8 < 2464d

  ROIPV1 + ROIWV1 < ROIPV2
  ROIPV2 + ROIWV2 < ROIPV3
  ROIPV3 + ROIWV3 < ROIPV4
…
  ROIPV8 + ROIWV8 < 2056d

* Set the horizontal and vertical setting in multiple of 4

* Minimum width of the window is as below.
 10 / 12bit mode
  ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≧ 258d
 8bit mode
  ROIWH1 + ROIWH2 + ROIWH3 + …. + ROIWH8 ≧ 516d
 8 / 10 / 12 bit mode
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 ≧ 4d

**Frame rate on ROI mode**

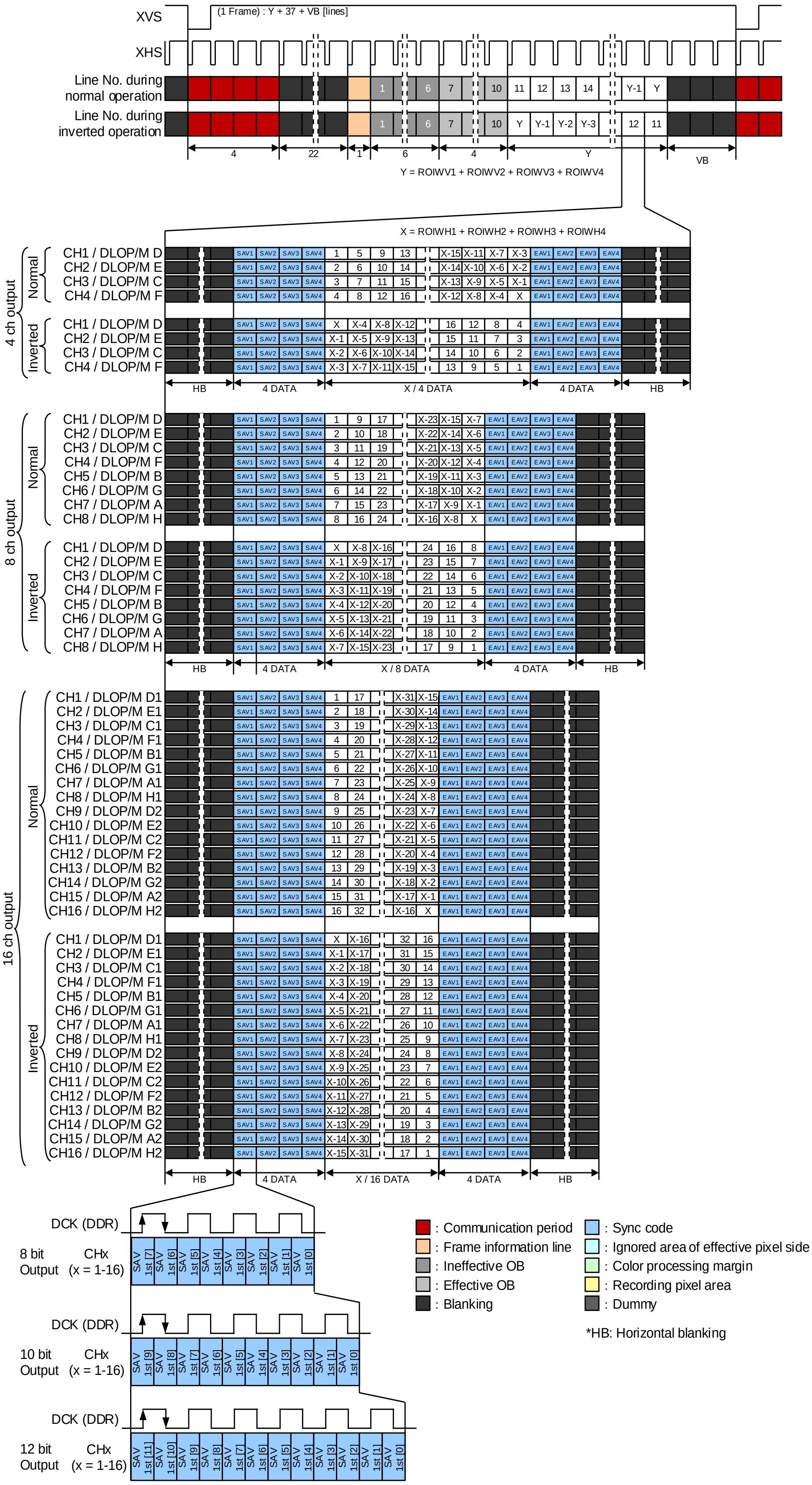
Frame rate [ frame/s ] = 1 / ((“Number of lines per frame” or VMAX ) × ( 1 H period ))

* Number of lines per frame or VMAX = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + 38
* 1 period: Change according to the data rate settings and the number of LVDS channels.
  Calculate by number of INCK in 1 H and the period of INCK.

The example of ROI setting is shown below.
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 600
  ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 = 4 (minimum value)

Frame rate List of each setting

| Register settings No. in register list | 1 H period [µs] | | Frame rate [frame/s] | | | |
|---|---|---|---|---|---|---|
| | FREQ 0h | FREQ 1h | Total number of ROI: 600 [line] | | Total number of ROI: 4 [line] | |
| | | | FREQ=0h | FREQ=1h | FREQ=0h | FREQ=1h |
| *1 | 2.923 | 4.337 | 537.1 | 361.9 | 8345.5 | 5624.1 |
| *2 | 4.175 | 7.919 | 376.0 | 198.2 | 5841.8 | 3079.8 |
| *3 | 7.758 | 15.084 | 202.3 | 104.0 | 3144.0 | 1616.9 |
| *4 | 3.300 | 5.253 | 475.7 | 298.8 | 7391.7 | 4643.5 |
| *5 | 5.118 | 9.764 | 306.7 | 160.7 | 4765.7 | 2497.9 |
| *6 | 9.562 | 18.721 | 164.1 | 83.8 | 2550.6 | 1302.8 |
| *7 | 5.333 | 6.141 | 294.3 | 255.6 | 4573.1 | 3971.4 |
| *8 | 5.980 | 11.556 | 262.5 | 135.8 | 4078.7 | 2110.6 |
| *9 | 11.394 | 22.303 | 137.7 | 70.3 | 2140.6 | 1093.5 |




Drive Timing Chart for Serial Output in ROI Mode

### Vertical / Horizontal 1/2 Subsampling mode

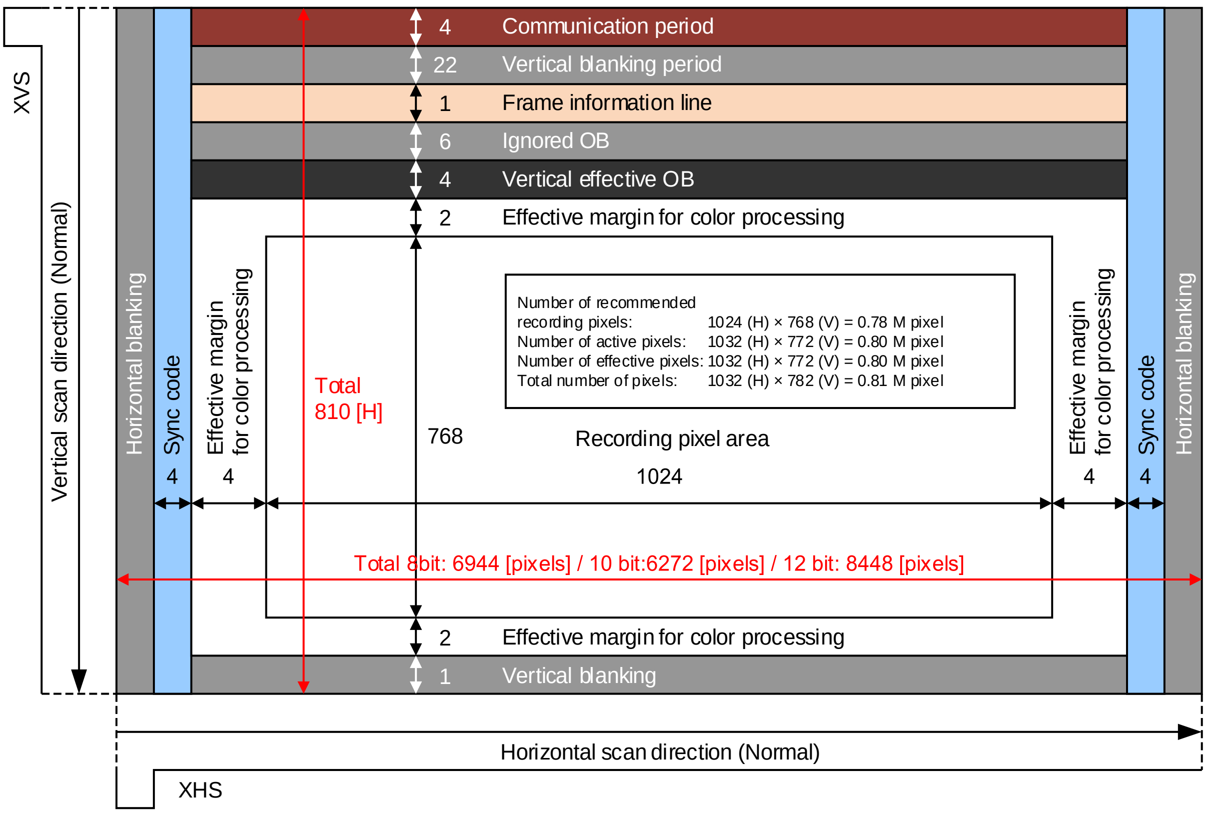
V direction and H direction must be set in this mode.

Register List of Vertical / Horizontal 1/2 subsampling mode

**Chip ID = 02 (Write : Chip ID = 02h, Read : Chip ID = 82h, $I^2C$ : 30**h)**

Please set All-pixel scan mode to the settings other than the following.

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | 442.4 [frame/s] | 420.4 [frame/s] | 286.4 [frame/s] | 374.1 [frame/s] | 374.1 [frame/s] | 235.0 [frame/s] | 231.4 [frame/s] | 231.4 [frame/s] | 201.0 [frame/s] | FREQ = 0h |
| | | | | 420.4 [frame/s] | 276.1 [frame/s] | 150.7 [frame/s] | 374.1 [frame/s] | 229.1 [frame/s] | 122.2 [frame/s] | 231.4 [frame/s] | 195.8 [frame/s] | 103.2 [frame/s] | FREQ = 1h |
| Chip ID = 02h | | | | | | | | | | | | | |
| 05h | [7:4] | STBLVDS | 0h | 0h | N/A | N/A | 0h | N/A | N/A | 0h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 2h | N/A | N/A | 2h | N/A | N/A | 2h | 4 ch LVDS |
| 0Dh | [3:0] | WINMODE | 0h | 9h | | | | | | | | | Subsampling mode |
| 0Dh | [4] | HMODE | 0 | 1 | | | | | | | | | Subsampling mode |
| 10h | [7:0] | VMAX | 82Eh | 32Ah | | | | | | | | | 810 line |
| 11h | [7:0] | | | | | | | | | | | | |
| 12h | [3:0] | | | | | | | | | | | | |
| 14h | [7:0] | HMAX | 15Eh | 0D9h | 0DAh | 140h | 0F5h | 0F5h | 186h | 18Ch | 18Ch | 1C8h | FREQ = 0h |
| 15h | [7:0] | | | 0DAh | 14Ch | 260h | 0F5h | 190h | 2EEh | 18Ch | 1D4h | 378h | FREQ = 1h |
| 1Bh | [1:0] | FREQ | 0h | 0h / 1h | | | | | | | | | |
| 1Ch | [7:4] | OPORTSEL | 9h | 9h | N/A | N/A | 9h | N/A | N/A | 9h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 3h | N/A | N/A | 3h | N/A | N/A | 3h | 4 ch LVDS |




Pixel Array Image Drawing in Vertical / Horizontal 1/2 subsampling mode (FREQ=0, 16ch LVDS)

### Vertical 2-pixel FD Binning mode

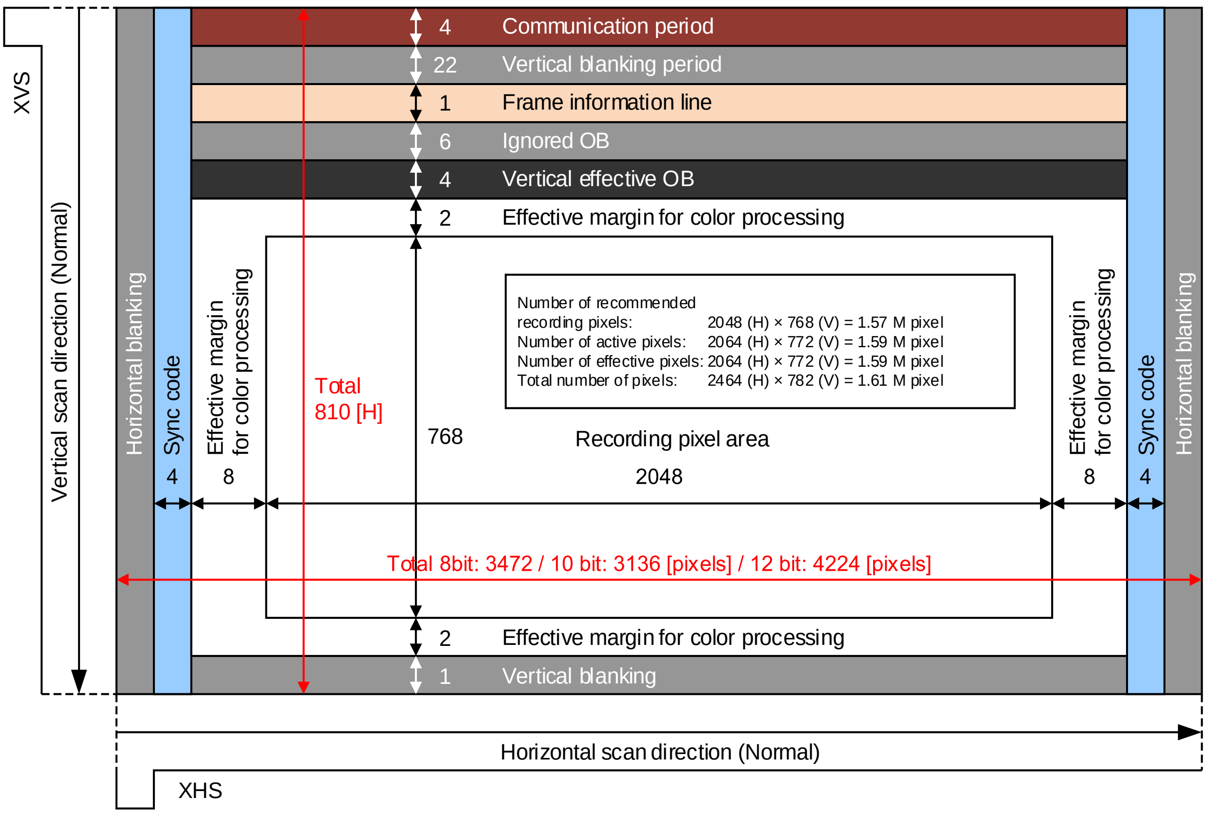
By setting vertical 2-pixel FD binning mode, the frame rate becomes double.

Register List of Vertical 2-pixel FD Binning mode

**Chip ID = 02 (Write : Chip ID = 02h, Read : Chip ID = 82h, $I^2C$ : 30**h)**

Please set All-pixel scan mode to the settings other than the following.

| Address | bit | Register name | Initial Value | Setting value | | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | AD = 8 bit | | | AD = 10 bit | | | AD = 12 bit | | | |
| | | | | 422.4 [frame/s] | 295.7 [frame/s] | 159.1 [frame/s] | 374.1 [frame/s] | 241.2 [frame/s] | 129.1 [frame/s] | 231.4 [frame/s] | 206.4 [frame/s] | 108.3 [frame/s] | FREQ = 0h |
| Chip ID = 02h | | | | | | | | | | | | | |
| 05h | [7:4] | STBLVDS | 0h | 0h | N/A | N/A | 0h | N/A | N/A | 0h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 2h | N/A | N/A | 2h | N/A | N/A | 2h | 4 ch LVDS |
| 0Dh | [3:0] | WINMODE | 0h | Ah | | | | | | | | | Binning mode |
| 10h | [7:0] | VMAX | 82Eh | 32Ah | | | | | | | | | 810 line |
| 11h | [7:0] | | | | | | | | | | | | |
| 12h | [3:0] | | | | | | | | | | | | |
| 14h | [7:0] | HMAX | 15Eh | 0D9h | 136h | 240h | 0F5h | 17Ch | 2C6h | 18Ch | 1BCh | 34Eh | FREQ = 0h |
| 1Bh | [1:0] | FREQ | 0h | 0h | | | | | | | | | |
| 1Ch | [7:4] | OPORTSEL | 9h | 9h | N/A | N/A | 9h | N/A | N/A | 9h | N/A | N/A | 16 ch LVDS |
| | | | | N/A | 1h | N/A | N/A | 1h | N/A | N/A | 1h | N/A | 8 ch LVDS |
| | | | | N/A | N/A | 3h | N/A | N/A | 3h | N/A | N/A | 3h | 4 ch LVDS |




Pixel Array Image Drawing in Vertical 2-pixel FD Binning mode (FREQ=0, 16ch LVDS)

# Description of Various Function

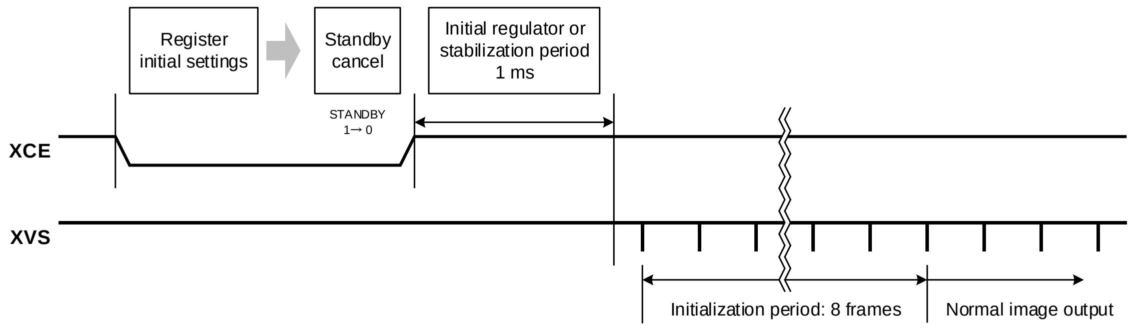
## Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

Register List of Standby setting

| Register | Register details | | | Initial value | Setting value | Remarks |
|---|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | bit | | | |
| STANDBY | 02h | 00h (3000h) | [0] | 1h | 1h: Standby<br>0h: Operating | Register communication is executed even in standby mode. |

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. For details on the sequence of setting and cancel of standby mode, see the sensor setting flow after power on.
After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (1 ms or more).




Sequence from Standby Cancel to Stable Image Output

## Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode.
The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Readout Drive mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of operation mode for details of the section of “Readout Drive Modes”.

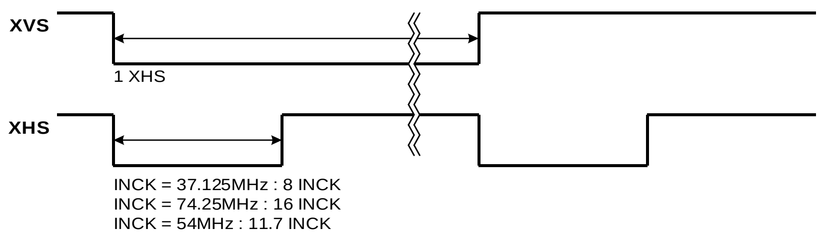
### Pin Processing

| Pin name | Pin processing | Operation mode | Remarks |
|---|---|---|---|
| XMASTER pin | Low fixed | Master mode | High: $OV_{DD}$<br>Low: GND |
| | High fixed | Slave mode | |

### Register List of Slave Mode and Master Mode

| Register | Register details | | | Initial value | Setting value | Remarks |
|---|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | Bit | | | |
| XMSTA | 02h | 0Ah (300Ah) | [0] | 1h | 1h: Master operation ready (Initial value)<br>0h: Master operation start | The master operation starts by setting 0. |
| VMAX [19:0] | | 10h (3010h) | [7:0] | 0082Eh | See the item of each drive mode | Line number per frame designated (Master mode and Slave mode common setting.) |
| | | 11h (3011h) | [7:0] | | | |
| | | 12h (3012h) | [3:0] | | | |
| HMAX [15:0] | | 14h (3014h) | [7:0] | 015Eh | See the item of each drive mode | Clock number per line designated (Master mode and Slave mode common setting.) |
| | | 15h (3015h) | [7:0] | | | |

### XVS / XHS Output Waveform in Master Mode



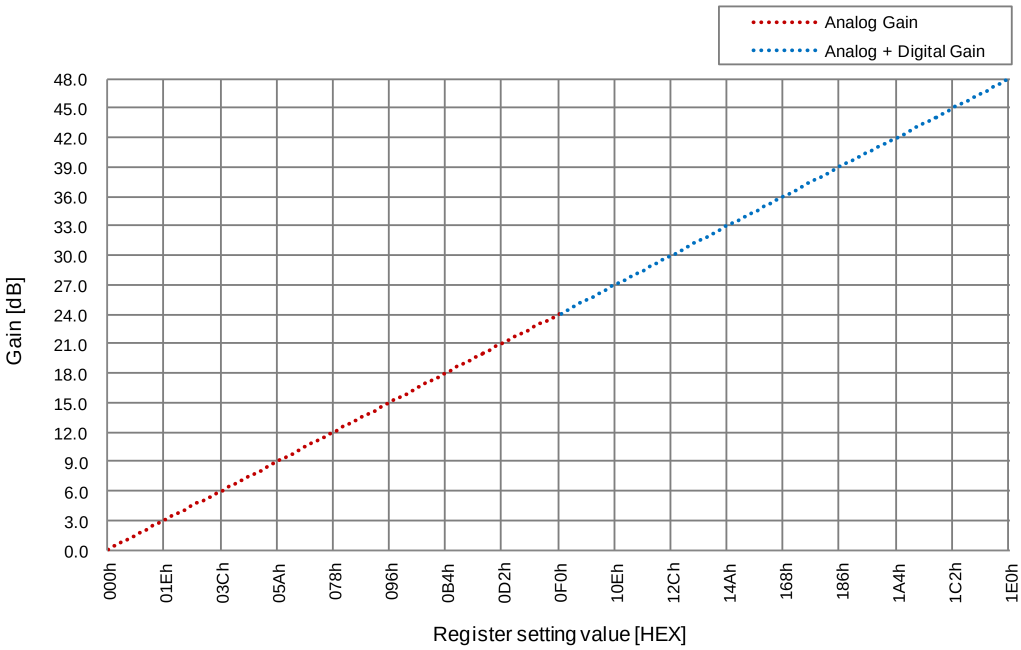
## Gain Adjustment Function

### PGC

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 48 dB by the GAIN [8:0] register setting.
The value which is ten times the gain is set to register.

Example)
When set to 6 dB:

6 × 10 = 60d, GAIN = 03Ch




Register List of Gain setting

| Register | Register details | | | Initial value | Setting value / Setting range | Remarks |
|---|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I²C | bit | | | |
| GAIN [8:0] | 04h | 04h (3204h) | [7:0] | 000h | 000h to 1E0h (0d to 480d) | Setting value: Gain [dB] × 10 |
| | | 05h (3205h) | [0] | | | |

## Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register. When the BLKLEVEL [11:0] setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
8 bit output: 00Fh (15 d)
10 bit output: 03Ch (60 d)
12 bit output: 0F0h (240 d)

Register List of Black level adjustment

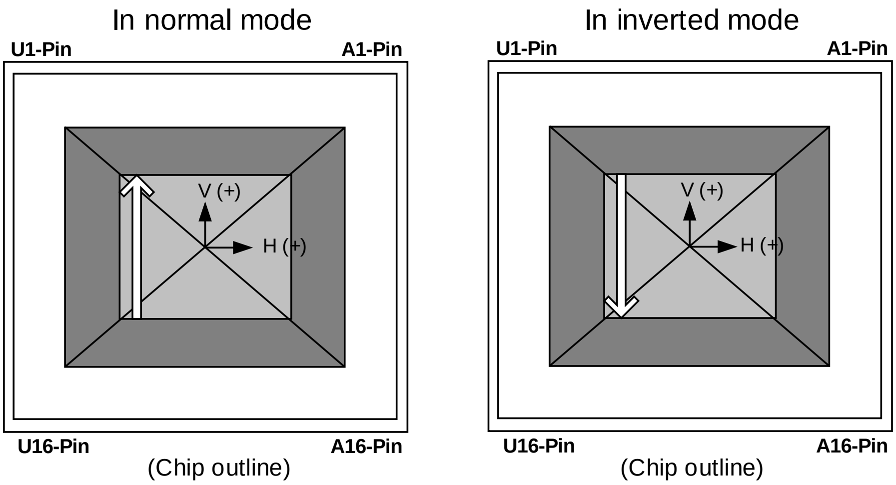
| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | bit | | |
| BLKLEVEL [11:0] | 04h | 54h (3254h) | [7:0] | 03Ch | 000h to FFFh |
| | | 55h (3255h) | [3:0] | | |

## Horizontal / Vertical Normal Operation and Inverted Operation

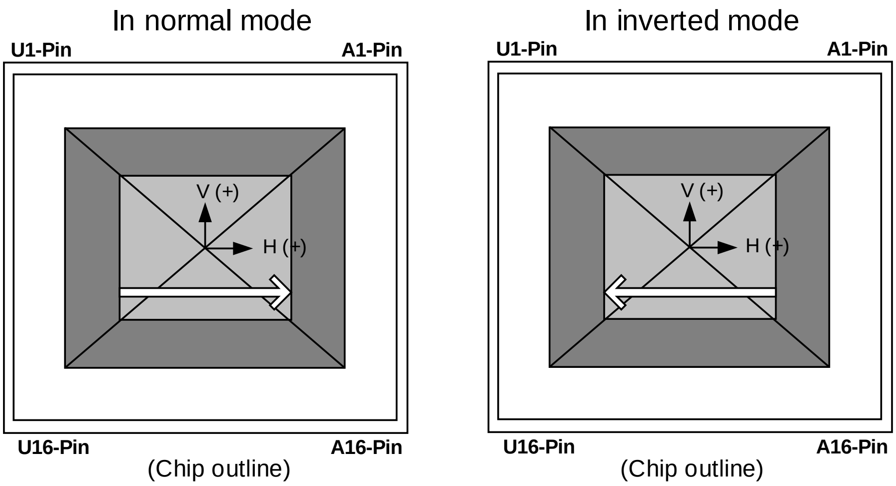
The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE register setting and sensor readout direction (normal / inverted) in horizontal direction can be switched by the HREVERSE register setting. See the section of "Readout Drive Modes" for the order of readout lines in normal and inverted modes.

Register List of Readout Drive Direction setting

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | bit | | |
| VREVERSE | 02h | 0Eh (300Eh) | [0] | 0h | 0h: Normal (Initial value)<br>1h: Inverted |
| HREVERSE | | | [1] | 0h | 0h: Normal (Initial value)<br>1h: Inverted |




Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)




Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

## Shutter and Integration Time Settings

This sensor has a global shutter function that integrates to the all line collectively by using memory in each pixel. This sensor has a variable electronic shutter function that can control the integration time in line units for adjust the exposure time. This sensor transferred signal to memory in pixel after the exposure (memory transfer), then this sensor performs output in which readout operation is performed sequentially for each line in sync with the XHS signal. This sensor has trigger mode that can be controlled exposure start timing and memory transfer timing by trigger.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

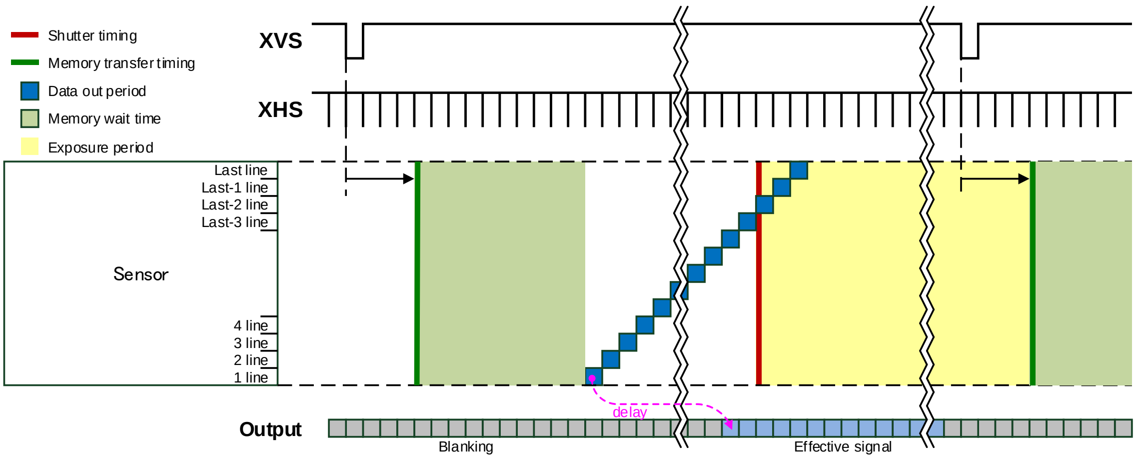



Image Drawing of Global Shutter (Normal mode) Operation

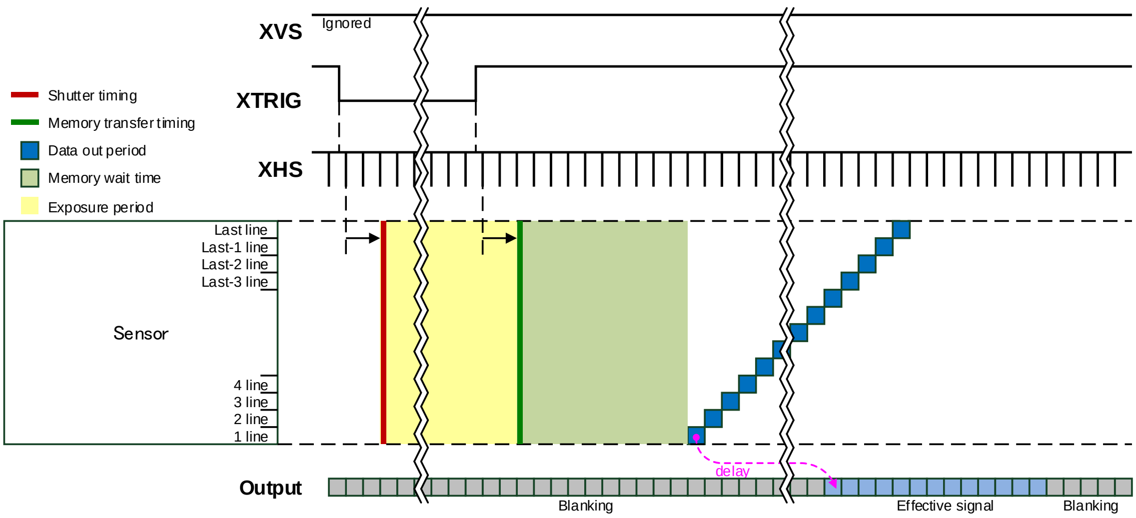



Image Drawing of Global Shutter (Sequential Trigger mode) Operation

## Global Shutter (Normal Mode) Operation

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS [19:0] register. For setting value of SHS [19:0], see the table "List of Exposure Setting". When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [19:0] register. The number of lines per frame differs according to the operating mode.

### Calculation Formula of Exposure Time

Exposure time [s] = (1 H period) × (Number of lines per frame - SHS) + 13.73(TBD) [μs][*1]

[*1]: Exposure time error ($t_{OFFSET}$)

Register List of Shutter setting

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I²C | bit | | |
| VMAX [19:0] | 02h | 10h (3010h) | [7:0] | 0082Eh | Set the number of lines per frame (only in master mode) |
| | | 11h (3011h) | [7:0] | | |
| | | 12h (3012h) | [3:0] | | |
| SHS [19:0] | | 8Dh (308Dh) | [7:0] | 0000Ah | Sets the shutter sweep time.<br>memory wait time to (Number of lines per frame - 1) |
| | | 8Eh (308Eh) | [7:0] | | |
| | | 8Fh (308Fh) | [3:0] | | |

## List of Exposure Setting

| Drive mode | memory wait time [H] | Number of lines per frame [DEC] | SHS Setting value [DEC] | Exposure Setting value [H] | 8 ch LVDS / Maximum frame rate | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Frame rate [frame/s] | | | Actually exposure [ms][*4] | | |
| | | | | | 8 bit | 10bit | 12 bit | 8 bit | 10bit | 12 bit |
| All-pixel | 10 | 1582 | 1581 | 1 | 151.4 | 123.5 | 105.7 | 0.018 | 0.019 | 0.020 |
| | | | 1580 | 2 | | | | 0.022 | 0.024 | 0.026 |
| | | | … | … | | | | … | … | … |
| | | | 11 | 1571 | | | | 6.581 | 8.057 | 9.408 |
| | | | 10 | 1572 | | | | 6.585 | 8.062 | 9.414 |
| 1080p-Full HD | 6 | 1125 | 1124 | 1 | — | 120 | | — | 0.021 | |
| | | | 1123 | 2 | | | | | 0.029 | |
| | | | … | … | | | | | … | |
| | | | 7 | 1118 | | | | | 8.298 | |
| | | | 6 | 1119 | | | | | 8.306 | |
| ROI | 10 | $V_{TR}$[*1] | $V_{TR}$-1 | 1 | *2 | | | 0.018 | 0.019 | 0.020 |
| | | | $V_{TR}$-2 | 2 | | | | 0.022 | 0.024 | 0.026 |
| | | | … | … | | | | … | | |
| | | | 11 | $V_{TR}$-11 | | | | *3 | | |
| | | | 10 | $V_{TR}$-10 | | | | | | |

*1 $V_{TR}$ = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + 38
*2 For the frame rate, see the section "ROI mode" in "Readout Drive Mode".
*3 Conform to the calculation formula of exposure time. (Number of lines per frame = $V_{TR}$)
*4 INCK frequency is input by typical value, and $t_{OFFSET}$ (13.73(TBD) [µs]) is included.

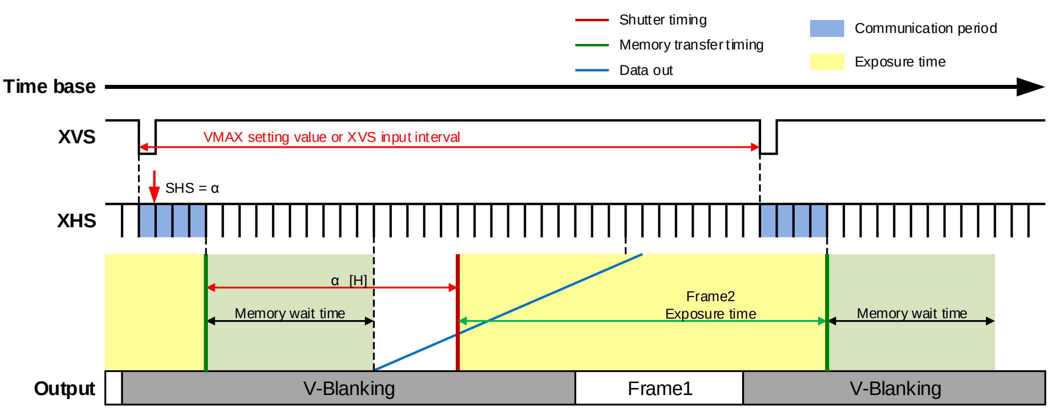



Image Drawing of Global Shutter (Normal Mode)

## Global Shutter (Sequential Tigger Mode) Operation

The integration time can be controlled by varying the pulse width that is input to XTRIG pin. The pulse width designated in XHS unit [H]. For the transition from normal mode to trigger mode, set 1 to the register TRIGEN. The XVS input signal is ignored during trigger mode operating. In case of inputting trigger continuously, there are period which prohibit the trigger rise input ($t_{TGPD}$) and fall input ($t_{GES}$) based on the previous trigger rise.
When the trigger rise is input before the rise input prohibited period ($t_{TGPD}$), interrupt operation starts.
This function is slave mode only. The number of lines per frame differs according to the operating mode.

### Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [H][*2]) + 13.73(TBD) [μs][*1]
[*1]: Exposure time error ($t_{OFFSET}$)
[*2]: Low level pulse width is counted by XHS pulse.

Register List of shutter setting

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I²C Address | bit | | |
| XMSTA | 02h | 0Ah (300Ah) | [0] | 1h | Setting of master mode operation<br>0: Master mode operation start<br>1: Master mode operation stop |
| TRIGEN | 02h | 0Bh (300Bh) | [0] | 0h | 0h: Global shutter (normal mode)<br>1h: Global shutter (trigger mode) |
| VINT_EN | 02h | AAh (30AAh) | [0] | 1h | Setting of Interrupt mode in Trigger Mode<br>0 : V interrupt is disable<br>1 : V interrupt is enable |

Parameter List of Global Shutter (Sequential Trigger Mode)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Integration start delay | $t_{TGST}$ | 2 | — | 3 | H |
| Integration end delay | $t_{TGED}$ | 2 + $t_{OFFSET}$ | — | 3 + $t_{OFFSET}$ | H |
| Integration time | $t_{TGSE}$ | 1 | — | — | H |
| Next trigger fall prohibited period (All-pixel, ROI, 1/2 Subsampling, FD Binning) | $t_{TGES}$ | 13 | — | — | H |
| Next trigger fall prohibited period (1080p Full-HD) | | 9 | — | — | H |
| Next trigger rise prohibited period (All-pixel) | $t_{TGPD}$ | 1582 | — | — | H |
| Next trigger rise prohibited period (1/2 Subsampling, FD Binning) | | 810 | | | |
| Next trigger rise prohibited period (1080p Full-HD) | | 1125 | — | — | |
| Next trigger rise prohibited period (ROI) | | $V_{TR}$ [*1] | — | — | |
| Data output delay (WUXGA / UXGA / ROI) | $t_{TGDLY}$ | — | 25 | — | H |
| Data output delay (1080p-Full HD) | | — | 17 | — | |

[*1] $V_{TR}$ = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + 38

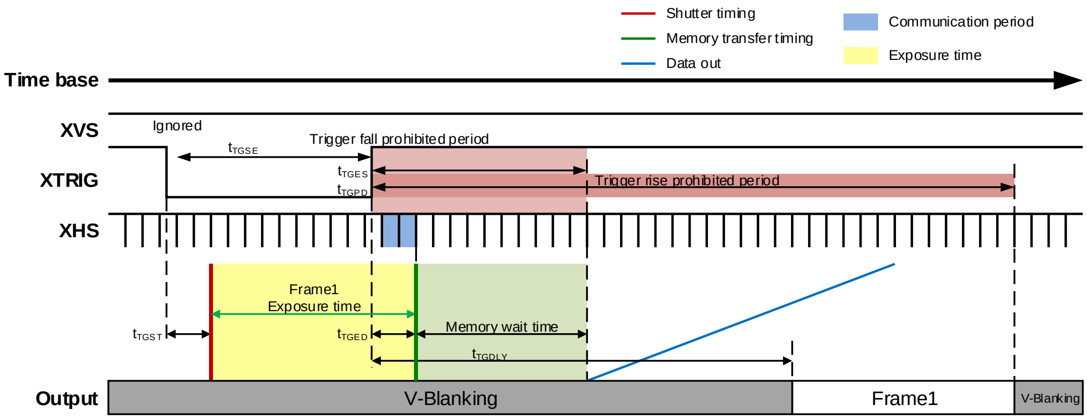



Image Drawing of Global Shutter (Sequential Trigger Mode)

## Interrupt Operation

In case of VINT_EN = 1h, the image drawing when the interrupt operation is generated is shown below. When the trigger is raised again and the next frame is output during read of the frame for which read was started by a trigger rise (Frame1 in the figure below), Frame1 becomes an invalid frame. Trigger timing of interrupt generating corresponds to $t_{TGPD}$ in Parameter List of Global Shutter (Trigger Mode)
In case of VINT_EN = 0h, the trigger signal is ignored in $t_{TGPD}$(Prohibit period).

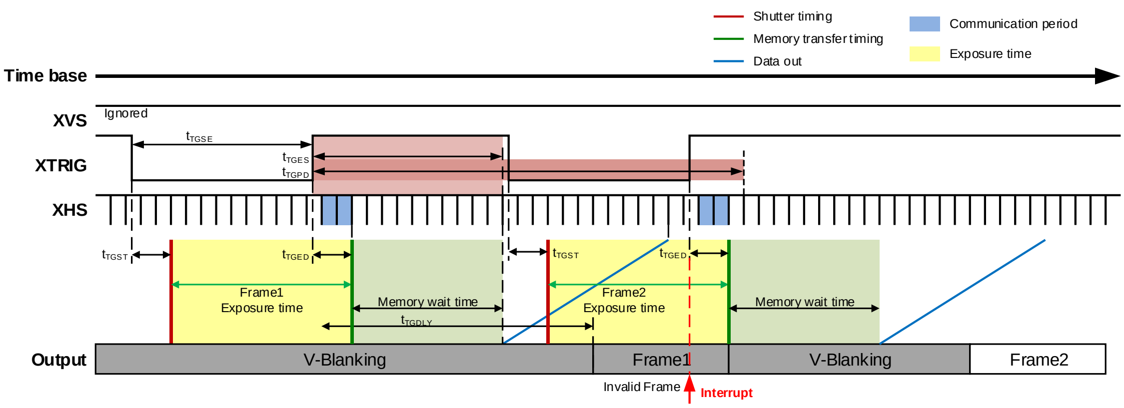



Image Drawing of Interrupt Operation in Global Shutter (Sequential Trigger Mode)

## Global Shutter (Fast Tigger Mode) Operation

Fast trigger mode is the trigger mode that starts exposure at fall of XTRIG immediately.
This mode supports Master mode only.

### Calculation Formula of Exposure Time

Exposure time [s] = (XTRIG low level pulse width [µs]) + 13.73(TBD) [µs]*1
*1: Exposure time error ($t_{OFFSET}$)

Register List of shutter setting

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I²C Address | bit | | |
| XMSTA | 02h | 0Ah (300Ah) | [0] | 1h | Setting of master mode operation<br>0: Master mode operation start<br>1: Master mode operation stop |
| TRIGEN | | 0Bh (300Bh) | [0] | 0h | 0h: Global shutter (normal mode)<br>1h: Global shutter (trigger mode) |
| SYNCSEL | | 36h (3036h) | [5:4] | 0h | XHS, XVS pin setting<br>0h : Normal Output<br>3h : Hi-Z |
| LOWLAGTRG | | AEh (30AEh) | [0] | 0h | Selection of trigger mode<br>0 : Sequential trigger mode<br>1 : Fast trigger mode |

Parameter List of Global Shutter (Fast Trigger Mode)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Integration start delay | $t_{TGST}$ | TBD | — | TBD | µs |
| Integration end delay | $t_{TGED}$ | TBD + $t_{OFFSET}$ | — | TBD + $t_{OFFSET}$ | µs |
| Integration time | $t_{TGSE}$ | TBD | — | — | µs |
| Next trigger rise / fall prohibited period (All-pixel) | $t_{TGPD}$ | 1598 | — | — | H |
| Next trigger rise / fall prohibited period (1/2 Subsampling, FD Binning) | | 826 | | | |
| Next trigger rise / fall prohibited period (1080p Full-HD) | | 1141 | — | — | |
| Next trigger rise / fall prohibited period (ROI) | | $V_{TR}$ *1 | — | — | |
| Data output delay (WUXGA / UXGA / ROI) | $t_{TGDLY}$ | — | 25 | — | H |
| Data output delay (1080p-Full HD) | | — | 17 | — | |

*1 $V_{TR}$ = ROIWV1 + ROIWV2 + ROIWV3 + … + ROIWV8 + 38

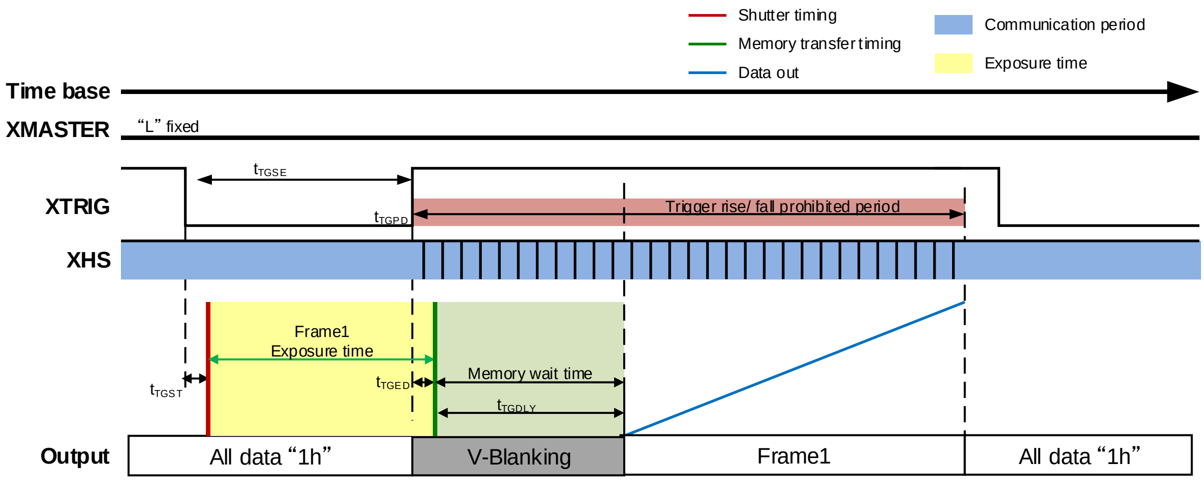



Image Drawing of Global Shutter (Fast Trigger Mode) (4-wire)

## Mode Transitions of Global Shutter Operation

The sensor can be switched between normal mode and trigger mode in global shutter operation by setting the register TRIGEN. The sensor will transition to normal mode or trigger mode 20H after the register TRIGEN is set. (The XVS and XTRIG input during transition are prohibited.)
In case of Fast Trigger mode, the mode transition must be done via sensor standby.

### Transition from Normal Mode to Sequential Trigger Mode

The sensor will transition from normal mode to trigger mode after setting 1d to register TRIGEN. The XVS input is ignored after transition to trigger mode. Trigger input is prohibited for a 20H period after the register TRIGEN is set. When TRIGEN is set during data read, read operation is stopped and that frame becomes an invalid frame.
* The communication is available till 9 H period only when sensor transition to the Trigger mode.

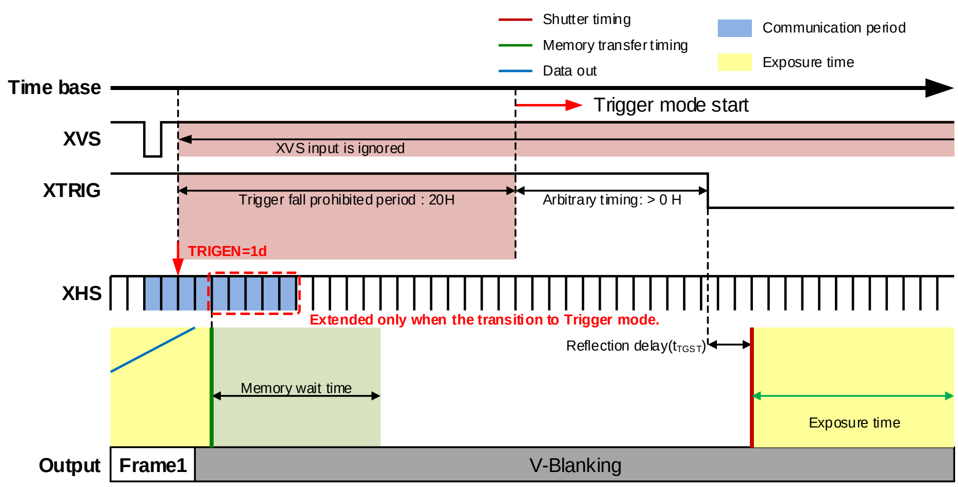



Image Drawing of Transition from Normal Mode to Sequential Trigger Mode

### Transition from Sequentiial Trigger Mode to Normal Mode

The sensor will transition from trigger mode to normal mode after setting 0d to register TRIGEN. Start XVS input after transition to normal mode. Set TRIGEN after Next trigger rise prohibited period ($t_{TGPD}$) has passed. When TRIGEN is set before $t_{TGPD}$, read operation is stopped and that frame becomes an invalid frame.

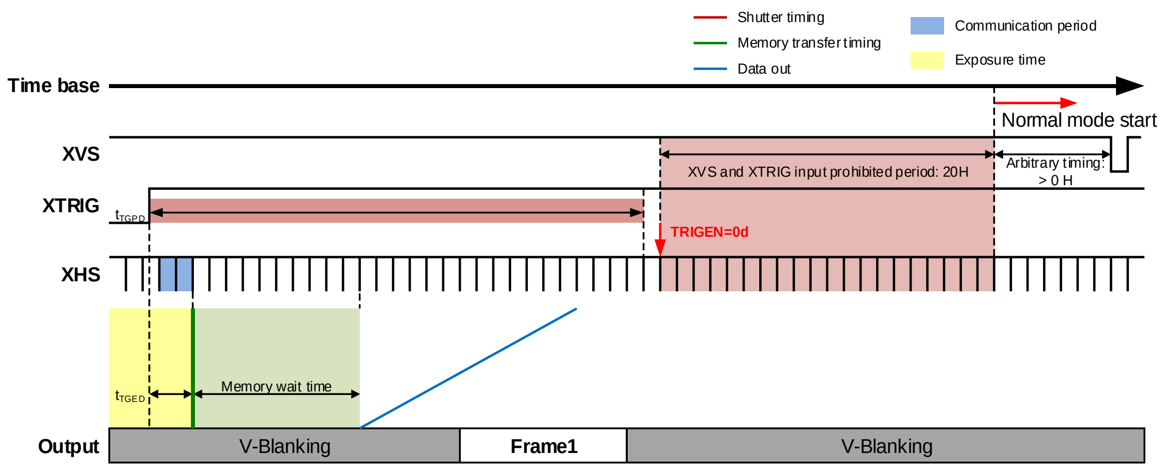



Image Drawing of Transition from Sequential Trigger Mode to Normal Mode

## Pulse Output Function

This sensor has a pulse output function that indicates each state of shutter operation. The pulse output from TOUT1 pin and TOUT2 pin. The rise timing and fall timing of pulse are set by Register. For the reference point (The timing when register value set to 0) to be set, see the table "List of Reference point". The pulse is output asynchronously with other signals on the basis of the sensor internal timing shown in the "List of Reference point". This function doesn't support Fast Trigger mode.

Register List of Pulse Output Function

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I$^2$C | bit | | |
| TOUT1SEL [1:0] | 02h | 26h (3026h) | [1:0] | 0h | TOUT1 pin setting<br>0h: Low fixed<br>3h: Pulse output |
| TOUT2SEL [1:0] | | | [3:2] | 0h | TOUT2 pin setting<br>0h: Low fixed<br>3h: Pulse output |
| TRIG_TOUT1_SEL [2:0] | | 29h (3029h) | [2:0] | 0h | TOUT1 pin output selection<br>0h: Low fixed 1h: Pulse1 output |
| TRIG_TOUT2_SEL [2:0] | | | [6:4] | 0h | TOUT2 pin output selection<br>0h: Low fixed 2h: Pulse2 output |
| PULSE1_EN_NOR | | 6Dh (306Dh) | [0] | 0 | Pulse1 enable in normal mode<br>0: disable 1: enable |
| PULSE1_EN_TRIG | | | [1] | 0 | Pulse1 enable in trigger mode<br>0: disable 1: enable |
| PULSE1_POL | | | [2] | 0 | Pulse1 polarity selection<br>0: High active 1: Low active |
| PULSE1_UP [19:0] | | 70h (3070h) | [7:0] | 00000h | Pulse1 active period start timing setting<br>Designated in line units from reference point |
| | | 71h (3071h) | [7:0] | | |
| | | 72h (3072h) | [3:0] | | |
| PULSE1_DN [19:0] | | 74h (3074h) | [7:0] | 00000h | Pulse1 active period end timing setting<br>Designated in line units from reference point |
| | | 75h (3075h) | [7:0] | | |
| | | 76h (3076h) | [3:0] | | |
| PULSE2_EN_NOR | | 79h (3079h) | [0] | 0 | Pulse2 enable in normal mode<br>0: disable 1: enable |
| PULSE2_EN_TRIG | | | [1] | 0 | Pulse2 enable in trigger mode<br>0: disable 1: enable |
| PULSE2_POL | | | [2] | 0 | Pulse2 polarity selection<br>0: High active 1: Low active |
| | | | [3] | 0 | Fixed to1 |
| PULSE2_UP [19:0] | | 7Ch (307Ch) | [7:0] | 00000h | Pulse2 active period start timing setting<br>Designated in line units from reference point |
| | | 7Dh (307Dh) | [7:0] | | |
| | | 7Eh (307Eh) | [3:0] | | |
| PULSE2_DN [19:0] | | 80h (3080h) | [7:0] | 00000h | Pulse2 active period end timing setting<br>Designated in line units from reference point |
| | | 81h (3081h) | [7:0] | | |
| | | 82h (3082h) | [3:0] | | |

List of Reference Point

| | Normal mode | Trigger mode |
|---|---|---|
| Reference point of Pulse1 | XVS fall edge in N frame | Fall edge of input trigger |
| Reference point of Pulse2 | XVS fall edge in N +1 frame | Rise edge of input trigger |

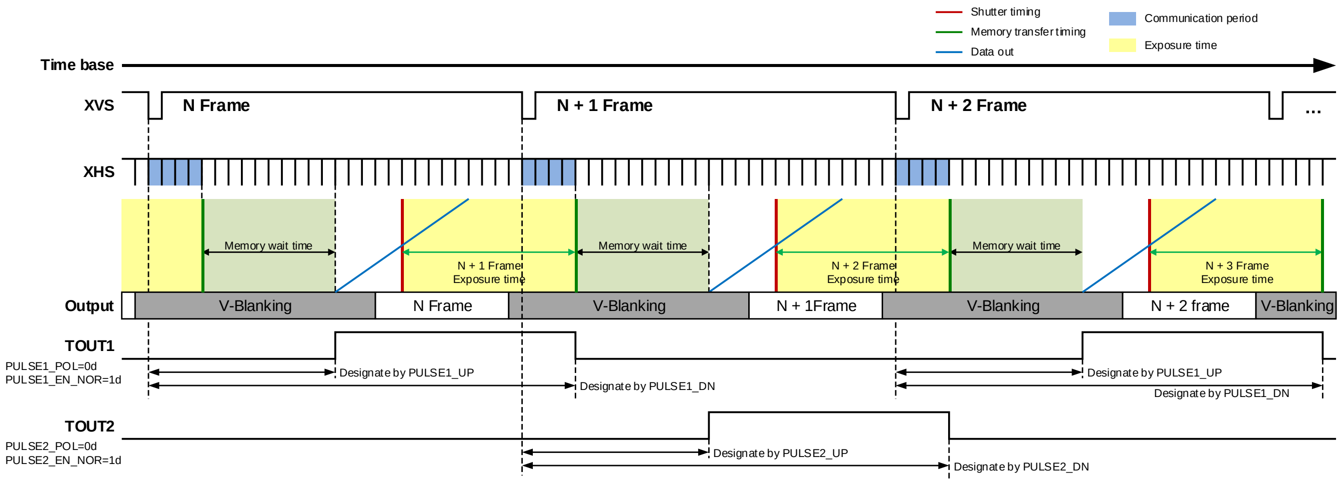



Image Drawing of Pulse Output Function in Global Shutter (Normal Mode)

In normal mode, TOUT1 and TOUT2 are output alternately each time inputting XVS.

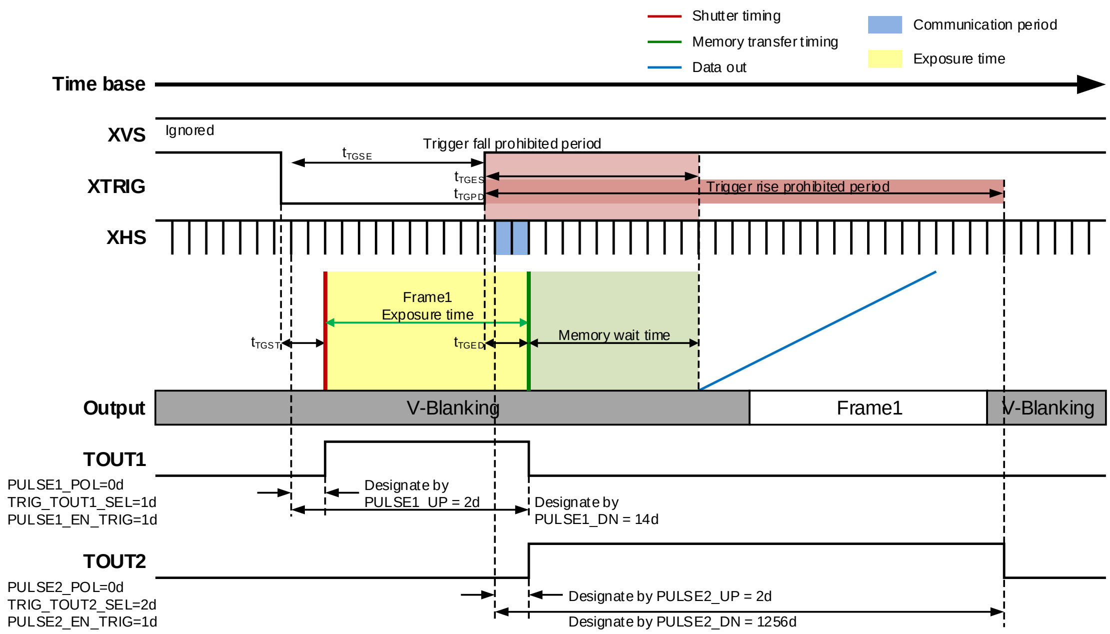



Image Drawing of Pulse Output Function in Global Shutter (Sequential Trigger Mode)

## Signal Output

### Output Pin Settings

This sensor supports Low voltage LVDS serial (4 ch / 8 ch / 16 ch switching) DDR output.
In addition, the data rate per channel is adjustable. The table below shows the output format settings.

Register List of Output Settings

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : I²C | bit | | |
| STBLVDS [3:0] | 02h | 05h (3005h) | [7:4] | 0h | The un-using LVDS channel go into standby |
| FREQ [1:0] | | 1Bh (301Bh) | [1:0] | 0h | Frame rate adjust |
| OPORTSEL [4:0] | | 1Ch (301Ch) | [7:4] | 9h | Output channel selection<br>(Refer the list of output setting below) |

Output Pins for Low Voltage LVDS Serial

| Output pins | Low voltage LVDS serial DDR output | | |
|---|---|---|---|
| | 4 ch | 8 ch | 16 ch |
| DLOPA1 / DLOMA1 | Hi-Z | Ch 7 | Ch 7 |
| DLOPB1 / DLOMB1 | Hi-Z | Ch 5 | Ch 5 |
| DLOPC1 / DLOMC1 | Ch 3 | Ch 3 | Ch 3 |
| DLOPD1 / DLOMD1 | Ch 1 | Ch 1 | Ch 1 |
| DLOPE1 / DLOME1 | Ch 2 | Ch 2 | Ch 2 |
| DLOPF1 / DLOMF1 | Ch 4 | Ch 4 | Ch 4 |
| DLOPG1 / DLOMG1 | Hi-Z | Ch 6 | Ch 6 |
| DLOPH1 / DLOMH1 | Hi-Z | Ch 8 | Ch 8 |
| DLOPA2 / DLOMA2 | Hi-Z | Hi-Z | Ch 15 |
| DLOPB2 / DLOMB2 | Hi-Z | Hi-Z | Ch 13 |
| DLOPC2 / DLOMC2 | Hi-Z | Hi-Z | Ch 11 |
| DLOPD2 / DLOMD2 | Hi-Z | Hi-Z | Ch 9 |
| DLOPE2 / DLOME2 | Hi-Z | Hi-Z | Ch 10 |
| DLOPF2 / DLOMF2 | Hi-Z | Hi-Z | Ch 12 |
| DLOPG2 / DLOMG2 | Hi-Z | Hi-Z | Ch 14 |
| DLOPH2 / DLOMH2 | Hi-Z | Hi-Z | Ch 16 |

Low-voltage LVDS serial 4 ch / 8 ch / 16 ch output format is shown in the figure below.

When setting 4 ch, after four data of SAV is output in the order of CH1 to CH4 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH4 respectively.

When setting 8 ch, after four data of SAV is output in the order of CH1 to CH8 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH1 to CH8 respectively.

When setting 16 ch, output in a format similar to the 4 ch and 8 ch output as shown below.

Data is sent MSB first. For details, see drive timing in each mode in the section of "Readout Drive Mode".

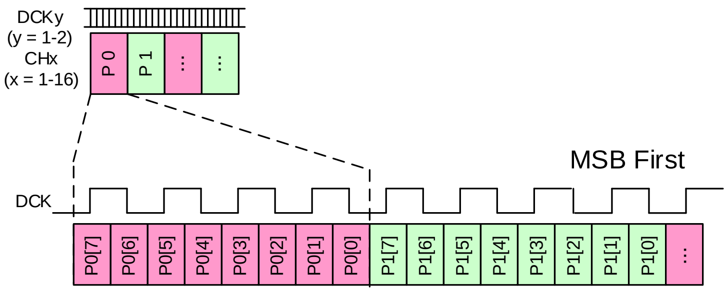

Output Format of Low voltage LVDS Serial 4 ch / 8 ch / 16 ch

## Output Pin Bit Width Selection

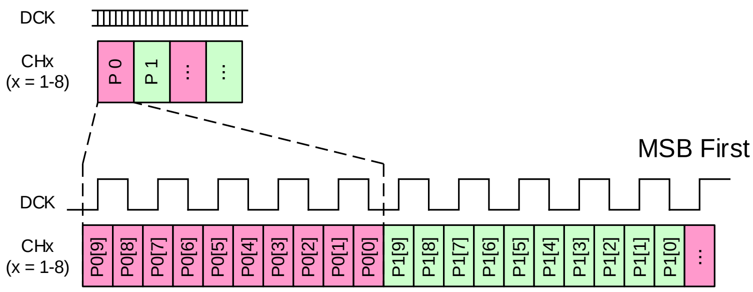
The output pin width can be selected from 8-bit, 10-bit or 12-bit output using register ADBIT, ODBIT. Sync code is output according to bit width setting of these register.

Register List of Bit Width Selection

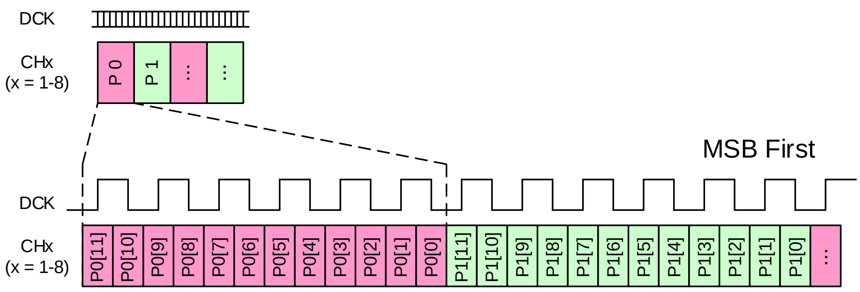
| Register | Register details | | | Initial value | Setting value | Remarks |
|---|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | bit | | | |
| ADBIT | 02h | 0Ch (300Ch) | [1:0] | 0h | 0h : 10 bit<br>1h : 12 bit<br>2h : 8bit | Set same value to both ADBIT and ODBIT |
| ODBIT | 02h | 16h (3016h) | [1:0] | 0h | 0h : 10 bit<br>1h : 12 bit<br>2h : 8bit | Set same value to both ADBIT and ODBIT |




Example of Data format in low-voltage LVDS serial 8-bit output




Example of Data format in low-voltage LVDS serial 10-bit output




Example of Data format in low-voltage LVDS serial 12-bit output

## Output Signal Range

The sensor output has either a 8-bit or 10-bit or 12-bit gradation, but output is not performed over the full range, and the maximum output value is the "FFh – 1" (8-bit output), the "3FFh - 1" (10-bit output) and the "FFFh - 1" (12-bit output). The minimum value is 001h. The output range for each output gradation is shown in the table below. The maximum level and the minimum level are output only in the sync code. See the item of "Sync Codes" in the section of "Operating Modes" for the sync codes.

Output Gradation and Output Range

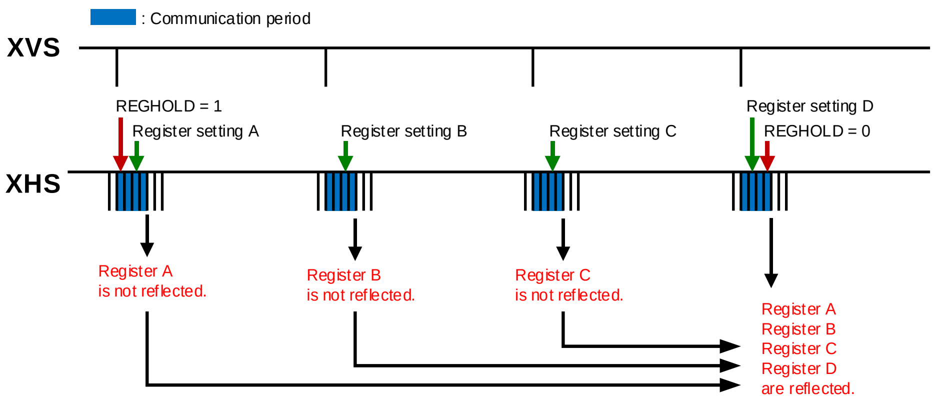
| Output gradation | Output value | |
|---|---|---|
| | Min. | Max. |
| 8bit | 01h | FEh |
| 10 bit | 001h | 3FEh |
| 12 bit | 001h | FFEh |

## Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register List of Register Hold

| Register | Register details | | | Initial value | Setting value |
|---|---|---|---|---|---|
| | Chip ID | Address ( ) : $I^2C$ | bit | | |
| REGHOLD | 02h | 08h (3008h) | [0] | 0h | 0h: Invalid<br>1h: Valid (Register hold) |




Register Hold Setting

## Mode Transition

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

| Transition | | | State |
|---|---|---|---|
| ROI | → | All-pixel | Via the Standby state is unnecessary |
| All-pixel | → | ROI | |
| - Transition between modes other than the above<br>- Change the input frequency of INCK<br>- Change the data rate (change the register FREQ)<br>- Change the number of output channels (change the register OPORTSEL)<br>- Change the bit width (change the register ADBIT, ODBIT) | | | Via the standby state is necessary |

*1 When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

## Other Function

IMX252 has the function as below. About detail, refer to each application note.

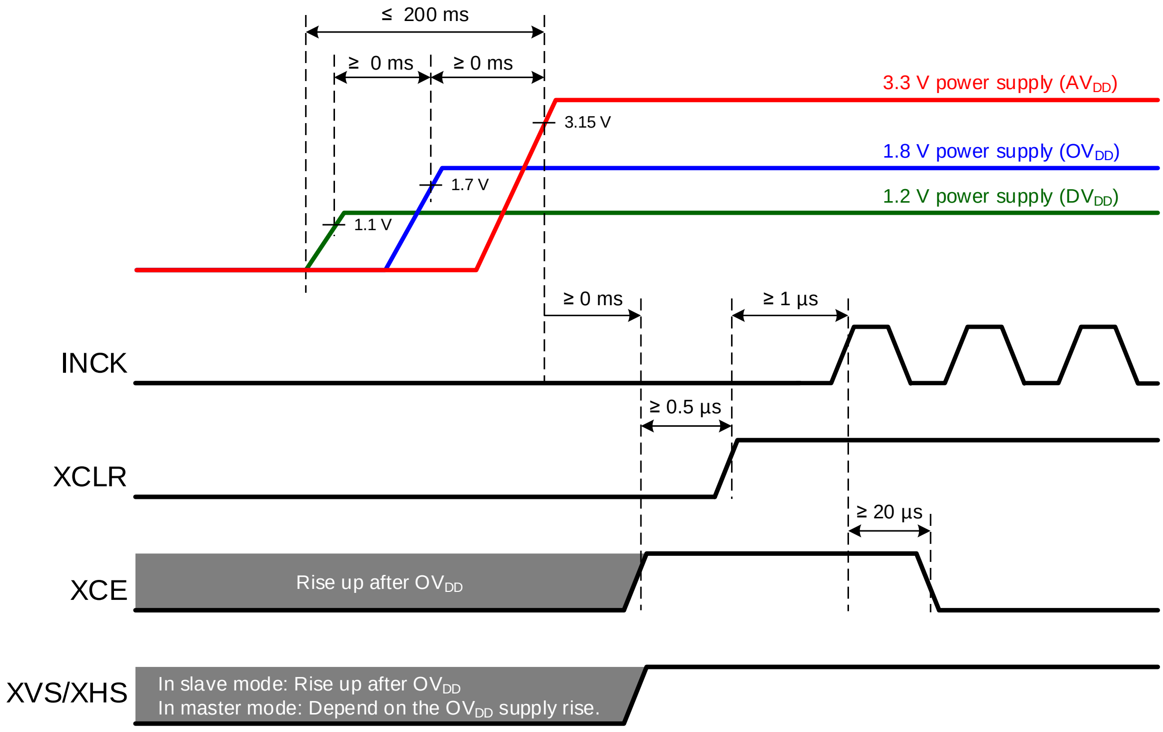
- Multi Frame Set Output mode (2 / 4 frame)
- Multi Exposure Trigger mode
- Multi Frame ROI (Multi Exposure + ROI) mode
- Driving Low Power Consumption at longtime exposure
- Simple Thermometer
- Gradation Compression
- Pattern Generator

## Power-on and Power-off Sequence

### Power-on sequence

Follow the sequence below to turn On the power supplies.

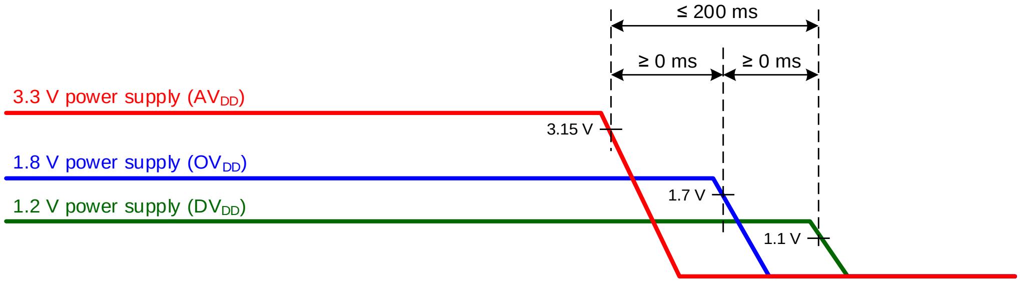
1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply ($DV_{DD}$) →1.8 V power supply ($OV_{DD}$) → 3.3 V power supply ($AV_{DD}$). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply ($OV_{DD}$), so hold XCE at High level until INCK is input.
3. Start the input of INCK after turning the level of XCLR into the high.
4. Make the sensor setting by register communication after the system clear. A period of 0 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE.




Power-on Sequence

### Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply ($AV_{DD}$) → 1.8 V power supply ($OV_{DD}$) → 1.2 V power supply ($DV_{DD}$). In addition, all power supplies should finish falling within 200 ms.
Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XTRIG, SLAMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply ($OV_{DD}$) falls.

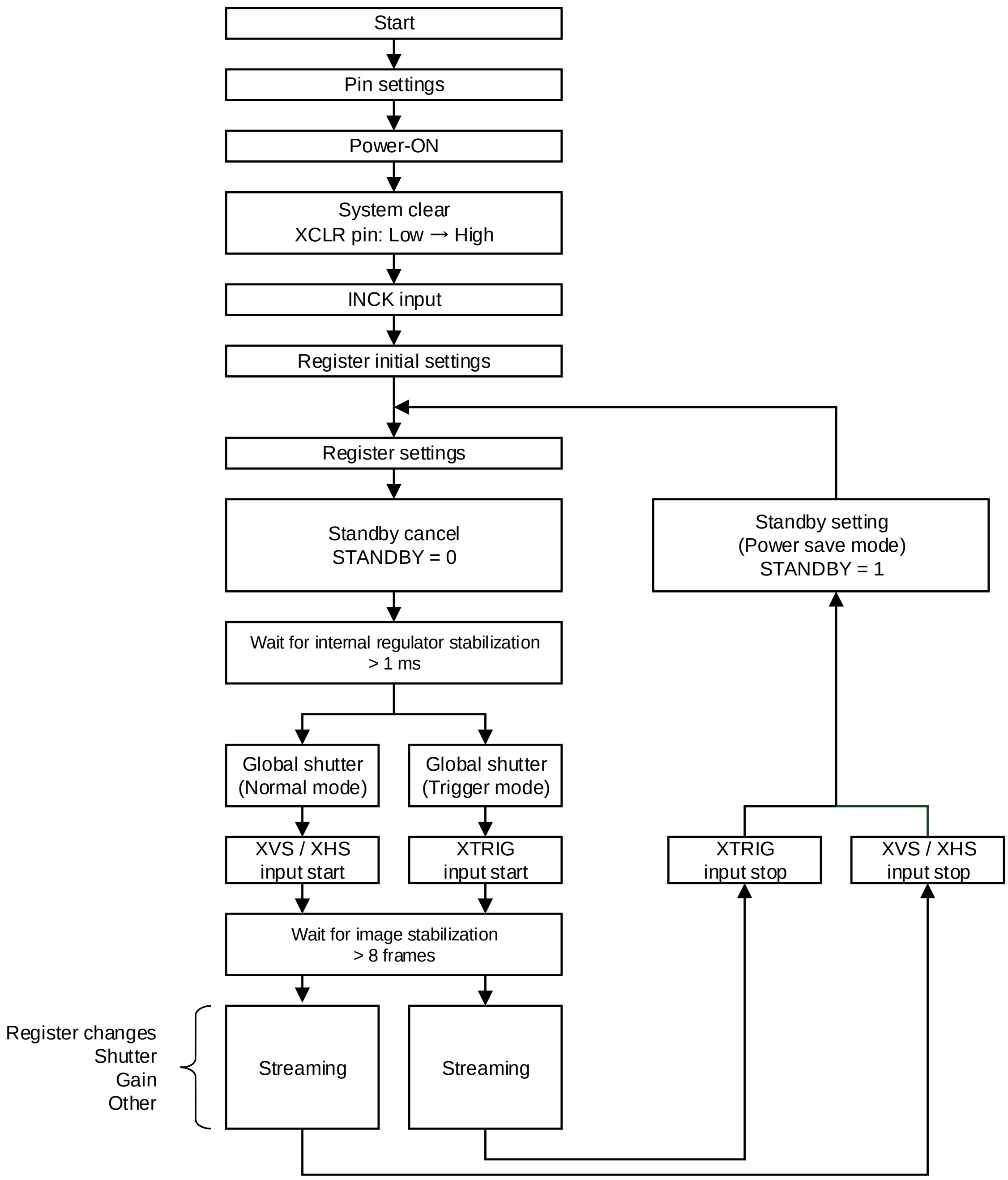



Power-off Sequence

## Sensor Setting Flow

### Setting Flow in Sensor Slave Mode

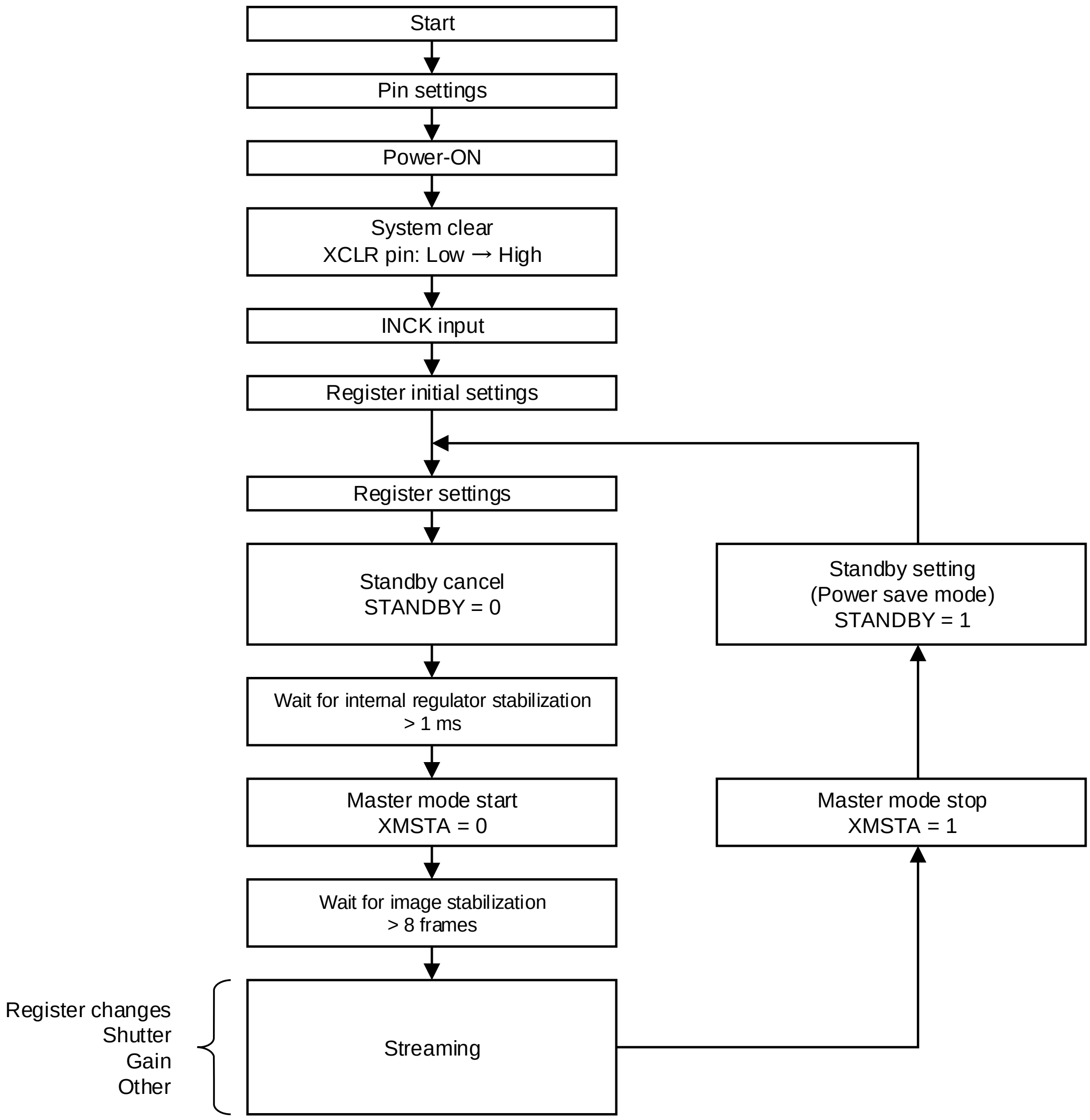
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". “Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.




Sensor Setting Flow (Sensor Slave Mode)

## Sensor Flow in Sensor Master Mode

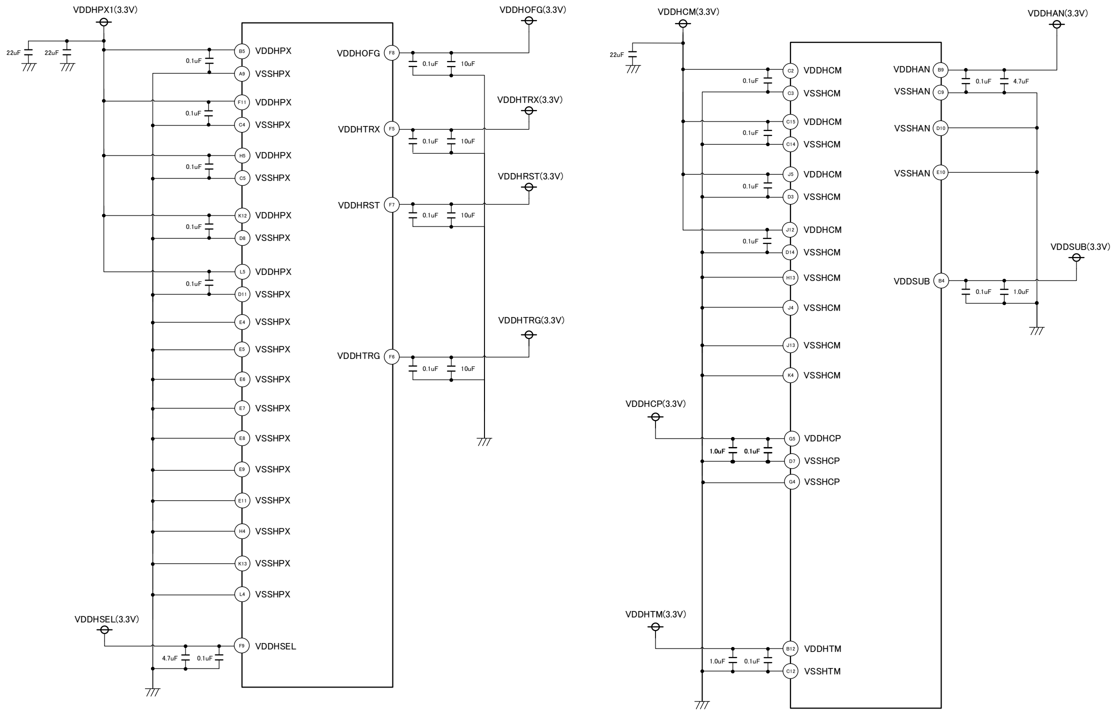
The figure below shows operating flow in sensor master mode.
For details of "Power on" to "System clear", see the item of "Power on sequence" in this section. For details of "Standby cancel" to "Wait for image stabilization", see the item of "Standby mode". In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Wait for internal regulator stabilization”.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".




Sensor Setting Flow (Sensor Master Mode)

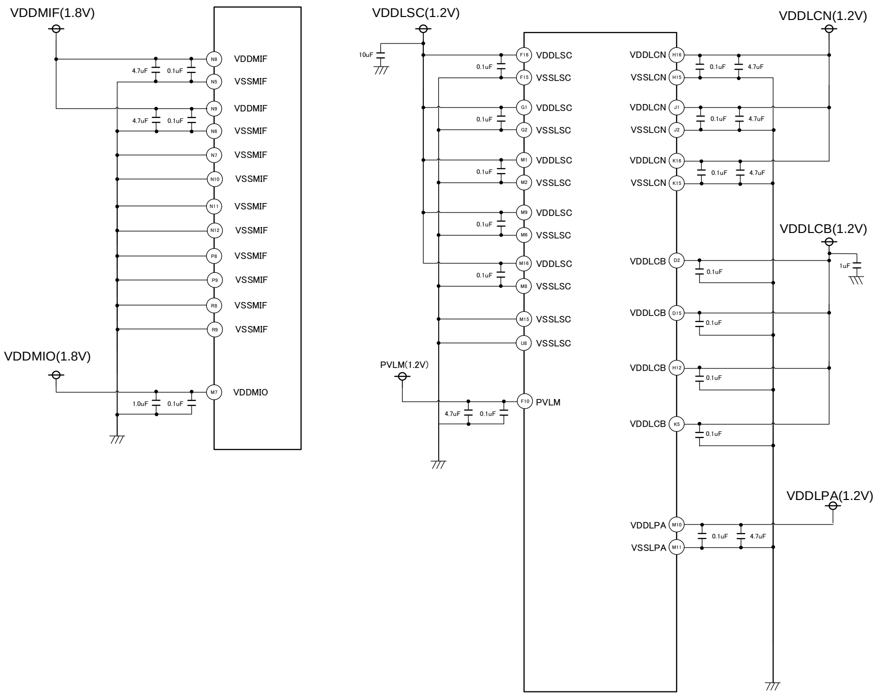
## Peripheral Circuit

### Analog Power Pins



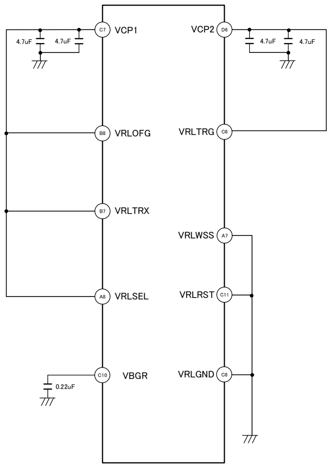

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## Digital Power Pins



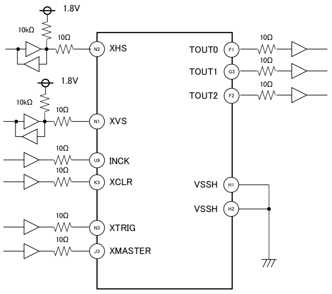

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## Analog Other Pins

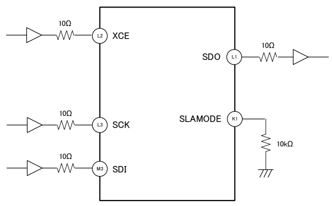



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

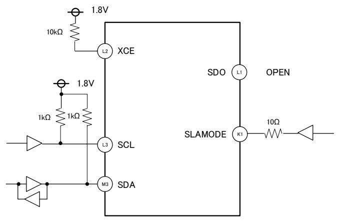
## Digital I/O Pins




4-wire serial communication

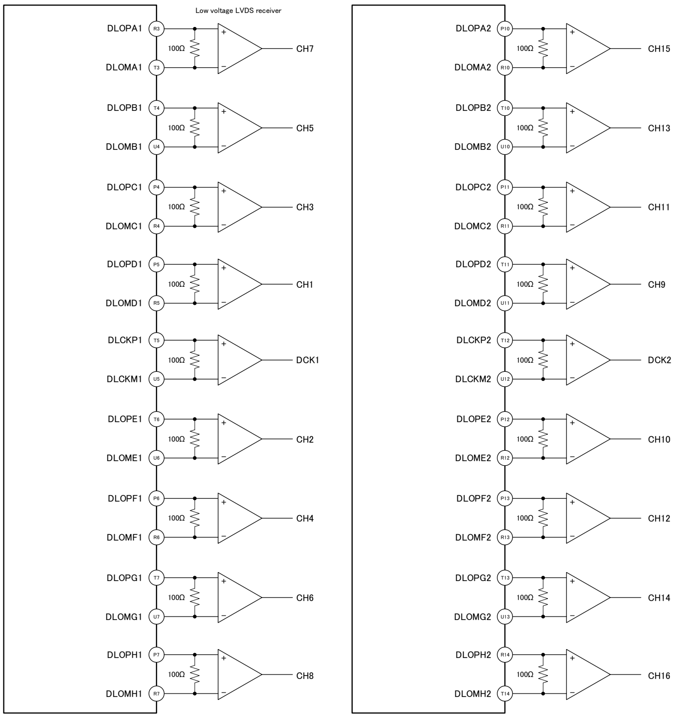



I²C communication




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

## Output pins




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

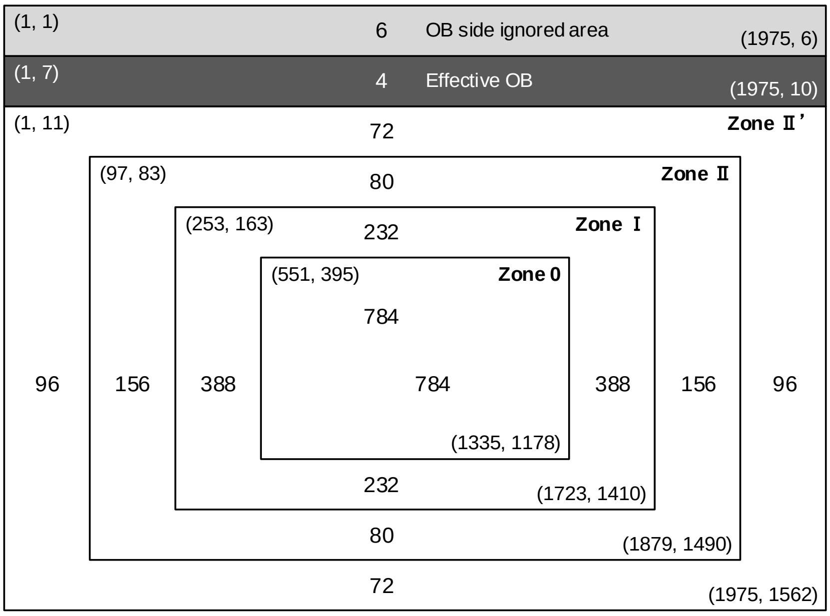
## Spot Pixel Specifications

(Tj = 60 ˚C)

| Type of distortion | Level | Maximum distorted pixels in each zone | | | Measurement method | Remarks |
|---|---|---|---|---|---|---|
| | | 0 to II' | Effective OB | Ineffective OB | | |
| Black and white pixels at high light | 30 % ≤ D | TBD | No evaluation criteria applied | | 1 | |
| White pixels in the dark | 5.6 mV ≤ D | TBD | | No evaluation criteria applied | 2 | 1/30 s storage |
| Black pixels at signal saturated | D ≤ TBD mV | 0 | No evaluation criteria applied | | 3 | |

Note) 1. Zone is specified based on all-pixel drive mode
2. D…Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

## Sport Pixel Zone Definition



## Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

### [For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

**Example of Annual Number of Occurrence**

| White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C) | Annual number of occurrence |
|---|---|
| 5.6 mV or higher | TBD pcs |
| 10.0 mV or higher | TBD pcs |
| 24.0 mV or higher | TBD pcs |
| 50.0 mV or higher | TBD pcs |
| 72.0 mV or higher | TBD pcs |

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

**For Your Reference:**

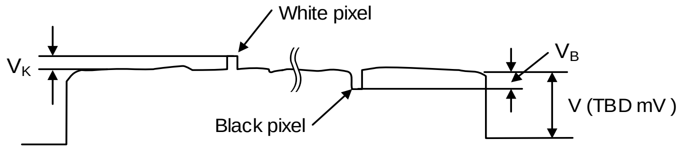
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

## Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value V of the Gr signal outputs is TBD mV, measure the local dip point (black pixel at high light, $V_B$) and peak point (white pixel at high light, $V_K$) in the signal output V, and substitute the value into the following formula.

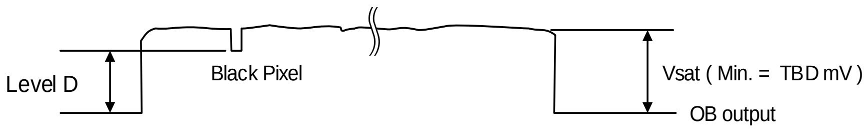
   Spot pixel level D = (($V_B$ or $V_K$) / Average value of V) × 100 [%]




Signal output waveform

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

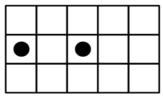
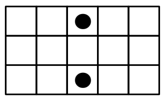



Signal output waveform

## Spot Pixel Pattern Specification

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

| No. | Pattern | White pixel<br>Black pixel<br>Bright pixel |
|---|---|---|
| 1 |  | Rejected |
| 2 |  | Rejected |

Note) 1. "● " shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated "Rejected" is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

## Marking

TBD

## Notes On Handling

**1. Static charge prevention**

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

**2. Protection from dust and dirt**

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

**3. Installing (attaching)**

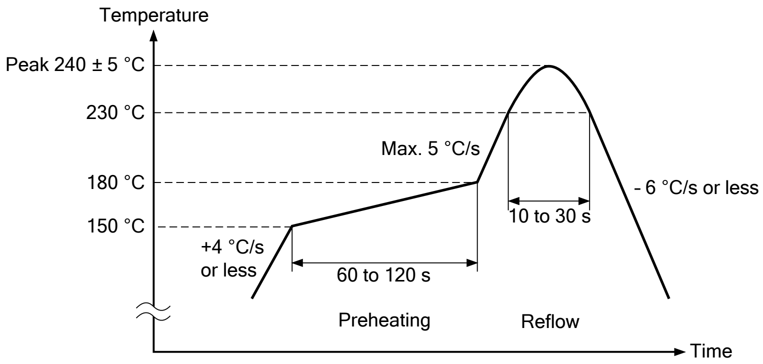
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

**4. Recommended reflow soldering conditions**

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

| Control item | Profile (at part side surface) |
|---|---|
| 1. Preheating | 150 to 180 °C<br>60 to 120 s |
| 2. Temperature up (down) | +4 °C/s or less (- 6 °C/s or less) |
| 3. Reflow temperature | Over 230 °C<br>10 to 30 s<br>Max. 5 °C/s |
| 4. Peak temperature | Max. 240 ± 5 °C |




(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

**5. Others**

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

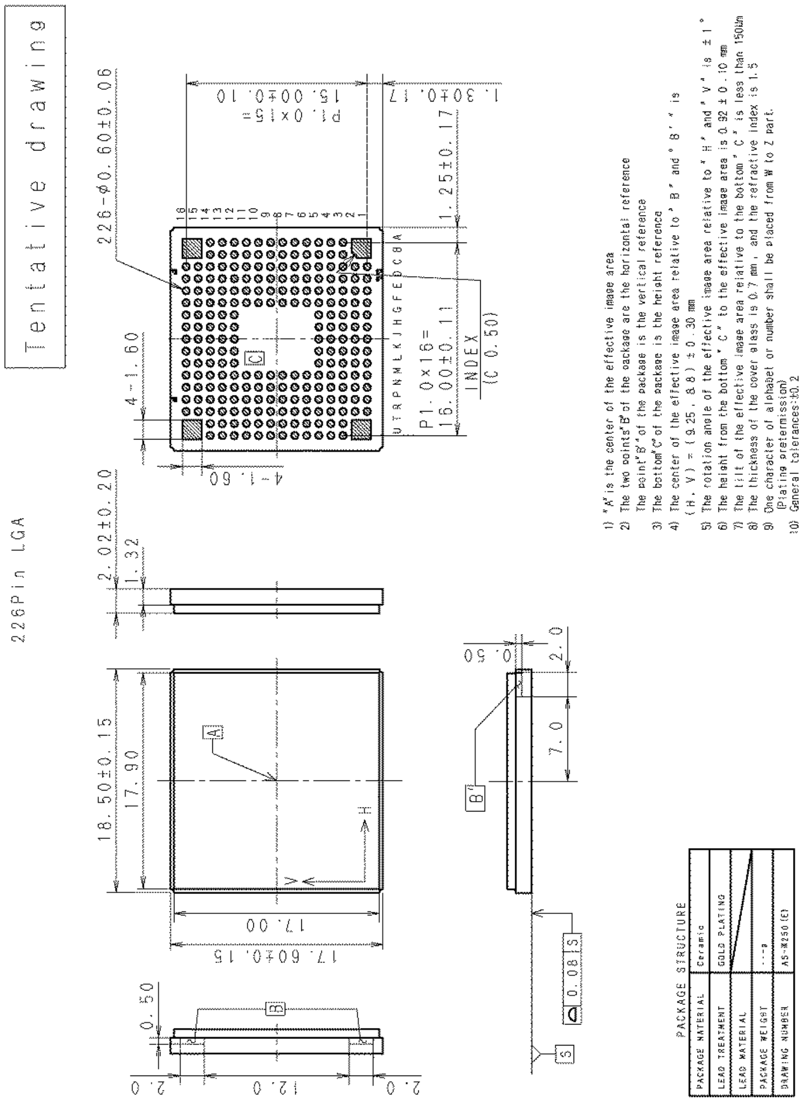
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

## Package Outline

(Unit: mm)



## List of Trademark Logos and Definition Statements

Exmor

* Exmor is a trademark of Sony Corporation. The Exmor is a version of Sony's high performance CMOS image sensor with high-speed processing, low noise and low power dissipation by using column-parallel A/D conversion.

Pregius

* Pregius is a trademark of Sony Corporation. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony's low-noise CCD structure, and realizes high picture quality.

## Revision History

| Date of change | Revision | Page | Contain of Change |
|---|---|---|---|
| 02-Mar-15 | 0.1 | - | First edition |
| 07-May-15 | 0.2 | P1, P47, P48, P49 P51, P60, P62, P63, | Correction:<br>Description relates to frame rate. |
| | | P26 to P28 | Added :<br>"(4-wire)" at Title. |
| | | P35 to P46 | Correction:<br>Register map |
| | | P36 | Correction:<br>Description of WINMODE. |
| | | P47 to P49 | Correction:<br>Value at "Total number of pixcels" and "Number of INCK in 1H" |
| | | P52, P55, P56,P62, P63 | Correction:<br>Total horizon data values on each pixel array image drawing. |
| | | P51, P54, P62, P63 | Correction:<br>HMAX setting value of each mode. |
| | | P53 | Correction:<br>Data number at the figure. |
| | | P53, P61 | Added:<br>"16ch output" at the figure. |
| | | P52, P62 | Correction:<br>Value at "Total number of pixels". |
| | | P62, P63 | Correction:<br>Line value at VMAX |
| | | P63 | Correction:<br>Title name. |
| | | P71 | Correction:<br>List of Exposure Setting. |
| | | P75 | Correction:<br>"tTGED" at figure. |
| | | P77 | Added :<br>ChipID=2, Address=79h, bit=3 at Register List of Pulse Output Function. |
| | | P77 | Delete : The Notice about registers |
| | | P85 | Delete:<br>8bit high speed recording mode.<br>Added:<br>Driving Low Power Consumption at longtime exposure.<br>Correction:<br>Multi exposure ⇒Multi Frame Set Output. |
| | | P102 | Update:<br>Package Outline figure. |