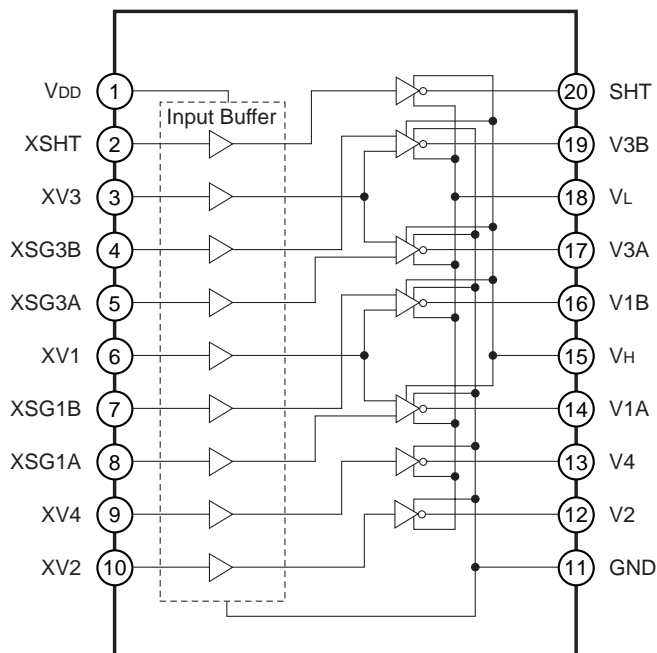




Block Diagram



Pin Description

Pin No.	Symbol	I/O	Functions
1	VDD	—	Input power supply (3.3V system)
2	XSHT	I	SHT pulse input
3	XV3	I	V3A and V3B transfer pulse input
4	XSG3B	I	V3B readout pulse input
5	XSG3A	I	V3A readout pulse input
6	XV1	I	V1A and V1B readout pulse input
7	XSG1B	I	V1B readout pulse input
8	XSG1A	I	V1A readout pulse input
9	XV4	I	V4 transfer pulse input
10	XV2	I	V2 transfer pulse input
11	GND	—	GND (= V <sub>M</sub> )
12	V2	O	High voltage output (2 levels: V <sub>M</sub> , V <sub>L</sub> )
13	V4	O	High voltage output (2 levels: V <sub>M</sub> , V <sub>L</sub> )
14	V1A	O	High voltage output (3 levels: V <sub>H</sub> , V <sub>M</sub> , V <sub>L</sub> )
15	V <sub>H</sub>	—	Positive power supply for high voltage output (15V system)
16	V1B	O	High voltage output (3 levels: V <sub>H</sub> , V <sub>M</sub> , V <sub>L</sub> )
17	V3A	O	High voltage output (3 levels: V <sub>H</sub> , V <sub>M</sub> , V <sub>L</sub> )
18	V <sub>L</sub>	—	Negative power supply for high voltage output (−7.5V system)
19	V3B	O	High voltage output (3 levels: V <sub>H</sub> , V <sub>M</sub> , V <sub>L</sub> )
20	SHT	O	High voltage output (2 levels: V <sub>H</sub> , V <sub>L</sub> )

## Truth Table

Input				Output		
XV1, 3	XSG1A, 1B, 3A, 3B	XV2, 4	XSHT	V1A, 1B, 3A, 3B	V2, 4	SHT
L	L	X	X	V <sub>H</sub>	X	X
L	H	X	X	V <sub>M</sub>	X	X
H	L	X	X	Z	X	X
H	H	X	X	V <sub>L</sub>	X	X
X	X	L	X	X	V <sub>M</sub>	X
X	X	H	X	X	V <sub>L</sub>	X
X	X	X	L	X	X	V <sub>H</sub>
X	X	X	H	X	X	V <sub>L</sub>

Z: High impedance X: Don't care

## Electrical Characteristics

## DC Characteristics

(V<sub>DD</sub> = 3.3V, V<sub>H</sub> = 15V, V<sub>M</sub> = GND, V<sub>L</sub> = -8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level input voltage	V <sub>IH</sub>		0.7V <sub>DD</sub>	—	—	V
"L" level input voltage	V <sub>IL</sub>		—	—	0.3V <sub>DD</sub>	V
Input current	I <sub>IN</sub>	V <sub>IN</sub> = GND to 5V	-10	0.0	10	μA
Operating supply current	I <sub>H</sub>	*1	—	0.10	0.20	mA
Operating supply current	I <sub>DD</sub>	*1	—	0.25	0.50	mA
Operating supply current	I <sub>L</sub>	*1	-8.5	-5.5	—	mA
Output current	I <sub>OL</sub>	V1A, 1B, 3A, 3B, V2, 4 = -8.25V	10	—	—	mA
Output current	I <sub>OM1</sub>	V1A, 1B, 3A, 3B, V2, 4 = -0.25V	—	—	-5.0	mA
Output current	I <sub>OM2</sub>	V1A, 1B, 3A, 3B = 0.25V	5.0	—	—	mA
Output current	I <sub>OH</sub>	V1A, 1B, 3A, 3B = 14.75V	—	—	-7.2	mA
Output current	I <sub>OSL</sub>	SHT = -8.25V	5.4	—	—	mA
Output current	I <sub>OSH</sub>	SHT = 14.75V	—	—	-4.0	mA

\*1 See Measurement Circuit. Shutter speed 1/10000

**Note)** Current direction +: inflow to IC; -: outflow from IC

## Switching Characteristics

(V<sub>DD</sub> = 3.3V, V<sub>H</sub> = 15V, V<sub>M</sub> = GND, V<sub>L</sub> = -7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T <sub>PLM</sub>	*1	50	70	100	ns
Propagation delay time	T <sub>PMH</sub>	*1	50	70	100	ns
Propagation delay time	T <sub>PLH</sub>	*1	50	70	100	ns
Propagation delay time	T <sub>PML</sub>	*1	10	30	50	ns
Propagation delay time	T <sub>PHM</sub>	*1	10	30	50	ns
Propagation delay time	T <sub>PHL</sub>	*1	10	30	50	ns
Rise time	T <sub>TLM</sub>	V <sub>L</sub> → V <sub>M</sub> *1	200	350	500	ns
Rise time	T <sub>TMH</sub>	V <sub>M</sub> → V <sub>H</sub> *1	200	350	500	ns
Rise time	T <sub>TLH</sub>	V <sub>L</sub> → V <sub>H</sub> *1	30	60	90	ns
Fall time	T <sub>TML</sub>	V <sub>M</sub> → V <sub>L</sub> *1	200	350	500	ns
Fall time	T <sub>THM</sub>	V <sub>H</sub> → V <sub>M</sub> *1	200	350	500	ns
Fall time	T <sub>THL</sub>	V <sub>H</sub> → V <sub>L</sub> *1	30	60	90	ns
Output noise voltage	V <sub>CLH</sub>	*2	—	—	1.0	V
Output noise voltage	V <sub>CLL</sub>	*2	—	—	1.0	V
Output noise voltage	V <sub>CMH</sub>	*2	—	—	1.0	V
Output noise voltage	V <sub>CML</sub>	*2	—	—	1.0	V

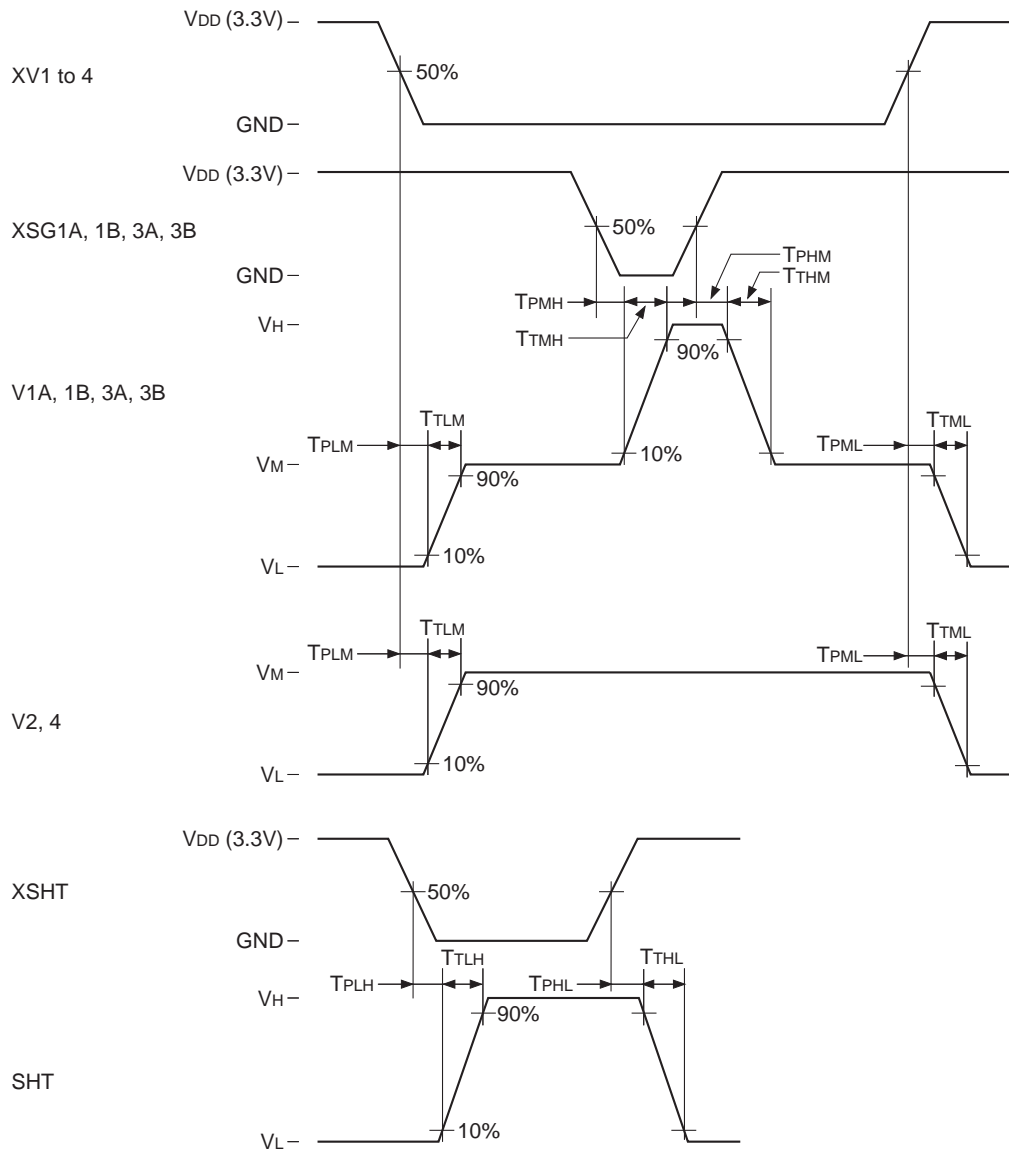
\*1 See Switching Waveform.

\*2 See Noise on a Waveform.

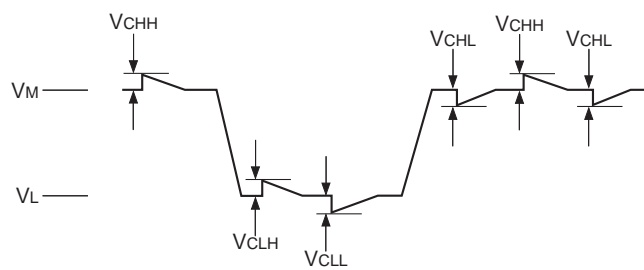
**Note)** Each item is evaluated by Measurement Circuit.**Notes on Operation** (See Application Circuit.)

1. Be sure to protect against static electricity because this IC is MOS structure.
2. A bypass capacitor (0.1μF or more) is connected between GND and near each power supply (V<sub>H</sub>, V<sub>DD</sub>, V<sub>L</sub>).
3. In order to protect CCD image sensor, input SHT pin output to SUB pin of CCD image sensor after that has been clamped at V<sub>H</sub>.

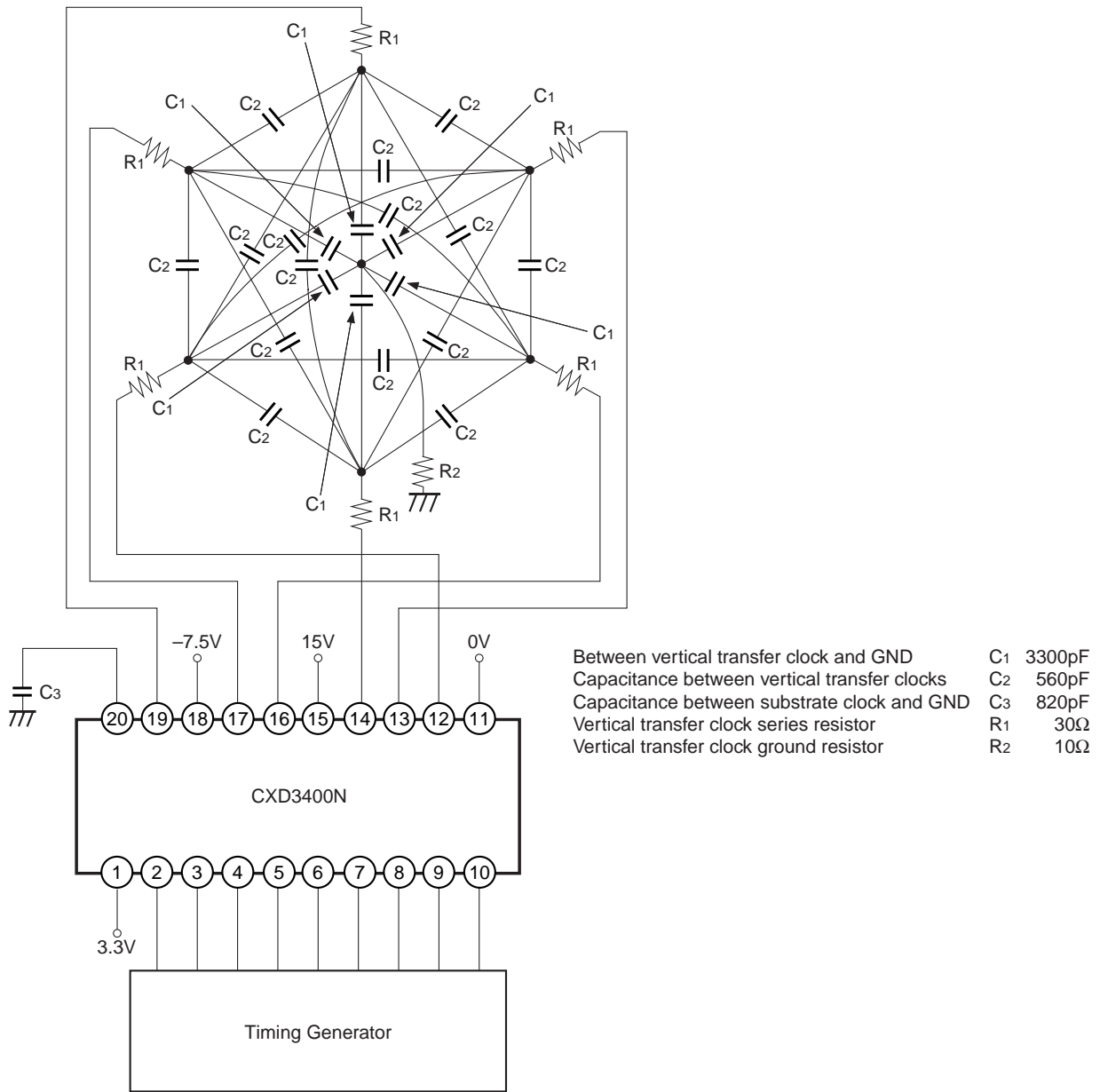
Switching Waveform



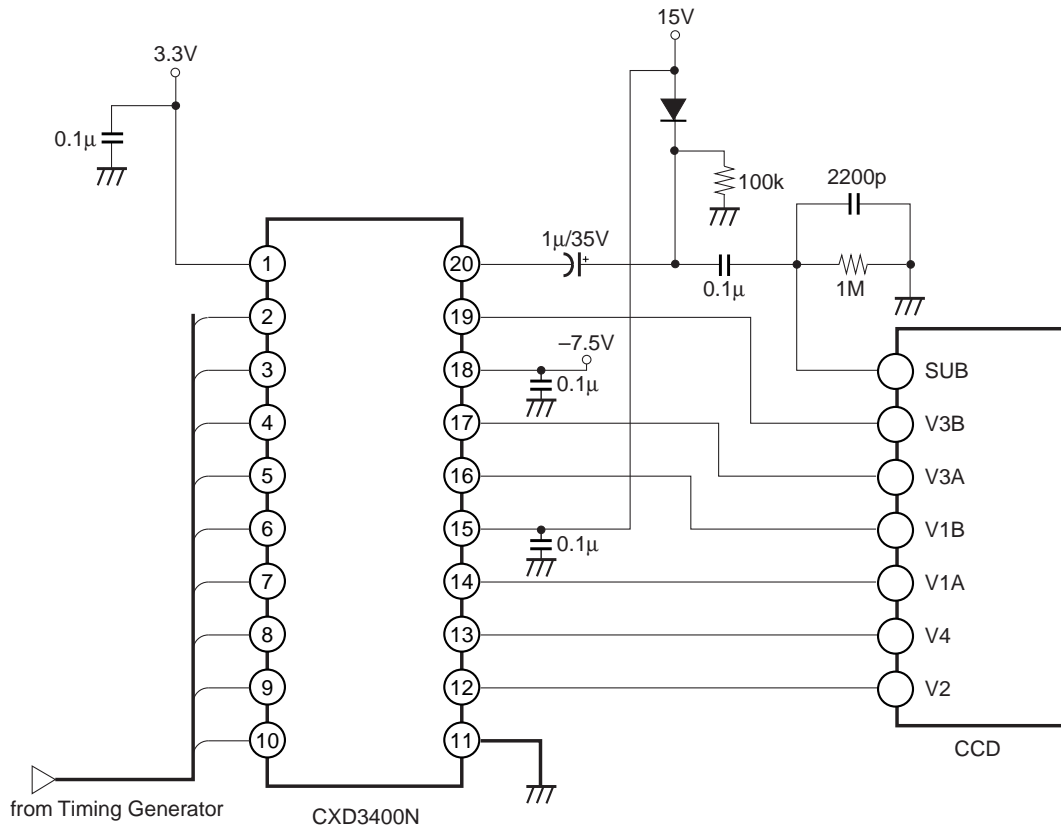
Noise on a Waveform



Measurement Circuit



Application Circuit

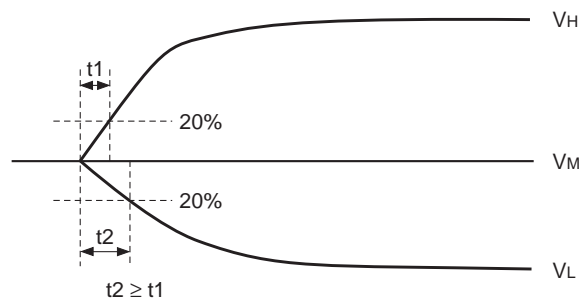


\* See with drive circuit of CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Note with Power-on Sequence

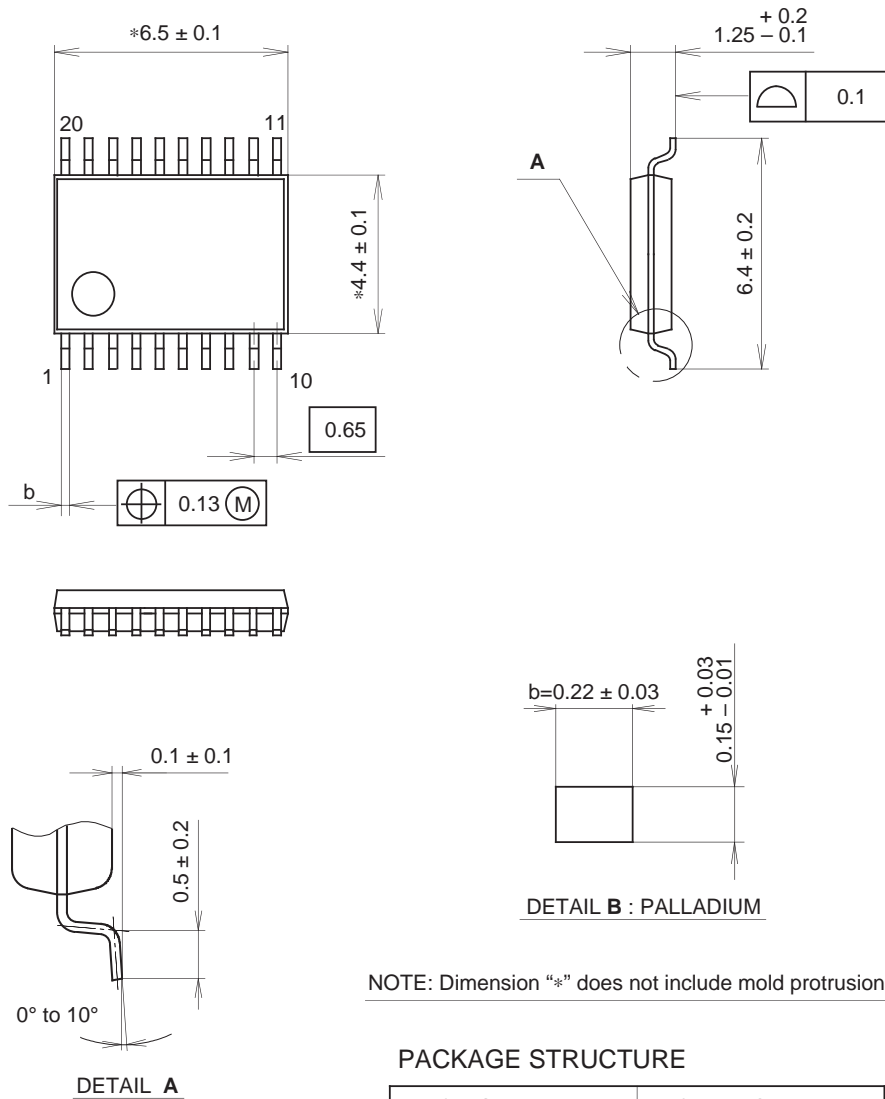
To protect CCD image sensor, rise two power supplies,  $V_L$  and  $V_H$  as follows. Note that rise  $V_{DD}$  first.



Package Outline

Unit: mm

20PIN SSOP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

Sales: Shenzhen Sunnywale Inc, [www.sunnywale.com](http://www.sunnywale.com), [awin@sunnywale.com](mailto:awin@sunnywale.com), Wechat: 9308762