3-Channel SDTV Video Amplifier With 5th-Order Filters and 6-dB Gain

Check for Samples: THS7314

FEATURES

- **3 SDTV Video Amplifiers for CVBS, S-Video, $Y'P'_BP'_R$ 480i/576i, Y'U'V', or G'B'R' (R'G'B')**
- **Integrated Low-Pass Filters**
  - **5th-Order 8.5-MHz (–3dB) Butterworth**
    - **–1dB Passband Bandwidth at 7-MHz**
    - **47dB Attenuation at 27-MHz**
- **Versatile Input Biasing**
  - **DC-Coupled With 285-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp**
  - **Allows AC-Coupled With DC-Biasing**
- **Built-in 6dB Gain (2V/V)**
- **3-V to 5-V Single Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings Within 100-mV From the Rails Allowing AC or DC Output Coupling**
  - **Able to Drive up to 2 Video Lines – 75 Ω**
- **Low 16-mA at 3.3-V Total Quiescent Current**
- **Low Differential Gain/Phase of 0.1% / 0.1°**
- **SOIC-8 Package**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR Output Buffering**
- **USB/Portable Low Power Video Buffering**

DESCRIPTION

Fabricated using the Silicon-Germanium (SiGe) BiCom-III process, the THS7314 is a low power single-supply 3-V to 5-V 3-channel integrated video buffer. It incorporates a 5th-order Butterworth filter which is useful as a DAC reconstruction filter or an ADC anti-aliasing filter. The 8.5-MHz filter is a perfect choice for SDTV video which includes Composite (CVBS), S-Video, Y'U'V', G'B'R' (R'G'B'), and $Y'P'_BP'_R$ 480i/576i.

As part of the THS7314 flexibility, the input can be configured for ac or dc coupled inputs. The 285-mV output level shift to allow for a full sync dynamic range at the output with 0-V input. The AC coupled modes include a transparent sync-tip clamp option for CVBS, Y', and G'B'R' signals with sync. AC-coupled biasing for $C'/P'_B/P'_R$ channels is achieved by adding an external resistor to Vs+.

The THS7314 is the perfect choice for all output buffer applications. Its rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive 2-lines, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 16-mA total quiescent current at 3.3-V makes it an excellent choice for USB powered, portable, or other power sensitive video applications.

The THS7314 is available in a small SOIC-8 package that is RoHS compliant.

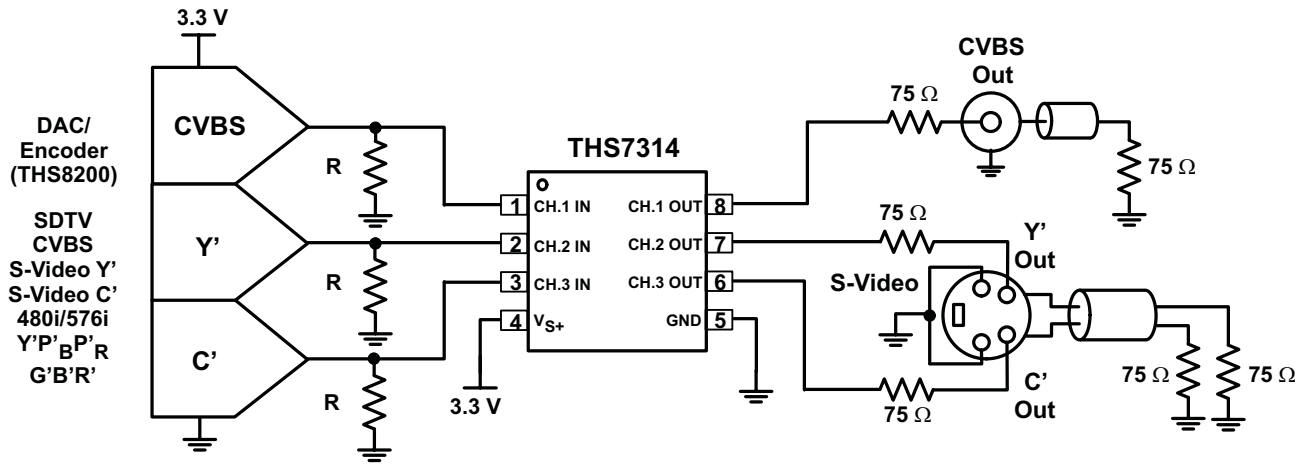


Figure 1. 3.3-V Single-Supply DC-Input/DC Output Coupled Video Line Driver

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

PACKAGED DEVICES	PACKAGE TYPE(1)	TRANSPORT MEDIA, QUANTITY
THS7314D	SOIC-8	Rails, 75
THS7314DR		Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	Supply voltage, V_{S+} to GND		5.5	V
V_I	Input voltage		–0.4 V to V_{S+}	
I_O	Output current		90	mA
	Continuous power dissipation		See Dissipation Rating Table	
T_J	Maximum junction temperature, any condition(2)		150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	ESD ratings	HBM	2000	V
		CDM	1500	
		MM	200	

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

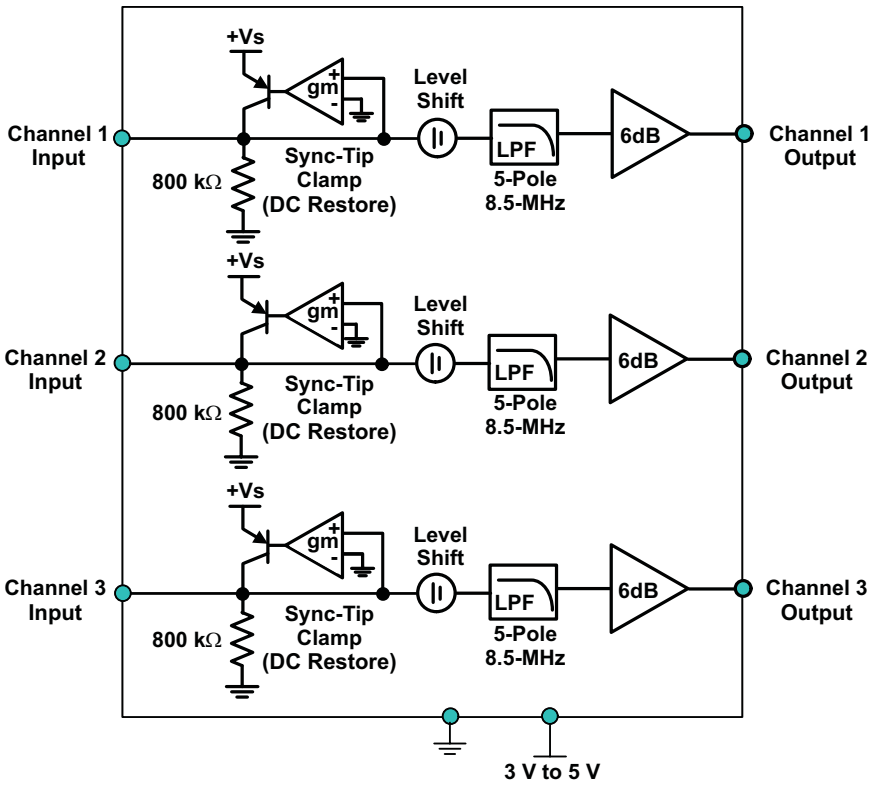
PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = 125°C)	
			T_A = 25°C	T_A = 85°C
SOIC-8 (D)	50	130(2)	769 mW	308 mW

(1) Power rating is determined with a junction temperature of 125°C. This is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(2) This data was taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 196°C/W.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{S+}	Supply voltage	3	5	V
T_A	Ambient temperature	–40	85	°C

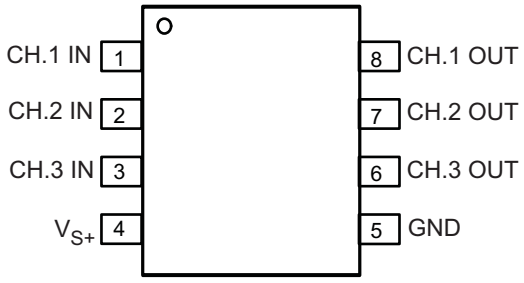
FUNCTIONAL DIAGRAM



PIN CONFIGURATION

SOIC-8 (D)
(TOP VIEW)

THS7314



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO. SOIC-8		
CH. 1 – INPUT	1	I	Video Input – Channel 1
CH. 2 – INPUT	2	I	Video Input – Channel 2
CH. 3 – INPUT	3	I	Video Input – Channel 3
+Vs	4	I	Positive Power Supply Pin – connect to 3 V to 5 V.
GND	5	I	Ground Pin for all internal circuitry.
CH. 3 – OUTPUT	6	O	Video Output – Channel 3
CH. 2 – OUTPUT	7	O	Video Output – Channel 2
CH. 1 – OUTPUT	8	O	Video Output – Channel 1

ELECTRICAL CHARACTERISTICS V_{S+} = 3.3 V:

R_L = 150Ω to GND – Reference Figure 2 and Figure 3 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-signal bandwidth (–3dB)	V_O – 0.2 V_{PP} (1)	8.5	6.7/10.3	6.6/10.5	6.5/10.6	MHz	Min/Max
Large-signal bandwidth (–3dB)	V_O – 2 V_{PP} (1)	8.5	6.7/10.3	6.6/10.5	6.5/10.6	MHz	Min/Max
–1dB Passband bandwidth		7				MHz	Typ
Attenuation	f = 6 MHz (2)	0.45	–0.3/2.4	–0.35/2.5	–0.4/2.6	dB	Min/Max
With respect to 100kHz	f = 27 MHz (2)	47	36	35	34	dB	Min
Group delay	f = 100 kHz	57				ns	Typ
Group delay variation with respect to 100kHz	f = 5.1 MHz	10.2				ns	Typ
Channel-to-channel delay		0.3				ns	Typ
Differential gain	NTSC / PAL	0.1 / 0.1				%	Typ
Differential phase	NTSC / PAL	0.1 / 0.1				°	Typ
Total harmonic distortion	f = 1 MHz; V_O = 2 V_{PP}; AC coupled I/O	–66				dB	Typ
Signal to noise ratio	NTC-7 Weighting, 100kHz to 4.2MHz	79.6				dB	Typ
Channel-to-channel crosstalk	f = 1 MHz, Worst Case Channels	–60				dB	Typ
AC Gain – All channels		6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output Impedance	f = 5 MHz	0.63				Ω	Typ
DC PERFORMANCE							
Biased output voltage	V_I = 0 V	285	210/370	200/380	190/390	mV	Min/Max
Input voltage range	DC input, limited by output	–0.1/1.46				V	Typ
Sync tip clamp charge current	V_I = –0.1 V	180				µA	Typ
Input resistance		800				kΩ	Typ
Input capacitance		2				pF	Typ
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to Midrail	3.15				V	Typ
	R_L = 150 Ω to GND	3.1	2.85	2.75	2.75	V	Min
	R_L = 75 Ω to Midrail	3.1				V	Typ
	R_L = 75 Ω to GND	3				V	Typ
Low output voltage swing	R_L = 150 Ω to Midrail (V_I = –0.2V)	0.15				V	Typ
	R_L = 150 Ω to GND (V_I = –0.2V)	0.1	0.17	0.2	0.21	V	Max
	R_L = 75 Ω to Midrail (V_I = –0.2V)	0.3				V	Typ
	R_L = 75 Ω to GND (V_I = –0.2V)	0.1				V	Typ
Output current (sourcing)	R_L = 10 Ω to Midrail	80				mA	Typ
Output current (sinking)	R_L = 10 Ω to Midrail	70				mA	Typ
POWER SUPPLY							
Maximum operating voltage	See (1)	3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage	See (1)	3.3	2.85	2.85	2.85	V	Min
Maximum quiescent current	V_I = 0V	16	20	22	24	mA	Max
Minimum quiescent current	V_I = 0V	16	12	11.6	11	mA	Min
Power Supply Rejection (+PSRR)		52				dB	Typ

(1) The Min/Max values listed for this specification are specified by design and characterization only.
(2) 3.3-V Supply Filter specifications are specified by 100% testing at 5-V supply along with design and characterization only.

ELECTRICAL CHARACTERISTICS V_{S+} = 5 V:

R_L = 150Ω to GND – Reference Figure 2 and Figure 3 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small-signal bandwidth (–3dB)	V_O – 0.2 V_{PP} (1)	8.5	6.7/10.3	6.6/10.5	6.5/10.6	MHz	Min/Max
Large-signal bandwidth (–3dB)	V_O – 2 V_{PP} (1)	8.5	6.7/10.3	6.6/10.5	6.5/10.6	MHz	Min/Max
–1dB Passband bandwidth		7				MHz	Typ
Attenuation	f = 6 MHz	0.45	–0.3/2.4	–0.35/2.5	–0.4/2.6	dB	Min/Max
With respect to 100kHz	f = 27 MHz	47	36	35	34	dB	Min
Group delay	f = 100 kHz	57				ns	Typ
Group delay variation with respect to 100kHz	f = 5.1 MHz	10				ns	Typ
Channel-to-channel delay		0.3				ns	Typ
Differential gain	NTSC / PAL	0.1 / 0.1				%	Typ
Differential phase	NTSC / PAL	0.1 / 0.1				°	Typ
Total harmonic distortion	f = 1 MHz; V_O =2 V_{PP}	–66				dB	Typ
Signal to noise ratio	NTC-7 Weighting, 100kHz to 4.2MHz	79.6				dB	Typ
Channel-to-channel crosstalk	f = 1 MHz, Worst Case Channels	–60				dB	Typ
AC Gain – All channels		6	5.7/6.3	5.65/6.35	5.65/6.35	dB	Min/Max
Output Impedance	f = 5 MHz	0.62				Ω	Typ
DC PERFORMANCE							
Biased output voltage	V_I = 0 V	290	210/370	200/380	190/390	mV	Min/Max
Input voltage range	Limited by output	–0.1/2.3				V	Typ
Sync tip clamp charge current	V_I = –0.1V	180				µA	Typ
Input resistance		800				kΩ	Typ
Input capacitance		2				pF	Typ
OUTPUT CHARACTERISTICS							
High output voltage swing	R_L = 150 Ω to Midrail	4.85				V	Typ
	R_L = 150 Ω to GND	4.7	4.2	4.1	4.1	V	Min
	R_L = 75 Ω to Midrail	4.7				V	Typ
	R_L = 75 Ω to GND	4.5				V	Typ
Low output voltage swing	R_L = 150 Ω to Midrail (V_I = –0.2V)	0.2				V	Typ
	R_L = 150 Ω to GND (V_I = –0.2V)	0.12	0.23	0.26	0.27	V	Max
	R_L = 75 Ω to Midrail (V_I = –0.2V)	0.35				V	Typ
	R_L = 75 Ω to GND (V_I = –0.2V)	0.1				V	Typ
Output current (sourcing)	R_L = 10 Ω to Midrail	90				mA	Typ
Output current (sinking)	R_L = 10 Ω to Midrail	85				mA	Typ
POWER SUPPLY							
Maximum operating voltage	See (1)	5	5.5	5.5	5.5	V	Max
Minimum operating voltage	See (1)	5	2.85	2.85	2.85	V	Min
Maximum quiescent current	V_I = 0V	17	22	24	25	mA	Max
Minimum quiescent current	V_I = 0V	17	12.5	12	11.5	mA	Min
Power Supply Rejection (+PSRR)		55				dB	Typ

(1) The Min/Max values listed for this specification are specified by design and characterization only.

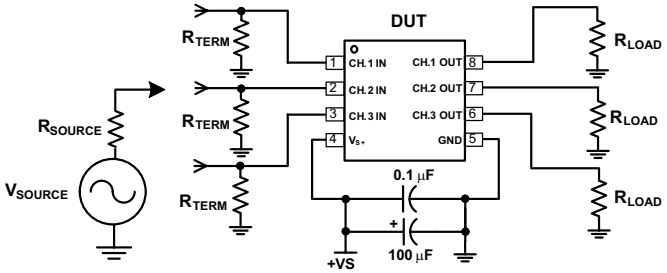


Figure 2. DC Coupled Input and Output Test Circuit

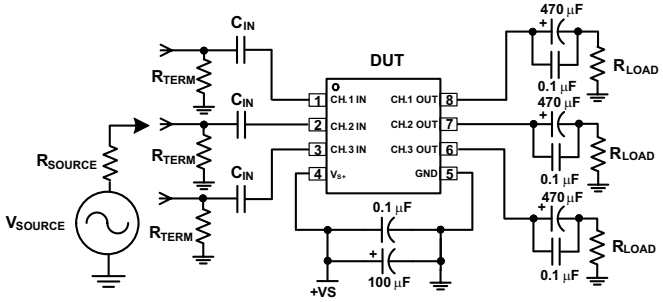


Figure 3. AC Coupled Input and Output Test Circuit

TYPICAL CHARACTERISTICS

SMALL-SIGNAL GAIN vs FREQUENCY

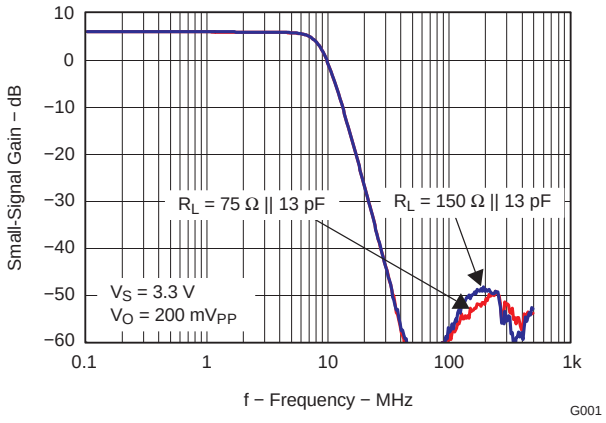


Figure 4.

PHASE vs FREQUENCY

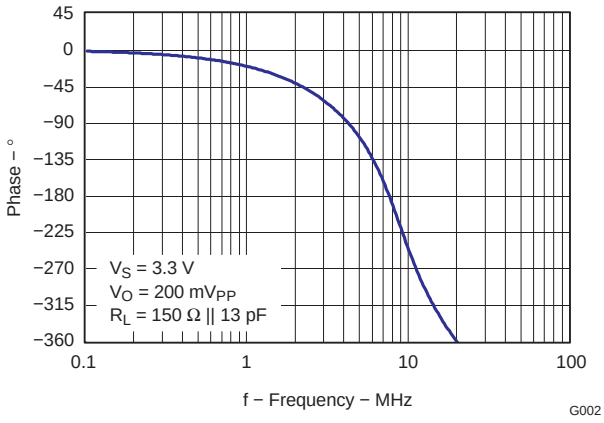


Figure 5.

SMALL-SIGNAL GAIN vs FREQUENCY

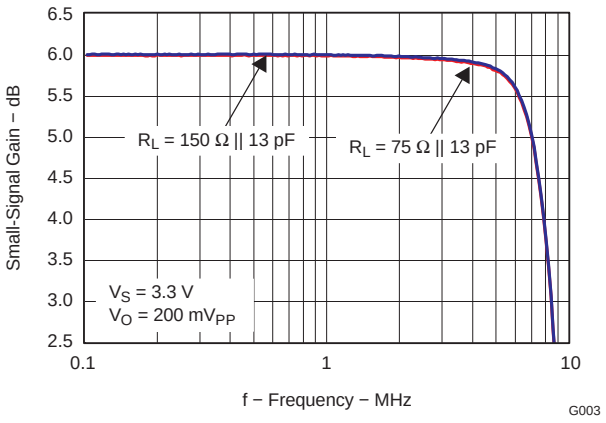


Figure 6.

GROUP DELAY vs FREQUENCY

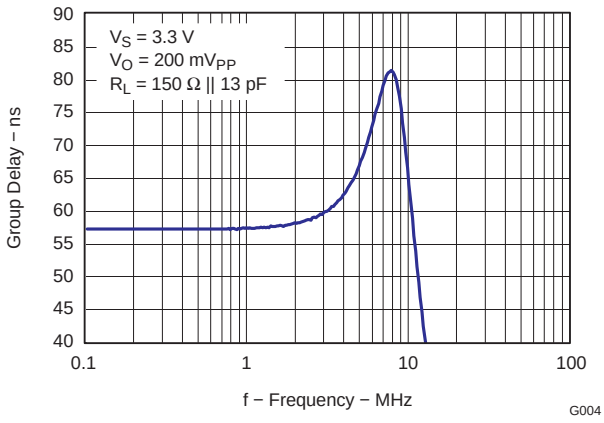


Figure 7.

SMALL-SIGNAL PULSE RESPONSE vs TIME

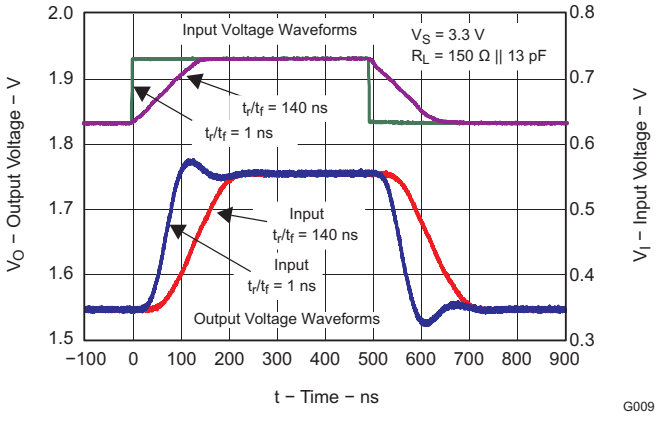


Figure 8.

LARGE-SIGNAL PULSE RESPONSE vs TIME

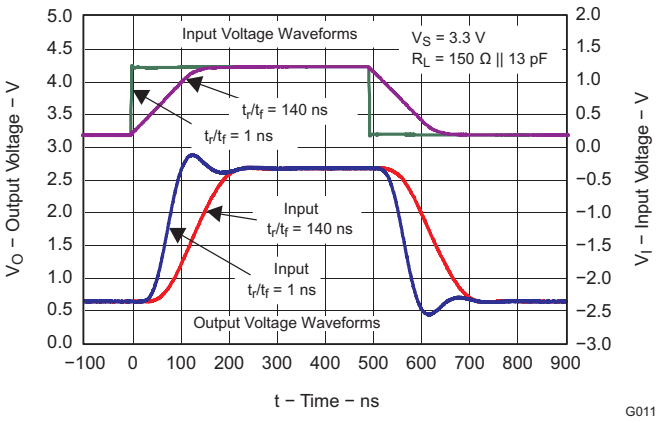


Figure 9.

TYPICAL CHARACTERISTICS (continued)

HD2 vs OUTPUT VOLTAGE

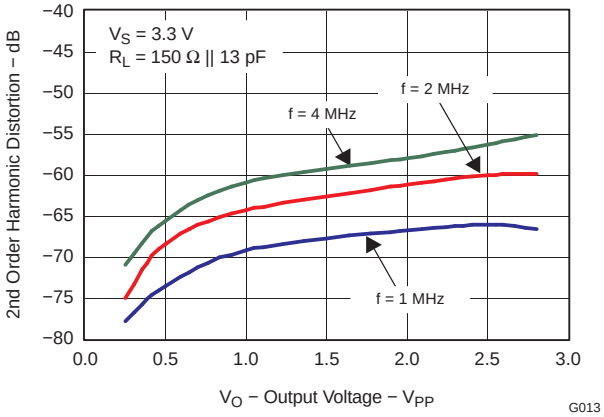


Figure 10.

HD3 vs OUTPUT VOLTAGE

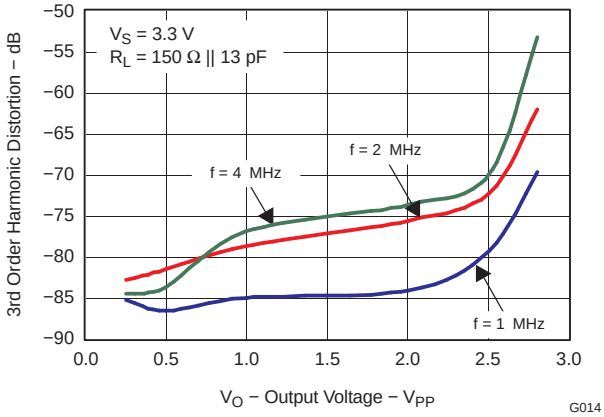


Figure 11.

SLEW RATE vs OUTPUT VOLTAGE

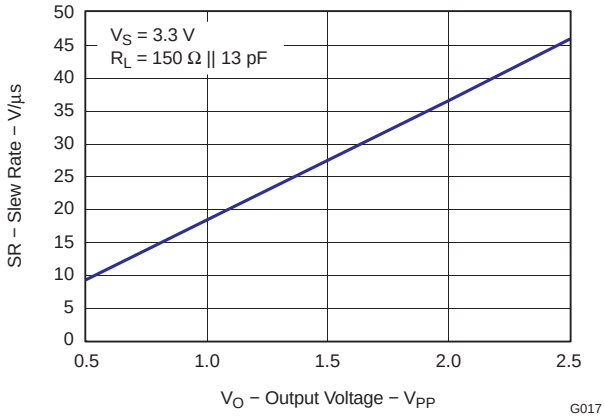


Figure 12.

CROSSTALK vs FREQUENCY

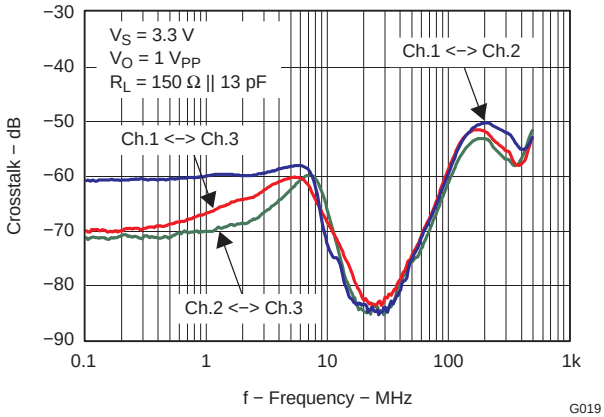


Figure 13.

SMALL-SIGNAL GAIN vs FREQUENCY

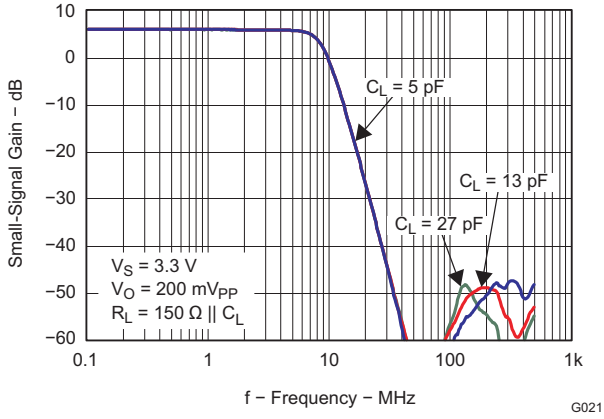


Figure 14.

OUTPUT IMPEDANCE vs FREQUENCY

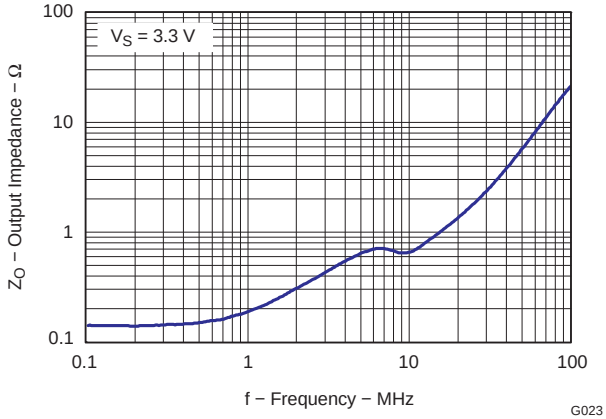


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL GAIN vs FREQUENCY

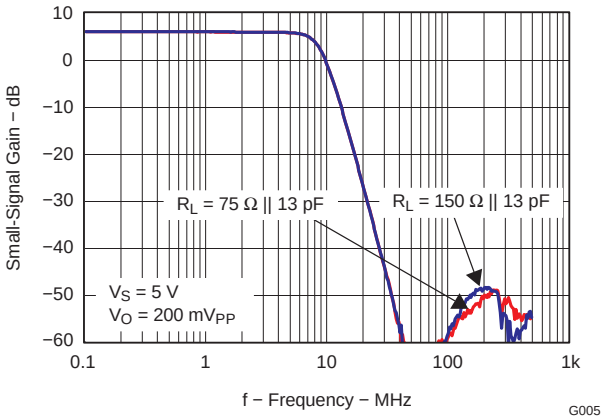


Figure 16.

PHASE vs FREQUENCY

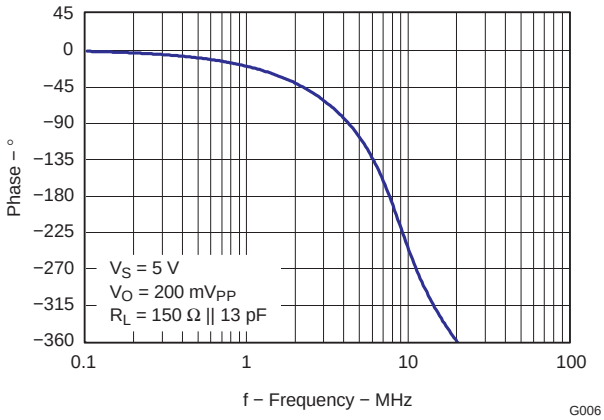


Figure 17.

SMALL-SIGNAL GAIN vs FREQUENCY

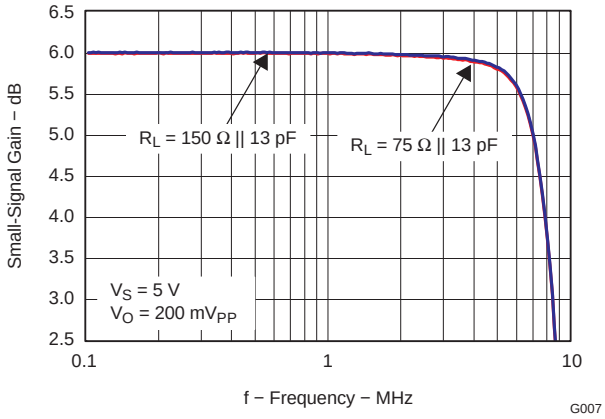


Figure 18.

GROUP DELAY vs FREQUENCY

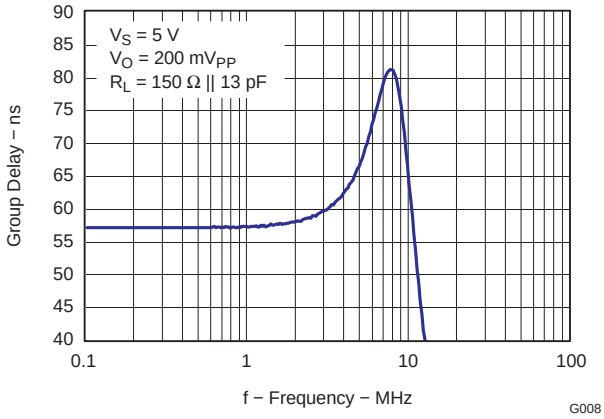


Figure 19.

SMALL-SIGNAL PULSE RESPONSE vs TIME

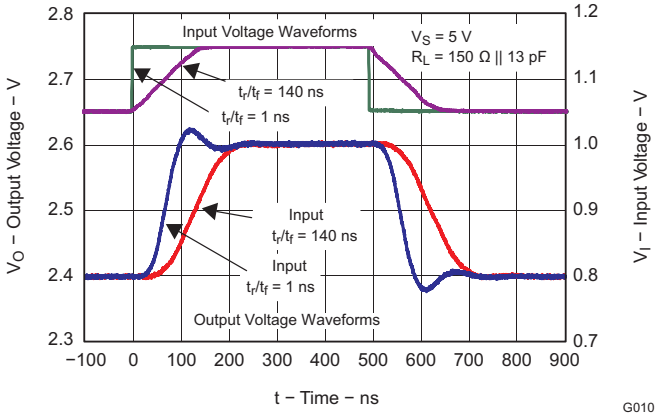


Figure 20.

LARGE-SIGNAL PULSE RESPONSE vs TIME

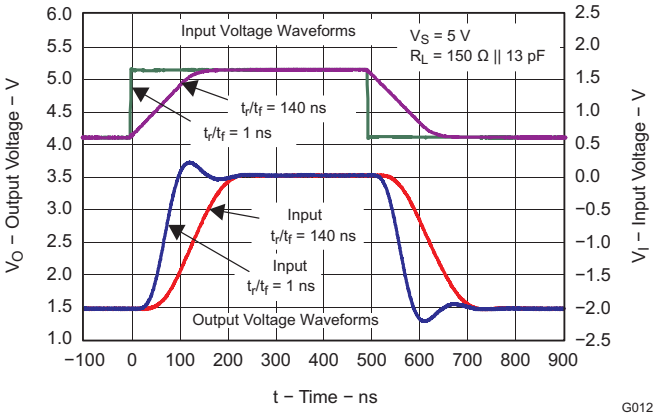


Figure 21.

TYPICAL CHARACTERISTICS (continued)

HD2 vs OUTPUT VOLTAGE

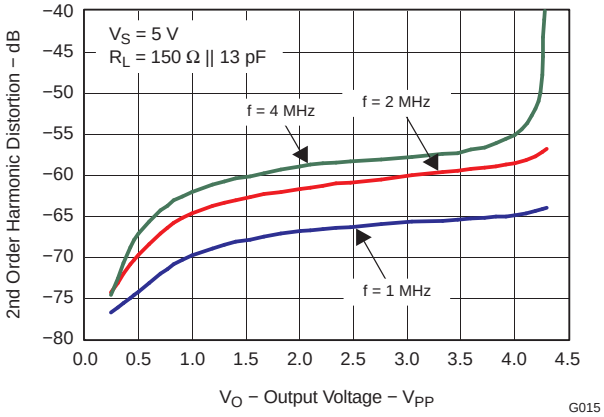


Figure 22.

HD3 vs OUTPUT VOLTAGE

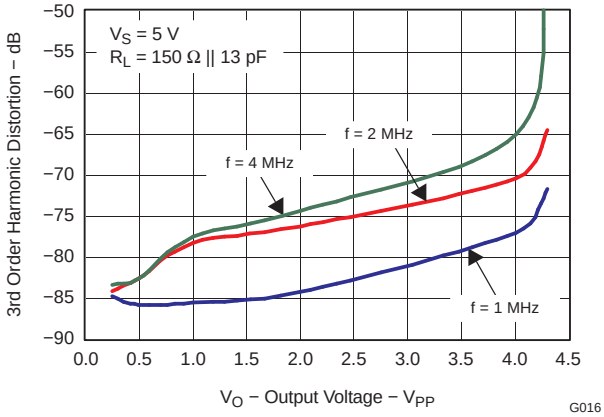


Figure 23.

SLEW RATE vs OUTPUT VOLTAGE

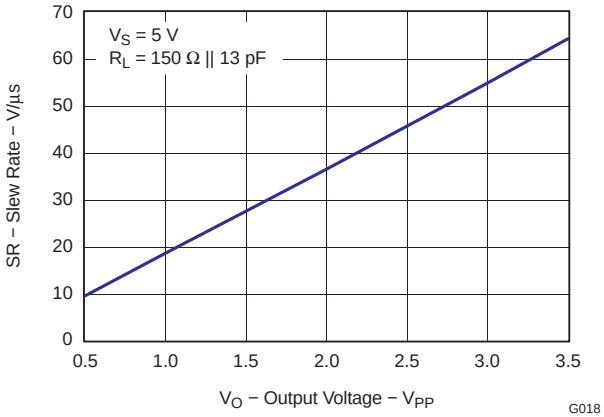


Figure 24.

CROSSTALK vs FREQUENCY

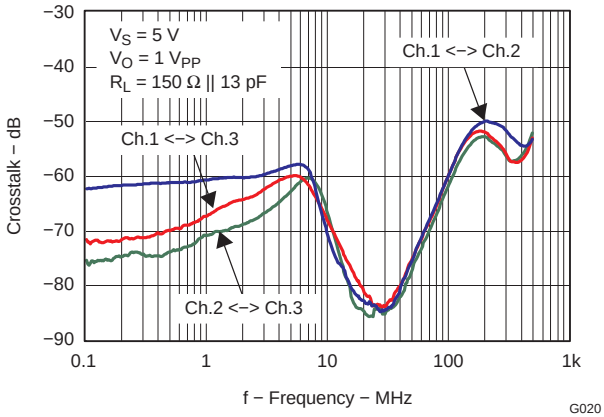


Figure 25.

SMALL-SIGNAL GAIN vs FREQUENCY

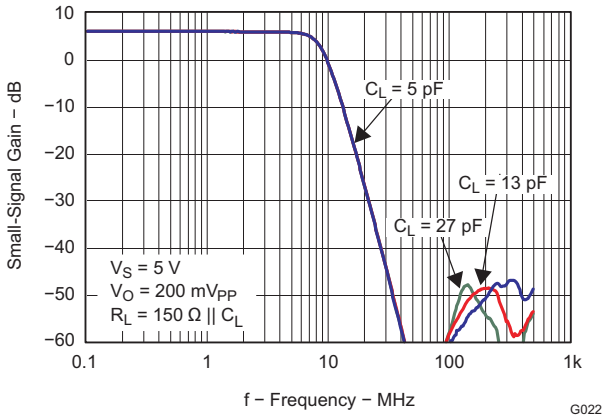


Figure 26.

OUTPUT IMPEDANCE vs FREQUENCY

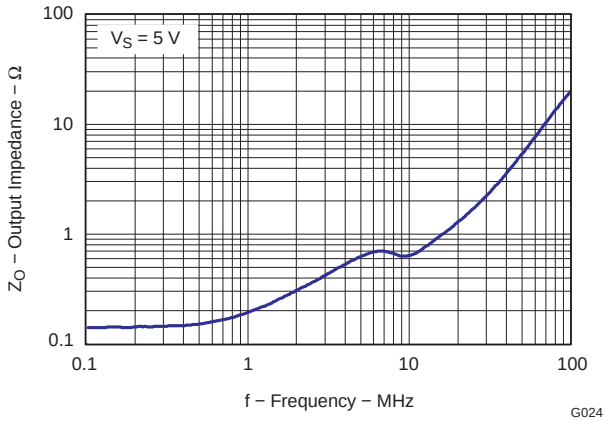


Figure 27.

APPLICATION INFORMATION

The THS7314 is targeted for standard definition video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal is an important design parameter of the THS7314. Built on the Silicon Germanium (SiGe) BiCom-3 process, the THS7314 incorporates many features not typically found in integrated video parts while consuming very low power.

The THS7314 has the following features:

- Single-Supply 3-V to 5-V operation with low total quiescent current of 16-mA at 3.3-V and 17-mA at 5-V.
- Input configuration accepting DC + Level shift, AC Sync-Tip Clamp, or AC-Bias.
- AC-Biasing is accomplished with the use of external pull-up resistor to the positive power supply.
- 5^{th}-Order Low Pass Filter for DAC reconstruction or ADC image rejection:
  - 8.5-MHz for NTSC, PAL, SECAM, Composite (CVBS), S-Video Y'C', 480i/576i $Y'P'_BP'_R$, and G'B'R' (R'G'B') signals.
- Internal fixed gain of 2 V/V (6 dB) buffer that can drive up to 2 video lines with dc coupling or traditional ac coupling.
- Signal flow-through configuration using an 8-pin SOIC package that complies with the latest lead-free (RoHS compatible) and Green manufacturing requirements.

OPERATING VOLTAGE

The THS7314 is designed to operate from 3-V to 5-V over a –40°C to 85°C temperature range. The impact on performance over the entire temperature range is negligible due to the implementation of thin film resistors and high quality – low temperature coefficient capacitors. The design of the THS7314 allows operation down to 2.85-V, but for best results the use of a 3-V supply or greater should be used to ensure there are no issues with headroom or clipping.

The power supply pins should have a 0.1 µF to 0.01 µF capacitor placed as close as possible to these pins. Failure to do so may result in the THS7314 outputs ringing or have an oscillation. Additionally, a large capacitor, such as 22 µF to 100 µF, should be placed on the power supply line to minimize interference with 50/60 Hz line frequencies.

INPUT VOLTAGE

The THS7314 input range allows for an input signal range from –0.2V to about (V_{S+} – 1.5V). But, due to the internal fixed gain of 2 V/V (6 dB) and the internal level shift of nominally 145-mV, the output will generally be the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.2V to 3.5V. But due to the gain and level shift, the linear output range limits the allowable linear input range to be from about –0.1V to 2.3V .

INPUT OVERVOLTAGE PROTECTION

The THS7314 is built using a very high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 28.

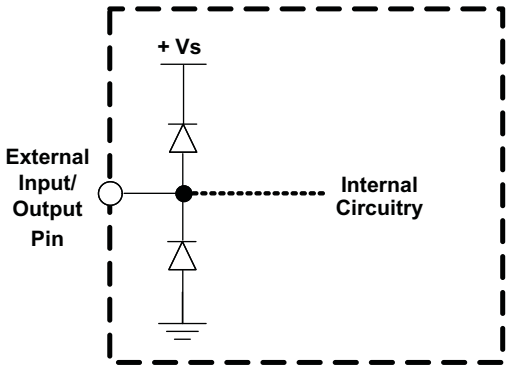


Figure 28. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30-mA of continuous current when overdriven.

TYPICAL CONFIGURATION and VIDEO TERMINOLOGY

A typical application circuit using the THS7314 as a video buffer is shown in Figure 29. It shows a DAC (or encoder such as the THS8200) driving the three input channels of the THS7314. Although the S-Video Y'C' channels and the Composite video channel of a Standard Definition video (SD) system are shown, these channels can easily be the $Y'P'_BP'_R$ (sometimes labeled Y'U'V' or incorrectly labeled $Y'C'_BC'_R$) signals of a 480i or 576i system. These signals can also be G'B'R' (R'G'B') signals or other variations.

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason is to account for the definition of luminance as stipulated by the CIE – International Commission on Illumination. Video departs from true luminance since a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus luminance (Y) is not maintained providing a difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the non-linear R'G'B' terms and thus it is nonlinear. Chominance (C) is derived from linear RGB giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B / P'_R / U' / V') are also referenced this way to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems sync is embeded on all three channels, but may not always be the case in all systems.

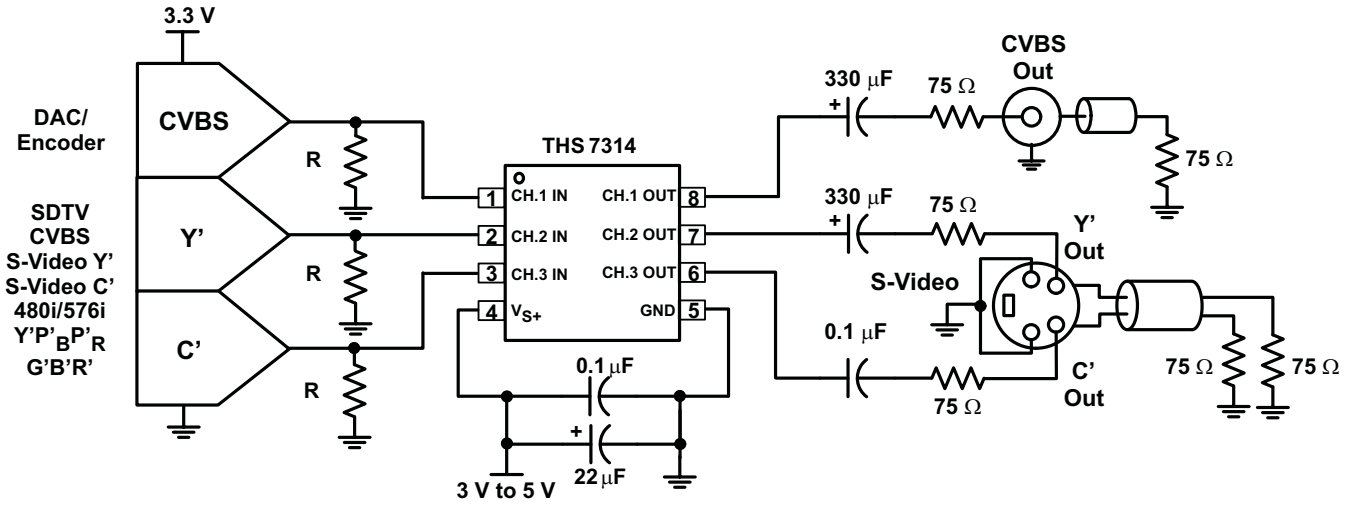


Figure 29. Typical SDTV CVBS/Y'/C' Inputs From DC-Coupled Encoder/DAC With AC-Coupled Line Driving

INPUT MODE OF OPERATION – DC

The inputs to the THS7314 allows for both ac-coupled and dc-coupled inputs. Many DACs or Video Encoders can be dc connected to the THS7314. One of the drawbacks to dc coupling is when 0-V is applied to the input. Although the input of the THS7314 allows for a 0-V input signal with no issues, the output swing of a traditional amplifier cannot yield a 0-V signal resulting in possible clipping. This is true for any single-supply amplifier due to the limitations of the output transistors. Both CMOS and bipolar transistors cannot go to 0-V while sinking current. This trait of a transistor is also the same reason why the highest output voltage is always less than the power supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync amplitudes) on the video signal. A problem occurs if the receiver of this video signal uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much – resulting in too much luma and/or chroma amplitude gain correction. This may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. But, it is good engineering design practice to ensure saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation/clipping problems, the THS7314 has a 145-mV input level shift feature. This feature takes the input voltage and adds an internal +145-mV shift to the signal. Since the THS7314 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is about 290-mV. The THS7314 rail-to-rail output stage can create this output level while connected to a typical video load with AC or DC coupling. This ensures that no saturation / clipping of the sync signals occur. This is a constant shift regardless of the input signal. For example, if a 1-V input is applied, the output is at 2.29-V.

Because the internal gain is fixed at 6 dB, the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3-V, the maximum output is about 2.9-V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ((2.9V / 2) – 0.145V) = 1.305V. This is true for up to the maximum recommended 5-V power supply that allows about a ((4.9V / 2) – 0.145V) = 2.305V input range while avoiding clipping on the output.

The input impedance of the THS7314 in this mode of operation is dictated by the internal 800-kΩ pull-down resistor. This is shown in Figure 30. Note that the internal voltage shift does not appear at the input pin, only the output pin.

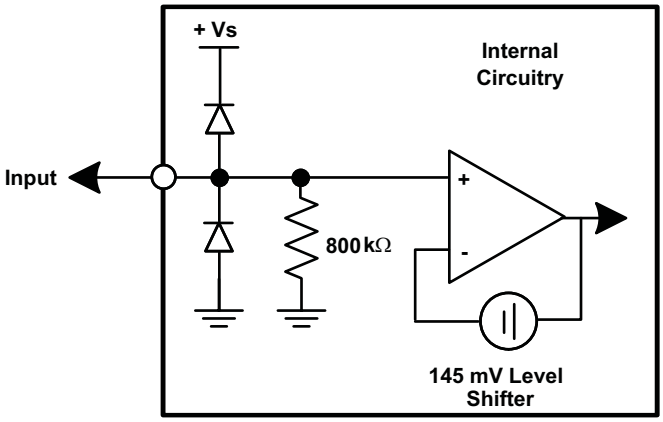


Figure 30. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION – AC SYNC TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. These DACs typically only sink current rather than the more traditional current sourcing DAC where the resistor is referenced to ground. The resulting video signals can be too high of a voltage for a dc-coupled video buffer to function properly. To account for this scenario the THS7314 incorporates a sync-tip clamp circuit. This function requires a capacitor (nominally 0.1 µF) to be in series with the input. Note that while the term sync-tip-clamp is used throughout this document, it should be noted that the THS7314 is be better termed as a dc-restoration circuit based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7314 has an internal control loop which sets the lowest input applied voltage to clamp at ground (0-V). By setting the reference at 0-V, the THS7314 allows a dc-coupled input to also function. Hence the STC is considered transparent since it does not operate unless the input signal goes below ground. The signal then goes thru the same 145-mV level shifter resulting in an output voltage low level of 290-mV. If the input signal tries to go below the 0-V, the internal control loop of the THS7314 will source up to 3-mA of current to increase the input voltage level on the THS7314 input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes high impedance.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals or reflections found in poor PCB layouts. Ideally the STC should not react to the overshoot voltage of the input signal. Otherwise, this could result in clipping on the rest of the video signal as it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7314 has an internal low-pass filter as shown in Figure 31. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general it is about a 100-ns delay. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage but rather the flat portion of the sync signal.

As a result of this delay, the sync may have an apparent voltage shift. The amount of shift is dependant upon the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because the sync is primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems.

While this feature may not fully eliminate overshoot issues on the input signal for excessive overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (ex: 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage appearing at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This helps ensure a very robust STC system.

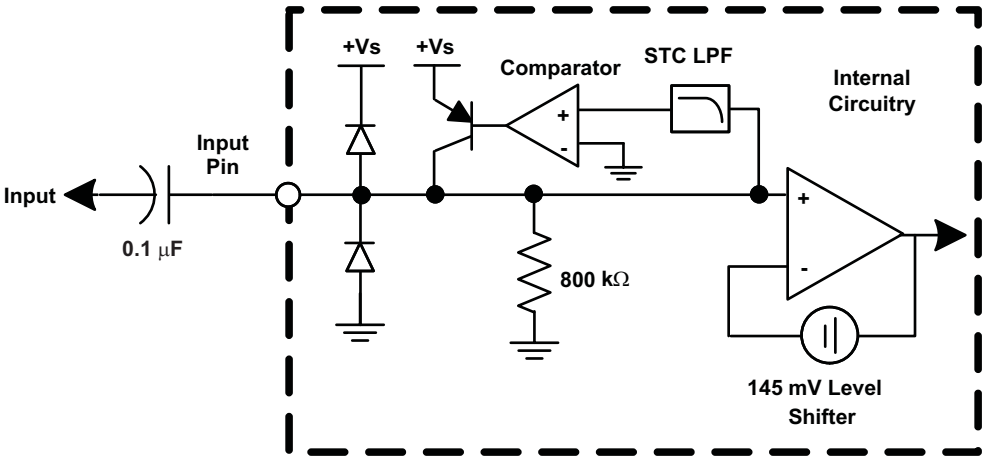


Figure 31. Equivalent AC Sync Tip Clamp Input Circuit

When the AC Sync-Tip-Clamp (STC) operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7314 will source current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally—supplying up to 3 mA of current. Thus the time to re-establish the proper STC voltage can be fast. If the difference is small, then the source current is also small to account for minor voltage droop.

But, what happens if the input signal goes above the 0-V input level? The problem is the video signal is always above this level, and must not be altered in any way. But if the Sync level of the input signal is above this 0-V level, then the internal discharge (sink) current will discharge the ac-coupled bias signal to the proper 0-V level.

This discharge current must not be large enough to alter the video signal appreciably, or picture quality issues may arise. This is often seen by looking at the tilt (aka droop) of a constant luma signal being applied and looking at the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of line tilt (droop).

If the discharge current is small, the amount of tilt is low which is good. But, the amount of time for the system to capture the sync signal could be too long. This is also termed hum rejection. Hum arises from the AC line voltage frequency of 50-Hz or 60-Hz. The value of the discharge current and the AC-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc-coupling and ac-coupling in the same part, the THS7314 incorporates an 800-kΩ resistor to ground. Although a true constant current sink is preferred over a resistor, there are significant issues when the voltage is near ground. This can cause the current sink transistor to saturate and cause potential problems with the signal. This resistor is large enough as to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is used. If the video signal is 1 V, then there is 1 V / 800 kΩ = 1.25-µA of discharge current. If more hum rejection is desired or there is a loss of sync occurring, then decrease the 0.1-µF input coupling capacitor. A decrease form 0.1 µF to 0.047 µF increases the hum rejection by a factor of 2.1. Alternatively an external pull-down resistor to ground may be added which decreases the overall resistance, and ultimately increases the discharge current.

To ensure proper stability of the AC STC control loop, the source impedance must be less than 1-kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop to ring and this ringing may appear on the output of the THS7314. Because most DACs or encoders use resistors to establish the voltage, which are typically less than 300-Ω, then meeting the <1kΩ requirement is easily done. But, if the source impedance looking from the THS7314 input perspective is high, then add a 1-kΩ resistor to GND to ensure proper operation of the THS7314.

INPUT MODE OF OPERATION – AC BIAS

Sync tip clamps work great for signals that have horizontal and/or vertical syncs associated with them. But, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7314. This function is accomplished with the THS7314 by adding an external pull-up resistor to the positive power supply as shown in Figure 32.

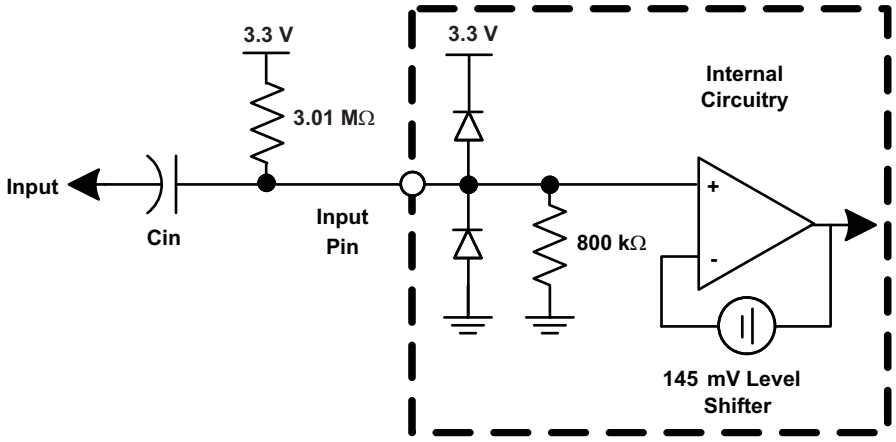


Figure 32. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is approxiamately equal to:

$$V_{DC} = V_S\left(\frac{800k}{800k + R_{PU}}\right) \quad (1)$$

The THS7314 allowable input range is approximately 0-V to (+Vs – 1.5V) which allows for a wide input voltage range. As such, the input dc-bias point is very flexible with the output dc-bias point being the primary factor. For example, if the output dc-bias point is desired to be mid-rail on a 3.3-V supply, then the input dc-bias point should be (1.65V – 290mV) /2 = 0.68V. Thus, the pull-up resistor calculates to about 3.01-MΩ resulting in 0.693V. If the output dc-bias point is desired to be 0.68-V with a 5-V power supply, then the pull-up resistor calculates to about 5.1-MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should take this into account. For the 0.693-V example above using an ideal 3.01-MΩ resistor, the input dc-bias voltage is about 0.693V ± 0.11V.

One other issue that must be taken into account is the dc-bias point is a function of the power supply. As such, there is an impact on PSRR on the system. To help reduce the impact, the input capacitor combined with the pull-up resistance functions as a low-pass filter. Additionally, the time to charge the capacitor to the final dc-bias point is also a function of the pull-up resistor and the input capacitor. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. It is good to have this high pass filter at about 3-Hz to minimize any potential droop on a P'_B, P'_R, or non-sync B' or R' signal. A 0.1µF input capacitor with a 3.01-MΩ pull-up resistor equates to about a 2.5-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and non-sync B' and/or R' signals.

OUTPUT MODE OF OPERATION – DC COUPLED

The THS7314 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors as shown in Figure 33. This offers the best line tilt and field tilt (or droop) performance since there is no ac-coupling occurring. Keep in mind that if the input is ac-coupled, then the resulting tilt due to the input ac-coupling will still be seen on the output irregardless of the output coupling. The 80-mA output current drive capability of the THS7314 was designed to drive two video lines simultaneously – essentially a 75-Ω load – while keeping the output dynamic range as wide as possible.

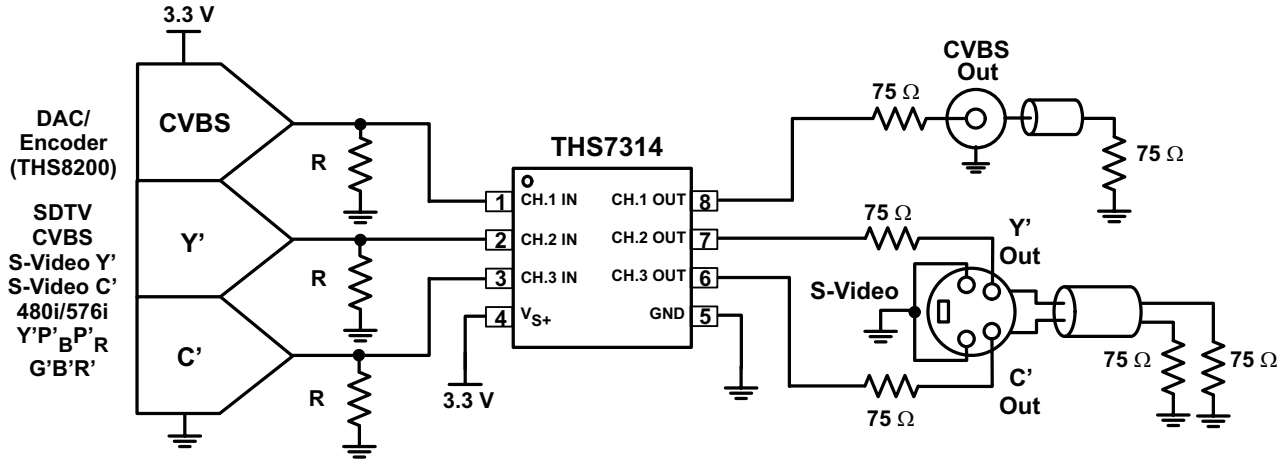


Figure 33. Typical SDTV CVBS/Y'/C' System with DC-Coupled Line Driving

One concern of dc-coupling is if the line is terminated to ground. If the ac-bias input configuration is used, the output of the THS7314 will have a dc-bias on the output. With 2 lines terminated to ground, this creates a dc-current path to exist which results in a slightly decreased high output voltage swing and resulting in an increase in power dissipation of the THS7314. While the THS7314 was designed to operate with a junction temperature of up to 125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long term reliability could suffer. Although this configuration only adds less then 10 mW of power dissipation per channel, the overall low power dissipation of the THS7314 design will minimize potential thermal issues even when using the SOIC package at high ambient temperatures.

Another concern of DC coupling is the blanking level voltage of the video signal. The EIA specification dictates that the blanking level shall be 0V ± 1V. While there is some question as to whether this voltage is at the output of the amplifier or at the reciever, it is generally regarded to be measured at the reciever side of a system as the rest of the specification voltage requirements are given with doubly terminated connections present. With the rail-to-rail output swing capability, combined with the 145-mV input level shift, meeting this requirement is easily accomplished. Thus, elimination of the large output AC coupling capacitor can be done while still meeting the EIA specification. This can save PCB area and costs.

Note that the THS7314 can drive the line with dc-coupling irregardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output – typically 75-Ω. This helps isolate capacitive loading effects from the THS7314 output. Failure to isolate capacitive loads may result in instabilities with the output buffer potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7314 output pins should be kept below 25-pF.

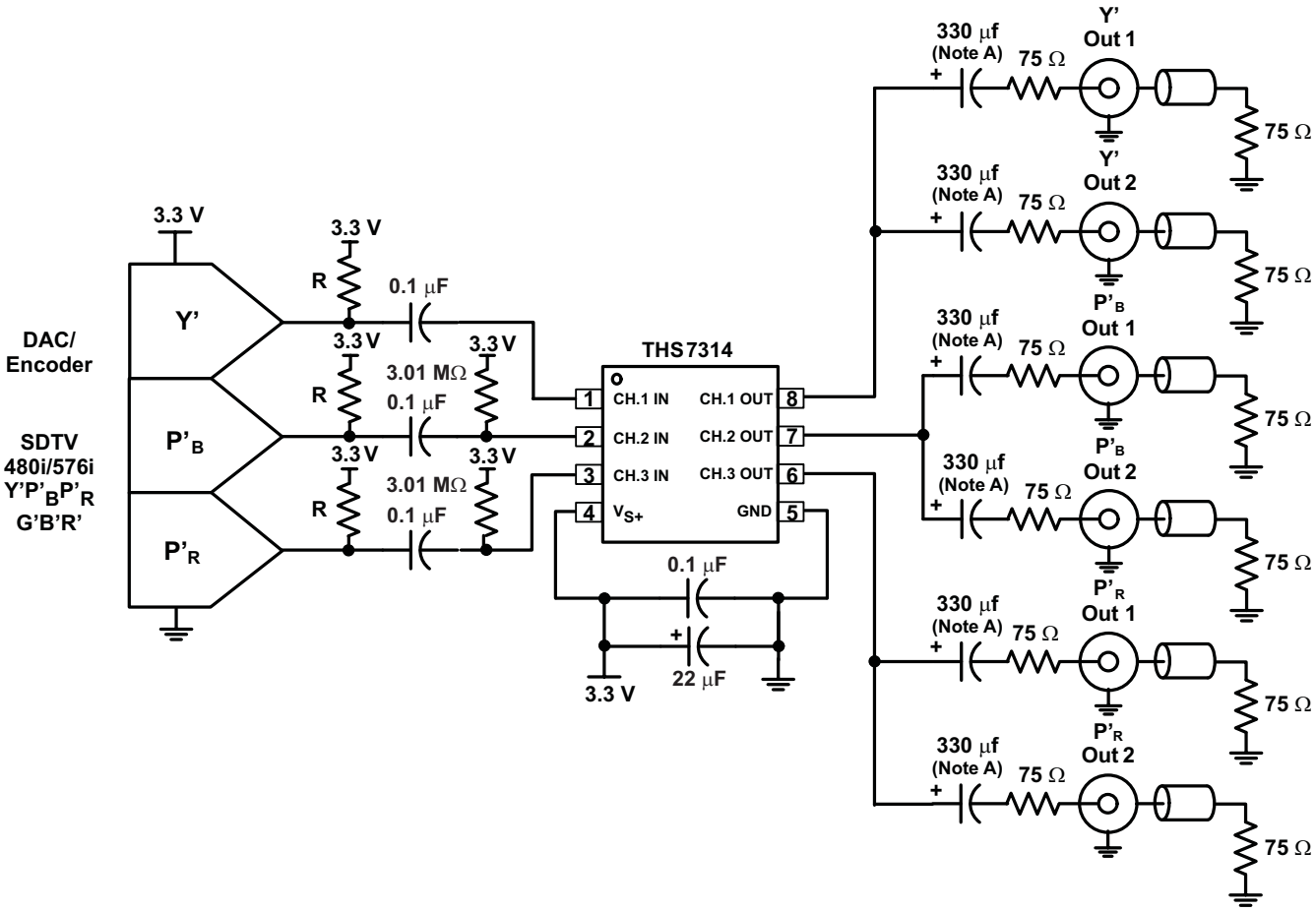
OUTPUT MODE OF OPERATION – AC COUPLED

The most common method of coupling the video signal to the line is with the use of a large capacitor. This capacitor is typically between 220-µF and 1000-µF, although 470-µF is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is done for several reasons, but the most common reason to do this is to ensure full inter-operability with the receiving video system. This minimizes possible ground loops. It also ensures that irregardless of the reference dc voltage used on the transmit side, the receive side will re-establish the dc reference voltage to its own requirements.

Just like the DC output mode of operation, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. If 2 lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components as shown in Figure 34. This helps ensure line-to-line dc isolation and the potential problems as stipulated above. Using a single 1000-µF capacitor for 2-lines can be done, but there is a chance for ground loops and interference to be created between the two receivers.

Lastly, due to the edge rates and frequencies of operation, it is recommended – but not required – to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large value capacitors are most commonly aluminum electrolytic. These capacitors have significantly large ESR (equivalent series resistance), and their impedance at high frequencies is large due to the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help pass these high frequency (>1 MHz) signals with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system are not required to go as low – or as high of a frequency – as the luma channels. Thus the capacitor values of the chroma line(s) can be smaller – such as 0.1-µF.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.1-µF or 0.01-µF capacitor in parallel with these large capators.

B. Current sinking DAC / Encoder shown. See the application notes.

Figure 34. Typical 480i/576i Y'P'$_B$P'$_R$ AC-Input System Driving 2 AC-Coupled Video Lines

LOW PASS FILTER

Each channel of the THS7314 incorporates a 5th-Order Low Pass Filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems due to aliasing of the ADC. Another benefit of the filter is to smooth out aberrations in the signal which some DACs can have if their own internal filtering is not good. This helps with picture quality and helps insure the signal meets video bandwidth requirements.

Each filter has a Butterworth characteristic associated with it. The benefit of the Butterworth response is the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications due to their very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these elliptic or chebyshev filters may help meet the video standard specifications with respect to amplitude attenuation, their group delay is well beyond the standard specifications. Couple this with the fact that video can go from a white pixel to a black pixel over and over again, ringing can easily occur. Ringing typically causes a display to have *ghosting* or *fuzziness* appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7314 filter has a slightly lower group delay variation near the corner frequency compared to an ideal Butterworth filter. This results in a time domain pulse response which still has some overshoot, but not as much as a true Butterworth filter. Additionally, the initial rate of attenuation in the frequency response is not quite as fast as an ideal Butterworth response, but it is an acceptable initial rate of attenuation considering the pulse and group delay characteristic benefits. The THS7314 still achieves 47-dB of attenuation at 27-MHz, which typically exceeds most SD video requirements.

The THS7314 filters have a nominal corner (-3dB) frequency at 8.5-MHz and a –1 dB passband typically at 7-MHz. This 8.5-MHz filter is ideal for Standard Definition (SD) NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i/576i $Y'P'_BP'_R$, Y'U'V', broadcast G'B'R' (R'G'B') signals, and computer video signals. The 8.5-MHz -3dB corner frequency was designed to allow a maximally flat video signal while achieving 47-dB of attenuation at 27-MHz – a common sampling frequency between the DAC/ADC 2nd and 3rd Nyquist zones found in many video systems. This is important because any signal appearing around this frequency can appear in the baseband due to aliasing effects of an analog to digital converter found in a receiver.

Keep in mind that images do not stop at 27-MHz, they continue around the sampling frequencies of 54-MHz, 81-MHz, 108-MHz, etc. Because of these multiple images that an ADC can fold down into the baseband signal, the low pass filter must also eliminate these higher order images. The THS7314 has over 70-dB attenuation at 54-MHz, 68-dB attenuation at 81-MHz, and over 60-dB attenuation at 108-MHz. Attenuation above 108-MHz is at least 55-dB which makes sure that images do not effect the desired video baseband signal.

The 8.5-MHz filter frequency was chosen to account for process variations in the THS7314. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is the attenuation must be large enough to ensure the anti-aliasing / reconstruction filtering is enough to meet the system demands. Thus, the selection of the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7314, over a passive system is PCB area and filter variations. The small SOIC-8 package for 3-video channels is much smaller over a passive RLC network, especially a 5-pole passive network. Add in the fact that inductors have at best ±10% tolerances (normally ±15% to ±20% is common) and capacitors typically have ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay will have wide variations. This can lead to potential performance and quality issues in mass-production environments. The THS7314 solves most of these problems with only the corner frequency being essentially the only variable.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7314 uses low temperature coefficient resistors and high quality – low temperature coefficient capacitors found in the BiCom-3 process. The filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This maintains a low channel-to-channel time delay which is required for proper video signal performance.

Another benefit of a THS7314 over a passive RLC filter are the input and output impedances. The input impedance presented to the DAC will vary significantly with a passive network and may cause voltage variations over frequency. The THS7314 input impedance is 800-kΩ and only the 2-pF input capacitance plus the PCB trace capacitance impacting the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with the THS7314.

On the output side of the filter, a passive filter will again have a impedance variation over frequency. The THS7314 is an op-amp which approxiamates an ideal voltage source. A voltage source is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss, this output impedance must maintain a 75-Ω impedance. A passive filter impedance variation cannot guarantee this while the THS7314 has about 0.6-Ω of output impedance at 5.1-MHz. Thus, the system is matched much better with a THS7314 compared to a passive filter.

One last benefit of the THS7314 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load - the reciever 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This forces the DAC to drive at least 1.25Vpeak (100% Saturation CVBS) / 37.5Ω = 33.3mA. A DAC is a current steering element and this amount of current flows internally to the DAC even if the output is 0-V. Thus, power dissipation in the DAC may be very high - especially when 6-channels are being driven. Using the THS7314, with a high input impedance and the capability to drive up to 2-video lines, can reduce the DAC power dissipation significantly. This is because the resistance the DAC is driving can be substantially increased. It is common to set this in a DAC by a current setting resistor on the DAC. Thus, the resistance can be 300-Ω or more - substantially reducing the current drive demands from the DAC and saving substantial amount of power. For example, a 3.3-V 6-Channel DAC dissipates 660mW just for the steering current capability (6ch X 33.3mA X 3.3V) if it needs to drive 37.5-Ω load. With a 300-Ω load, the DAC power dissipation due to current steering current would only be 82.5mW (6ch X 4.16mA X 3.3V).

EVALUATION MODULE

To evaluate the THS7314, an evaluation module (EVM) is available. This allows for testing of the THS7314 in many different systems. Inputs and outputs include RCA connectors for consumer grade interconnections, or BNC connectors for higher level lab grade connections. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user.

Figure 35 shows the schematic of the THS7314EVM. Figure 36 and Figure 37 shows the top layer and bottom layer of the EVM which incorporates standard high-speed layout practices. The Bill of materials can located at: SLOR103

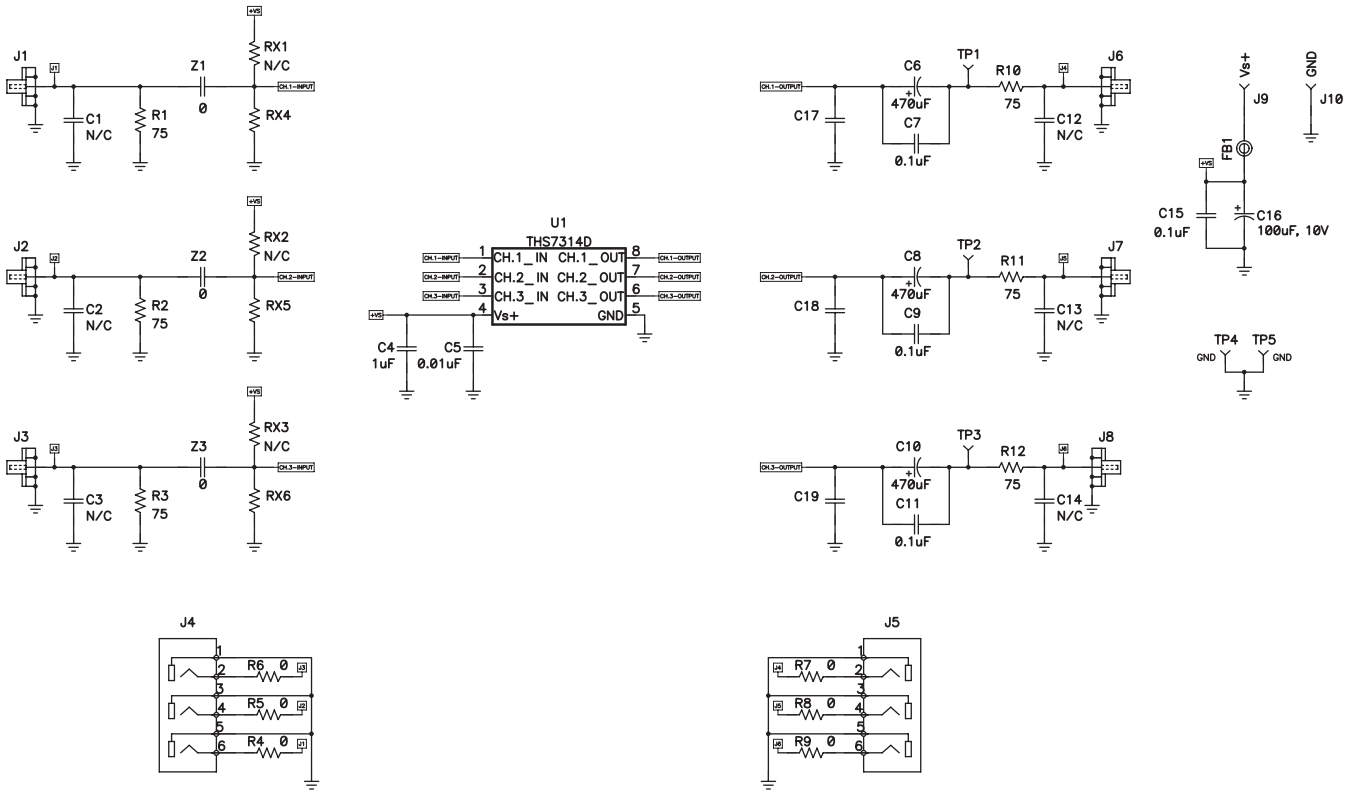


Figure 35. THS7314 Schematic

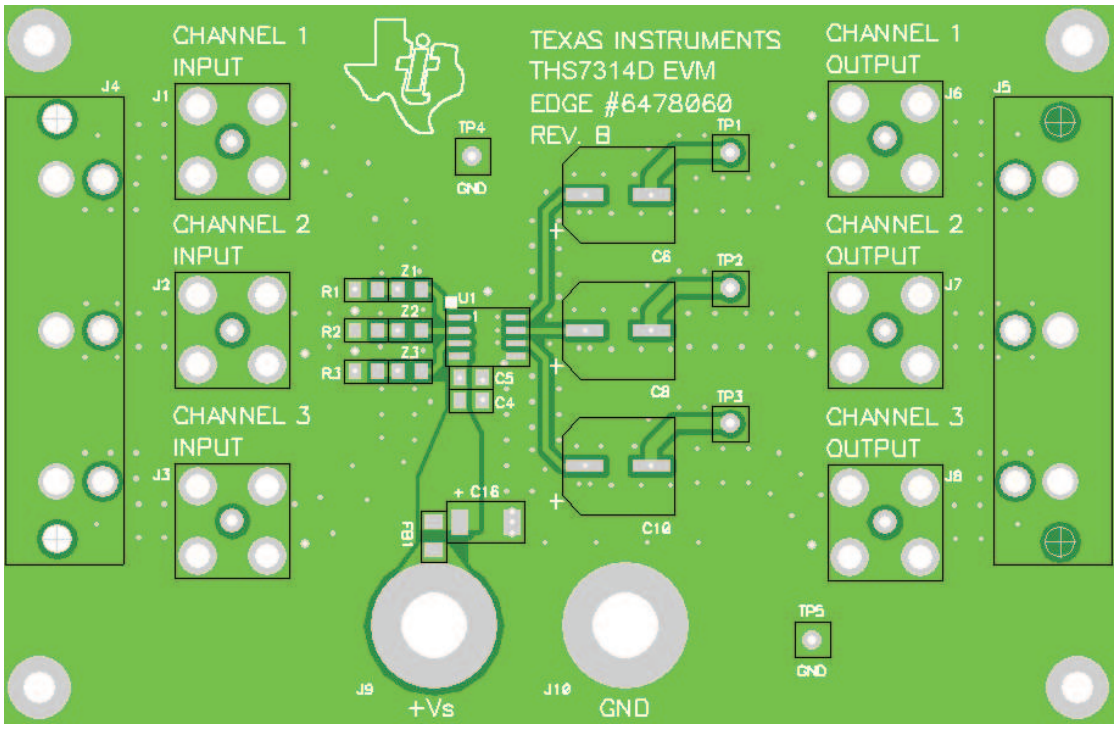


Figure 36. Top View

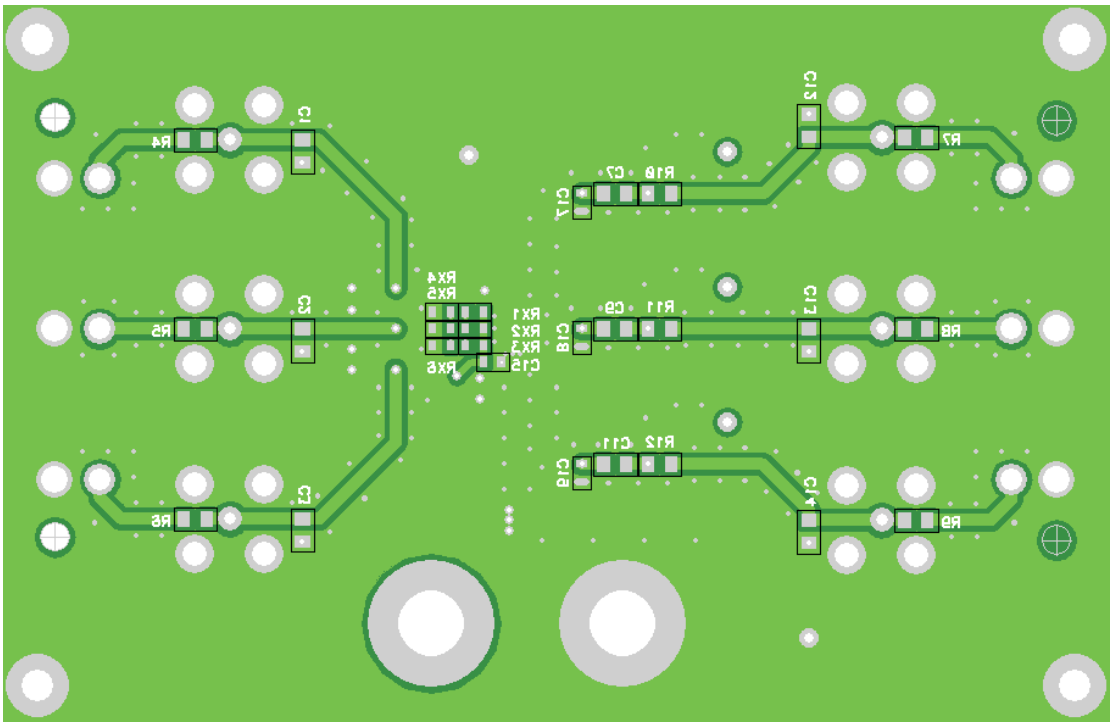


Figure 37. Bottom View

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to 2.3V and the output voltage range of 0V to 5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

REVISION HISTORY

Changes from Original (December 2006) to Revision A	Page
• Added the EVALUATION MODULE section	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00190DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7314	Samples
THS7314D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7314	Samples
THS7314DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7314	Samples
THS7314DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7314	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

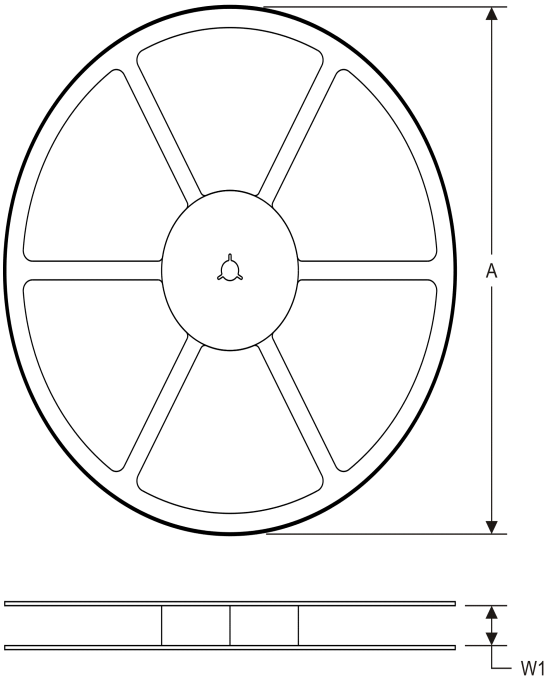
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

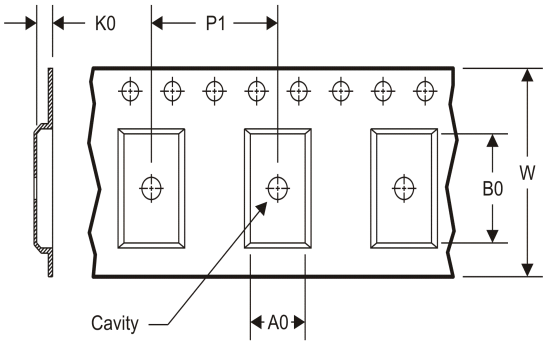
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



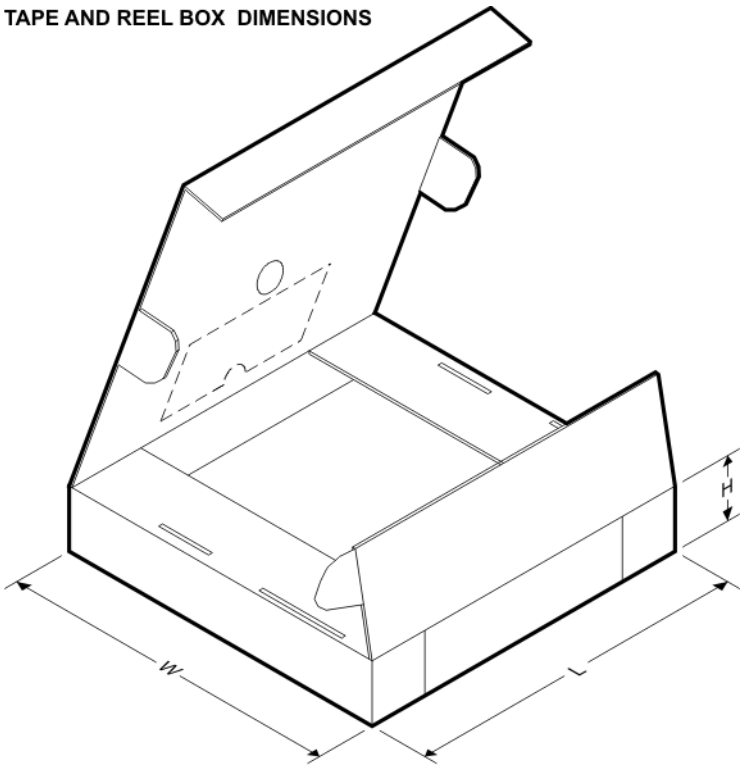
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7314DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

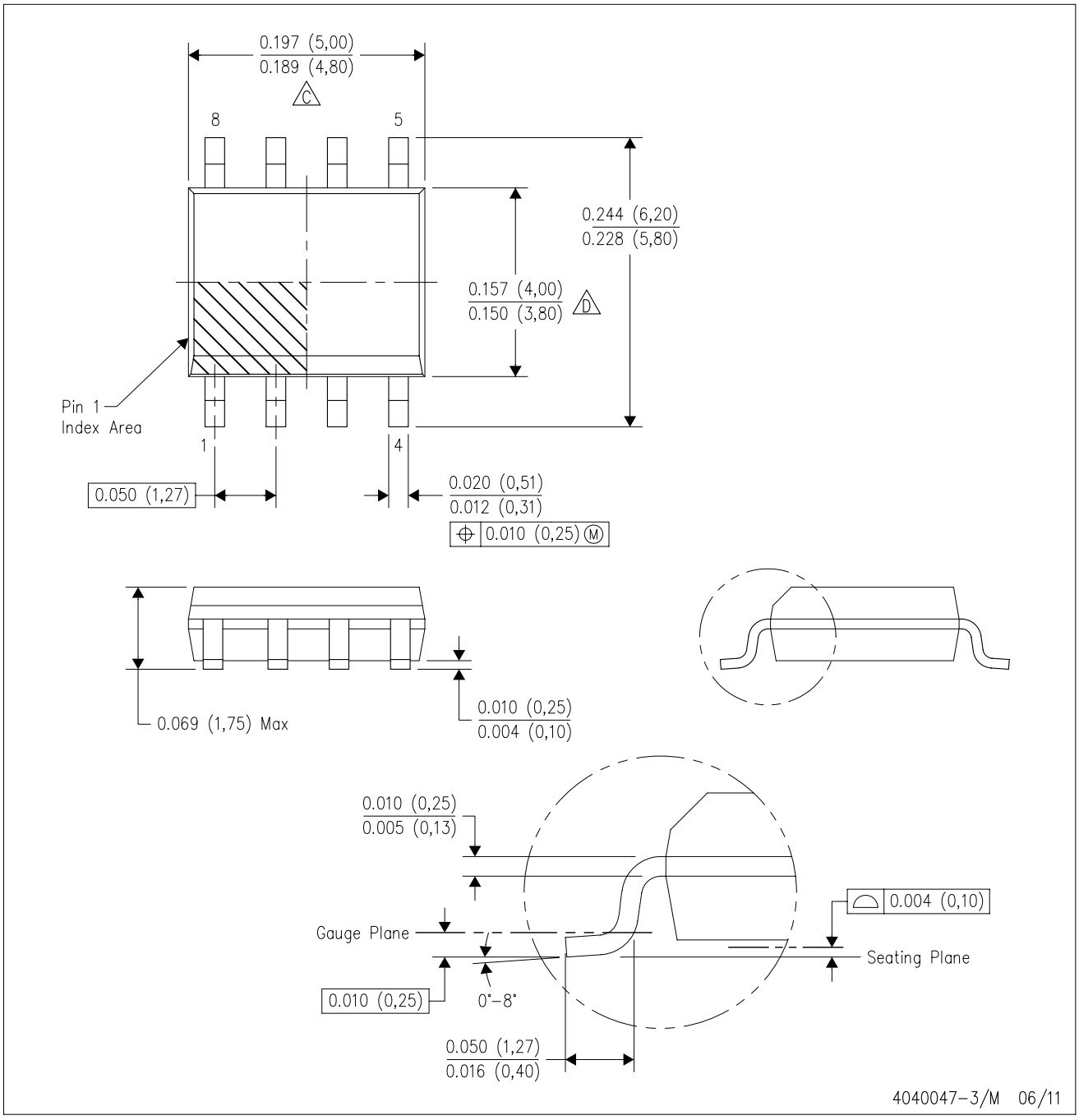
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

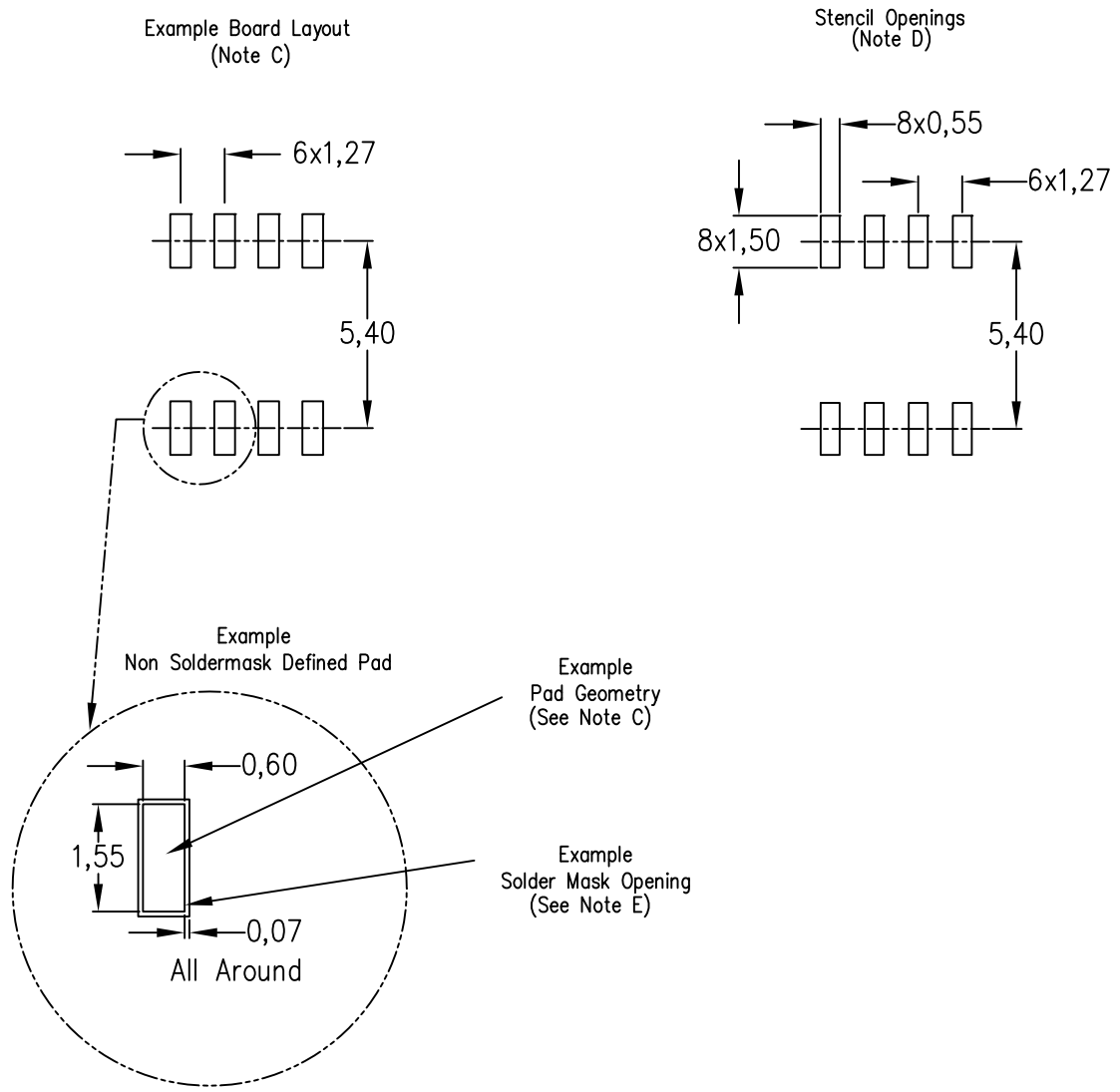
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7314DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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