SONY

Diagonal 7.20 mm (Type 1/2.5) CMOS Image Sensor with Square Pixel for Color Cameras

TENTATIVE

IMX317CQC-C

For the latest data sheet, please visit www.sunnywale.com

Description

The IMX317CQC-C is a diagonal 7.20 mm (Type 1/2.5) CMOS image sensor with a color square pixel array and approximately 8.51 M effective pixels. 12-bit digital output makes it possible to output the signals of approximately 8.51 M effective pixels with high definition for shooting still pictures.
It also operates with three power supply voltages: analog 2.8 V, digital 1.2 V, and 1.8 V for I/O interface and achieves low power consumption.
Furthermore, it realizes 12-bit digital output for shooting high-speed and high-definition moving pictures by horizontal and vertical addition and subsampling. Realizing high-sensitivity, low dark current, this sensor also has an electronic shutter function with variable storage time.
In addition, this product is designed for use in consumer use digital still camera and consumer use camcorder. When using this for another application, Sony does not guarantee the quality and reliability of the product.
Therefore, don't use this for applications other than consumer use digital still camera and consumer use camcorder.
In addition, individual specification change cannot be supported because this is a standard product.
Consult your Sony sales representative if you have any questions.

Features

- ◆CMOS active pixel type pixels
- ◆Input clock frequency 6 to 27 MHz (CSI-2), 12/24/36/72 MHz (Sub-LVDS)
- ◆Both MIPI Specifications (CSI-2 high-speed serial interface) and Sub-LVDS supported
- ◆All-pixel scan mode 12-bit, 10-bit
  Horizontal/vertical 2/2-line binning mode 12-bit, 10-bit
  Vertical 2/3 subsampling binning horizontal 3 binning mode
  Vertical 2/8 subsampling horizontal 3 binning mode
- ◆High-sensitivity, low dark current, no smear, excellent anti-blooming characteristics
- ◆Vertical and horizontal arbitrary cropping function
- ◆Variable-speed shutter function (minimum unit: 1 horizontal period)
- ◆Low power consumption
- ◆High dynamic range (HDR) function: Digital overlap HDR
- ◆H driver, V driver and serial communication circuit on chip
- ◆CDS/PGA on chip: Gain +27 dB (step pitch 0.1 dB)
- ◆10-bit/12-bit A/D conversion on chip
- ◆R, G, B primary color mosaic filters on chip
- ◆All-pixel simultaneous reset supported
- ◆96-pin high-precision ceramic package

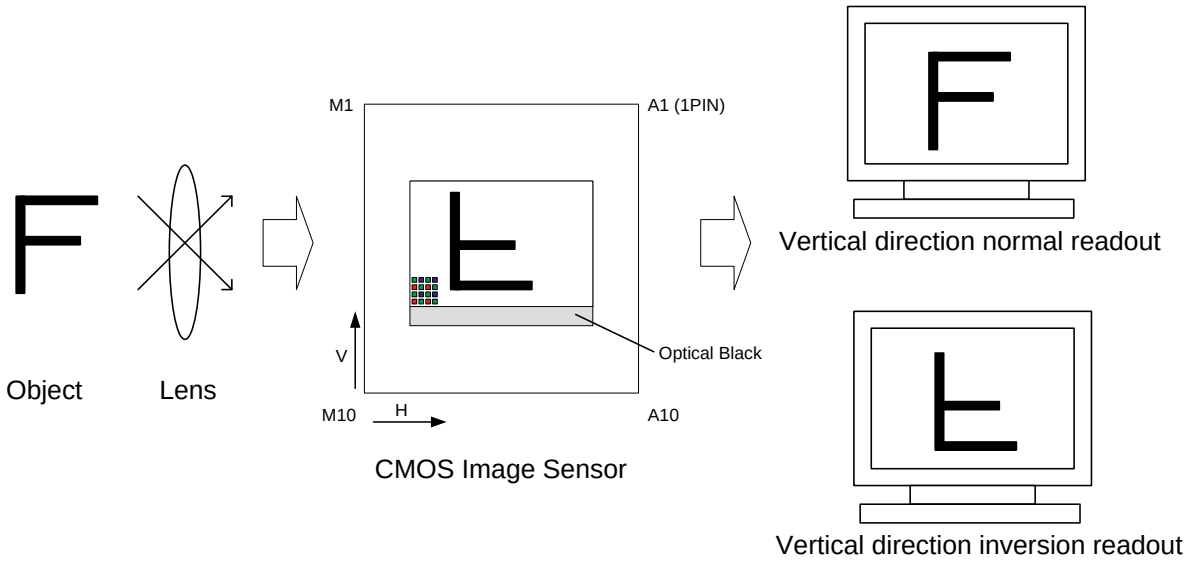
Exmor R

Device Structure

- ◆CMOS image sensor
- ◆Image size
  Diagonal 7.20 mm (Type 1/2.5)
- ◆Total number of pixels
  3864 (H) × 2218 (V) approx. 8.57 M pixels
- ◆Number of effective pixels
  3864 (H) × 2202 (V) approx. 8.51 M pixels
- ◆Number of active pixels
  3864 (H) × 2196 (V) approx. 8.49 M pixels diagonal 7.20 mm
- ◆Number of recommended recording pixels
  3840 (H) × 2160 (V) 8.29 M pixels aspect ratio 16:9
- ◆Chip size
  8.365 mm (H) × 6.615 mm (V) (include scribe area)
- ◆Unit cell size
  1.62 µm (H) × 1.62 µm (V)
- ◆Optical black
  Horizontal (H) direction : Front 0 pixel, rear 0 pixel
  Vertical (V) direction : Front 16 pixels, rear 0 pixel
- ◆Substrate material
  Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during normal readout in the vertical direction.

Optical Black Array and Readout Scan Direction

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage (Analog)	V_{ADD} *1	–0.3 to +3.3	V
Supply voltage (Digital 1)	V_{DDD1} *2	–0.5 to +2.0	V
Supply voltage (Digital 2)	V_{DDD2} *3	–0.5 to +3.3	V
Supply voltage (Digital 3)	V_{DDD3} *4	–0.5 to +2.0	V
Input voltage (Digital)	V_I	–0.3 to V_{DDD2} + 0.3	V
Output voltage (Digital)	V_O	–0.3 to V_{DDD2} + 0.3	V
Guaranteed operating temperature	T_{OPR}	–10 to +75	˚C
Storage guarantee temperature	T_{STG}	–30 to +80	˚C
Performance guarantee temperature	T_{SPEC}	–10 to +60	˚C

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Supply voltage (Analog)	V_{ADD} *1	2.8 ± 0.1	V
Supply voltage (Digital 1)	V_{DDD1} *2	1.2 ± 0.1	V
Supply voltage (Digital 2)	V_{DDD2} *3	1.8 ± 0.1	V
Supply voltage (Digital 3)	V_{DDD3} *4	1.2 ± 0.1	V
Input voltage (Digital)	V_I	–0.1 to V_{DDD2} + 0.1	V

*1 V_{ADD}: V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP (2.8 V power supply)
*2 V_{DDD1}: V_{DD}LCN, V_{DD}LSC1 to 2, V_{DD}LPA, V_{DD}LPL1 (1.2 V power supply)
*3 V_{DDD2}: V_{DD}MIO, V_{DD}MIF (1.8 V power supply)
*4 V_{DDD3}: V_{DD}LPL2 to 3, V_{DD}LIF (1.2 V power supply)

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

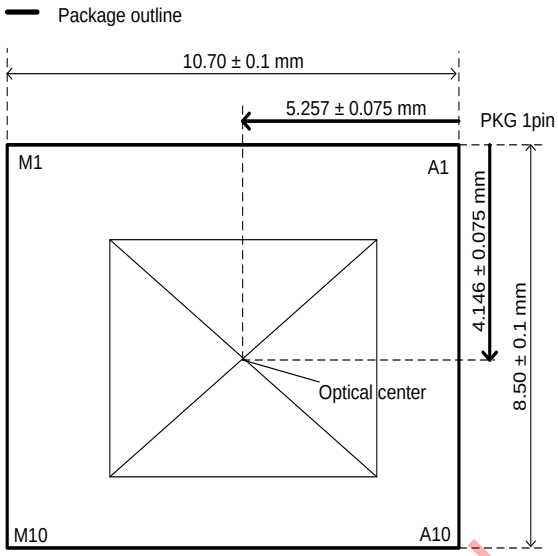
Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

Contents

Optical Center

(Top View)

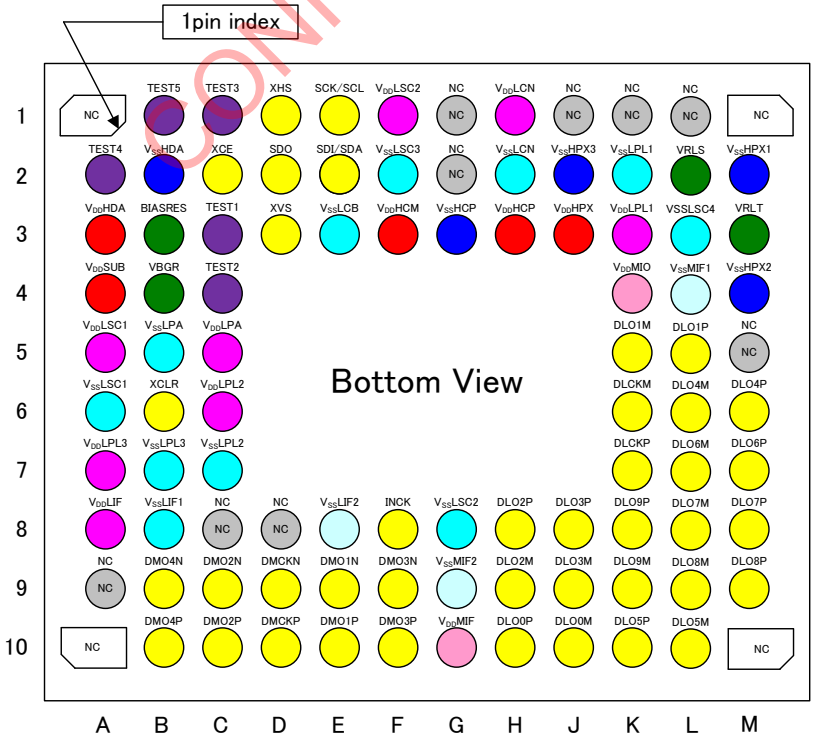


* See page TBD “Package Outline” for details

Optical Center

Pin Configuration

(Bottom View)



Pin Configuration

Pin Description

When using CSI-2

Pin No.	Symbol	I/O	A/D	Pin description (CSI-2)	State in Standby mode	Remarks
A2	TEST4	O	A	Test		Leave open. (No connection)
A3	V_{DD}HDA	Power	A	Analog power supply (2.8 V)	—	
A4	V_{DD}SUB	Power	A	Analog power supply (2.8 V)	—	
A5	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
A6	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
A7	V_{DD}LPL3	Power	D	Digital power supply (1.2 V)	—	
A8	V_{DD}LIF	Power	D	Digital power supply (1.2 V)	—	
B1	TEST5	O	A	Test		Leave open. (No connection)
B2	V_{SS}HDA	GND	A	Analog GND (2.8 V)	—	
B3	BIASRES	O	A	Resister connection		
B4	VBGR	O	A	Capacitor connection		
B5	V_{SS}LPA	GND	D	Digital GND (1.2 V)	—	
B6	XCLR	I	D	Reset pulse input	—	
B7	V_{SS}LPL3	GND	D	Digital GND (1.2 V)	—	
B8	V_{SS}LIF1	GND	D	Digital GND (1.2 V)	—	
B9	DMO4N	O	D	Digital MIPI output	Low Level	Data Lane 4 connection
B10	DMO4P	O	D	Digital MIPI output	Low Level	Data Lane 4 connection
C1	TEST3	O	D	Test		Leave open. (No connection)
C2	XCE	I	D	Connect to 1.8 V power supply	—	
C3	TEST1	I	D	Test		Leave open. (No connection)
C4	TEST2	I	D	Test		Leave open. (No connection)
C5	V_{DD}LPA	Power	D	Digital power supply (1.2 V)	—	
C6	V_{DD}LPL2	Power	D	Digital power supply (1.2 V)	—	
C7	V_{SS}LPL2	GND	D	Digital GND (1.2 V)	—	
C9	DMO2N	O	D	Digital MIPI output	Low Level	Data Lane 2 connection
C10	DMO2P	O	D	Digital MIPI output	Low Level	Data Lane 2 connection
D1	XHS	O	D	Horizontal sync signal output	—	If unused XHS, leave open.
D2	SDO	O	D	Test output	Low Level	Leave open. (No connection)
D3	XVS	O	D	Vertical sync signal output	—	If unused XVS, leave open.
D9	DMCKN	O	D	Digital MIPI output	Low Level	Clock Lane connection.
D10	DMCKP	O	D	Digital MIPI output	Low Level	Clock Lane connection.
E1	SCL	I	D	I^2C communication clock input	—	
E2	SDA	I/O	D	I^2C communication data input/output	—	

Pin No.	Symbol	I/O	A/D	Pin description (CSI-2)	State in Standby mode	Remarks
E3	V_{SS}LCB	GND	D	Digital GND (1.2 V)	—	
E8	V_{SS}LIF2	GND	D	Digital GND (1.2 V)	—	
E9	DMO1N	O	D	Digital MIPI output	Low Level	Data Lane 1 connection
E10	DMO1P	O	D	Digital MIPI output	Low Level	Data Lane 1 connection
F1	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
F2	V_{SS}LSC3	Power	D	Digital power supply (1.2 V)	—	
F3	V_{DD}HCM	Power	A	Analog power supply (2.8 V)	—	
F8	INCK	I	D	Input clock	—	
F9	DMO3N	O	D	Digital MIPI output	Low Level	Data Lane 3 connection
F10	DMO3P	O	D	Digital MIPI output	Low Level	Data Lane 3 connection
G3	V_{SS}HCP	GND	A	Analog GND (2.8 V)	—	
G8	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
G9	V_{SS}MIF2	GND	D	Digital GND (1.8 V)	—	
G10	V_{DD}MIF	Power	D	Digital power supply (1.8 V)	—	
H1	V_{DD}LCN	GND	D	Digital GND (1.2 V)	—	
H2	V_{SS}LCN	GND	D	Digital GND (1.2 V)	—	
H3	V_{DD}HCP	Power	A	Analog power supply (2.8 V)	—	
H8	DLO2P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
H9	DLO2M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
H10	DLO0P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
J2	V_{SS}HPX3	GND	A	Analog GND (2.8 V)	—	
J3	V_{DD}HPX	Power	A	Analog power supply (2.8 V)	—	
J8	DLO3P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
J9	DLO3M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
J10	DLO0M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K2	V_{SS}LPL1	GND	D	Digital GND (1.2 V)	—	
K3	V_{DD}LPL1	Power	D	Digital power supply (1.2 V)	—	
K4	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
K5	DLO1M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K6	DLCKM	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K7	DLCKP	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K8	DLO9P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K9	DLO9M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
K10	DLO5P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)

Pin No.	Symbol	I/O	A/D	Pin description (CSI-2)	State in Standby mode	Remarks
L2	VRLS	O	A	Capacitor connection	Pull-down	
L3	V_{SS}LSC4	GND	D	Digital GND (1.2 V)	—	
L4	V_{SS}MIF1	GND	D	Digital GND (1.8 V)	—	
L5	DLO1P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
L6	DLO4M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
L7	DLO6M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
L8	DLO7M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
L9	DLO8M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
L10	DLO5M	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
M2	V_{SS}HPX1	GND	A	Analog GND (2.8 V)	—	
M3	VRLT	O	A	Capacitor connection	Pull-down	
M4	V_{SS}HPX2	GND	A	Analog GND (2.8 V)	—	
M6	DLO4P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
M7	DLO6P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
M8	DLO7P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)
M9	DLO8P	O	D	(Pin for Sub-LVDS)		Leave open. (No connection)

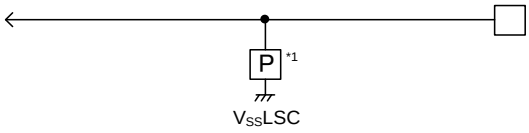
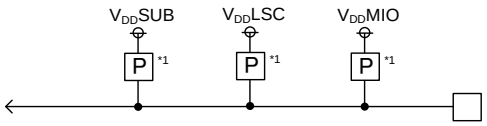
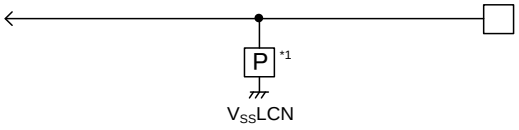
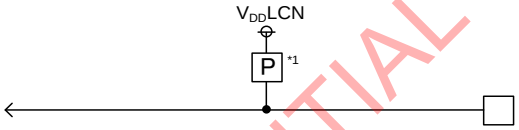
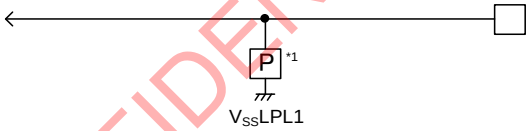
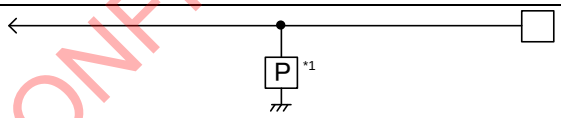
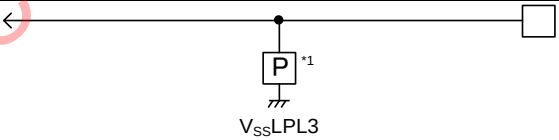
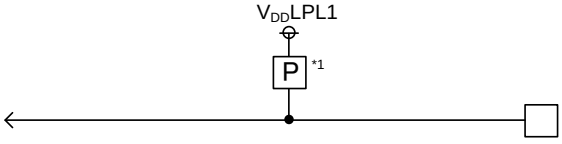
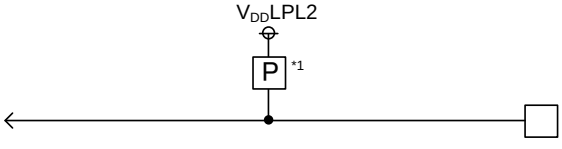
When using Sub-LVDS

Pin No.	Symbol	I/O	A/D	Pin description (Sub-LVDS)	State in Standby mode	Remarks
A2	TEST4	O	A	Test		Leave open. (No connection)
A3	V_{DD}HDA	Power	A	Analog power supply (2.8 V)	—	
A4	V_{DD}SUB	Power	A	Analog power supply (2.8 V)	—	
A5	V_{DD}LSC1	Power	D	Digital power supply (1.2 V)	—	
A6	V_{SS}LSC1	GND	D	Digital GND (1.2 V)	—	
A7	V_{DD}LPL3	Power	D	Digital power supply (1.2 V)	—	
A8	V_{DD}LIF	Power	D	Digital power supply (1.2 V)	—	
B1	TEST5	O	A	Test		Leave open. (No connection)
B2	V_{SS}HDA	GND	A	Analog GND (2.8 V)	—	
B3	BIASRES	O	A	Resister connection		
B4	VBGR	O	A	Capacitor connection		
B5	V_{SS}LPA	GND	D	Digital GND (1.2 V)	—	
B6	XCLR	I	D	Reset pulse input	—	
B7	V_{SS}LPL3	GND	D	Digital GND (1.2 V)	—	
B8	V_{SS}LIF1	GND	D	Digital GND (1.2 V)	—	
B9	DMO4N	O	D	(Pin for CSI-2)		Leave open. (No connection)
B10	DMO4P	O	D	(Pin for CSI-2)		Leave open. (No connection)
C1	TEST3	O	D	Test		Leave open. (No connection)
C2	XCE	I	D	Serial communication enable input	—	
C3	TEST1	I	D	Test		Leave open. (No connection)
C4	TEST2	I	D	Test		Leave open. (No connection)
C5	V_{DD}LPA	Power	D	Digital power supply (1.2 V)	—	
C6	V_{DD}LPL2	Power	D	Digital power supply (1.2 V)	—	
C7	V_{SS}LPL2	GND	D	Digital GND (1.2 V)	—	
C9	DMO2N	O	D	(Pin for CSI-2)		Leave open. (No connection)
C10	DMO2P	O	D	(Pin for CSI-2)		Leave open. (No connection)
D1	XHS	I	D	Horizontal sync signal input	—	
D2	SDO	O	D	Test output	Low Level	Leave open. (No connection)
D3	XVS	I	D	Vertical sync signal input	—	
D9	DMCKN	O	D	(Pin for CSI-2)		Leave open. (No connection)
D10	DMCKP	O	D	(Pin for CSI-2)		Leave open. (No connection)
E1	SCK	I	D	Serial communication clock input	—	
E2	SDI	I	D	Serial communication data input	—	
E3	V_{SS}LCB	GND	D	Digital GND (1.2 V)	—	
E8	V_{SS}LIF2	GND	D	Digital GND (1.2 V)	—	

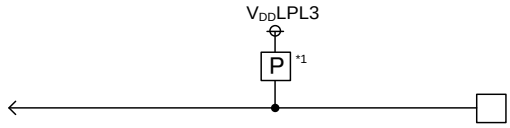
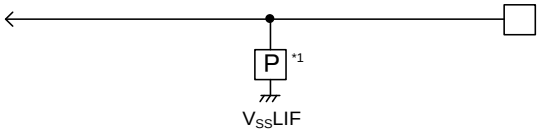
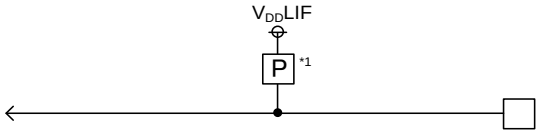
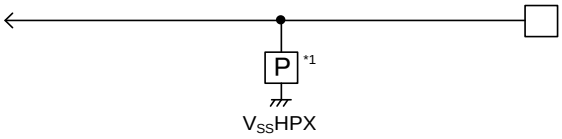
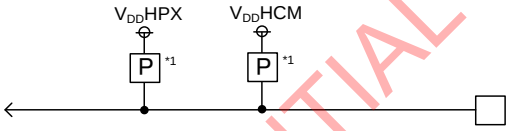
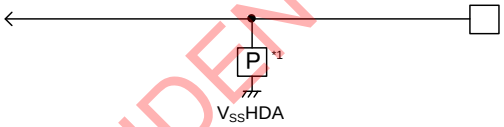
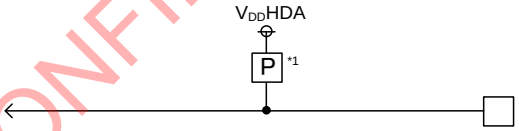
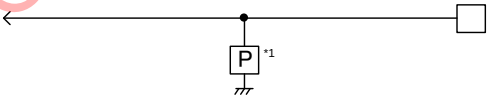
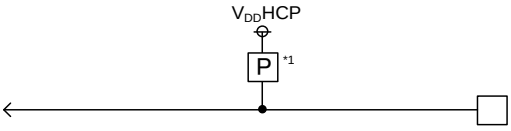
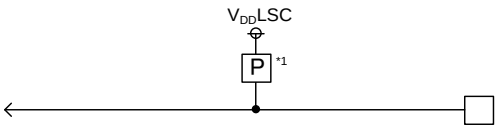
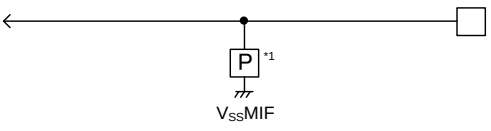
Pin No.	Symbol	I/O	A/D	Pin description (Sub-LVDS)	State in Standby mode	Remarks
E9	DMO1N	O	D	(Pin for CSI-2)		Leave open. (No connection)
E10	DMO1P	O	D	(Pin for CSI-2)		Leave open. (No connection)
F1	V_{DD}LSC2	Power	D	Digital power supply (1.2 V)	—	
F2	V_{SS}LSC3	Power	D	Digital power supply (1.2 V)	—	
F3	V_{DD}HCM	Power	A	Analog power supply (2.8 V)	—	
F8	INCK	I	D	Input clock	—	
F9	DMO3N	O	D	(Pin for CSI-2)		Leave open. (No connection)
F10	DMO3P	O	D	(Pin for CSI-2)		Leave open. (No connection)
G3	V_{SS}HCP	GND	A	Analog GND (2.8 V)	—	
G8	V_{SS}LSC2	GND	D	Digital GND (1.2 V)	—	
G9	V_{SS}MIF2	GND	D	Digital GND (1.8 V)	—	
G10	V_{DD}MIF	Power	D	Digital power supply (1.8 V)	—	
H1	V_{DD}LCN	GND	D	Digital GND (1.2 V)	—	
H2	V_{SS}LCN	GND	D	Digital GND (1.2 V)	—	
H3	V_{DD}HCP	Power	A	Analog power supply (2.8 V)	—	
H8	DLO2P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
H9	DLO2M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
H10	DLO0P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
J2	V_{SS}HPX3	GND	A	Analog GND (2.8 V)	—	
J3	V_{DD}HPX	Power	A	Analog power supply (2.8 V)	—	
J8	DLO3P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
J9	DLO3M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
J10	DLO0M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K2	V_{SS}LPL1	GND	D	Digital GND (1.2 V)	—	
K3	V_{DD}LPL1	Power	D	Digital power supply (1.2 V)	—	
K4	V_{DD}MIO	Power	D	Digital power supply (1.8 V)	—	
K5	DLO1M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K6	DLCKM	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K7	DLCKP	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K8	DLO9P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K9	DLO9M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
K10	DLO5P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L2	VRLS	O	A	Capacitor connection	Pull-down	
L3	V_{SS}LSC4	GND	D	Digital GND (1.2 V)	—	
L4	V_{SS}MIF1	GND	D	Digital GND (1.8 V)	—	

Pin No.	Symbol	I/O	A/D	Pin description (Sub-LVDS)	State in Standby mode	Remarks
L5	DLO1P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L6	DLO4M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L7	DLO6M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L8	DLO7M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L9	DLO8M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
L10	DLO5M	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
M2	V_{SS}HPX1	GND	A	Analog GND (2.8 V)	—	
M3	VRLT	O	A	Capacitor connection	Pull-down	
M4	V_{SS}HPX2	GND	A	Analog GND (2.8 V)	—	
M6	DLO4P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
M7	DLO6P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
M8	DLO7P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output
M9	DLO8P	O	D	Digital Sub-LVDS output	Hi-Z	Digital LVDS output

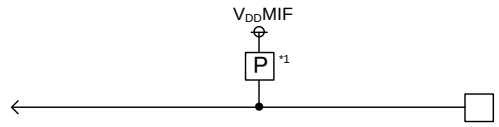
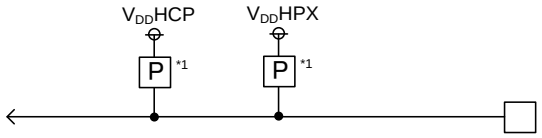
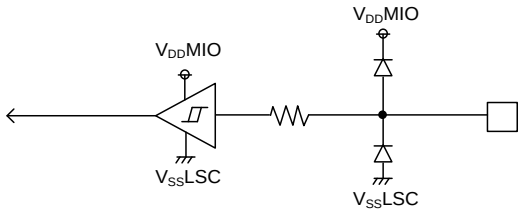
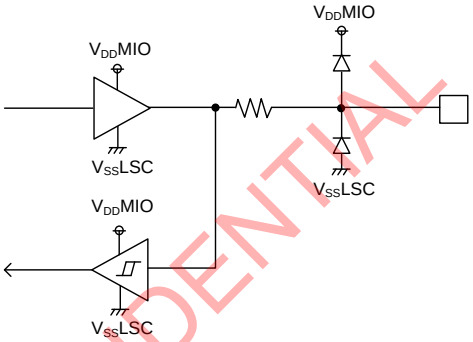
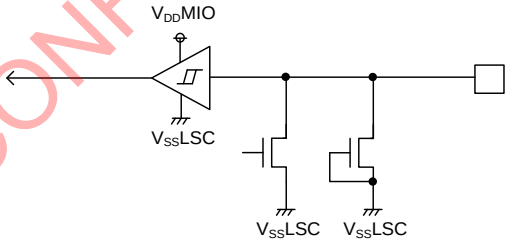
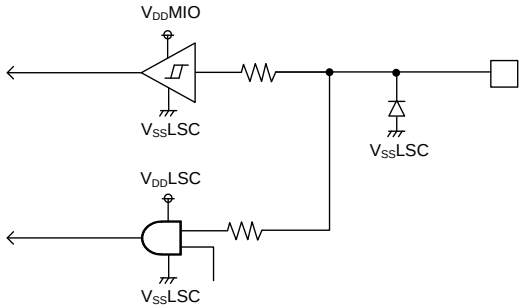
I/O Equivalent Circuit Diagram

Symbol	Equivalent circuit
V_{DD}LSC1 to 3 V_{DD}MIO V_{DD}SUB	 V_{DD}LSC1, V_{DD}LSC2 and V_{DD}LSC3 are internally connected.
V_{SS}LSC1 to 2	 V_{SS}LSC1 and V_{SS}LSC2 are internally connected.
V_{DD}LCN1 to 2	 V_{DD}LCN1 and V_{DD}LCN2 are internally connected.
V_{SS}LCN1 to 2	 V_{SS}LCN1 and V_{SS}LCN2 are internally connected.
V_{DD}LPL1	
V_{DD}LPL2	
V_{DD}LPL3	
V_{SS}LPL1	
V_{SS}LPL2	

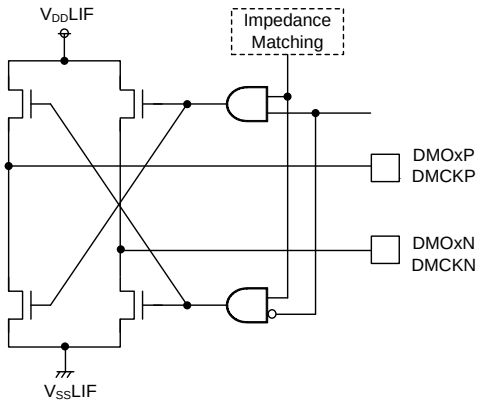
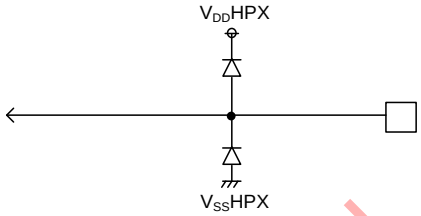
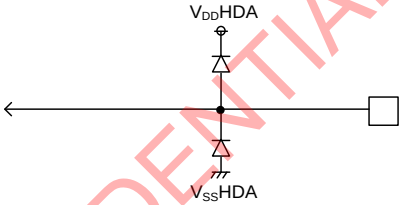
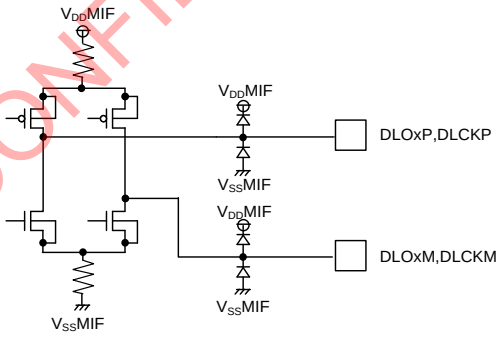
☐ External pins

Symbol	Equivalent circuit
V_{SS}LPL3	
V_{DD}LIF1 to 2	 V_{DD}LIF1 and V_{DD}LIF2 are internally connected.
V_{SS}LIF1 to 2	 V_{SS}LIF1 and V_{SS}LIF2 are internally connected.
V_{DD}HPX V_{DD}HCM	
V_{SS}HPX	
V_{DD}HDA	
V_{SS}HDA	
V_{DD}HCP	
V_{SS}HCP	
V_{SS}LCB	
V_{DD}MIF	

□ External pins

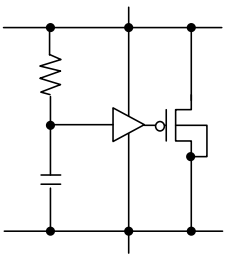
Symbol	Equivalent circuit
V_{SS}MIF1 to 2	 V_{SS}MIF1 and V_{SS}MIF 2 are internally connected.
VRLT VRLS	
INCK XCE	
XVS XHS	
SDA/SCL SCL/SDA	
XCLR	

☐ External pins

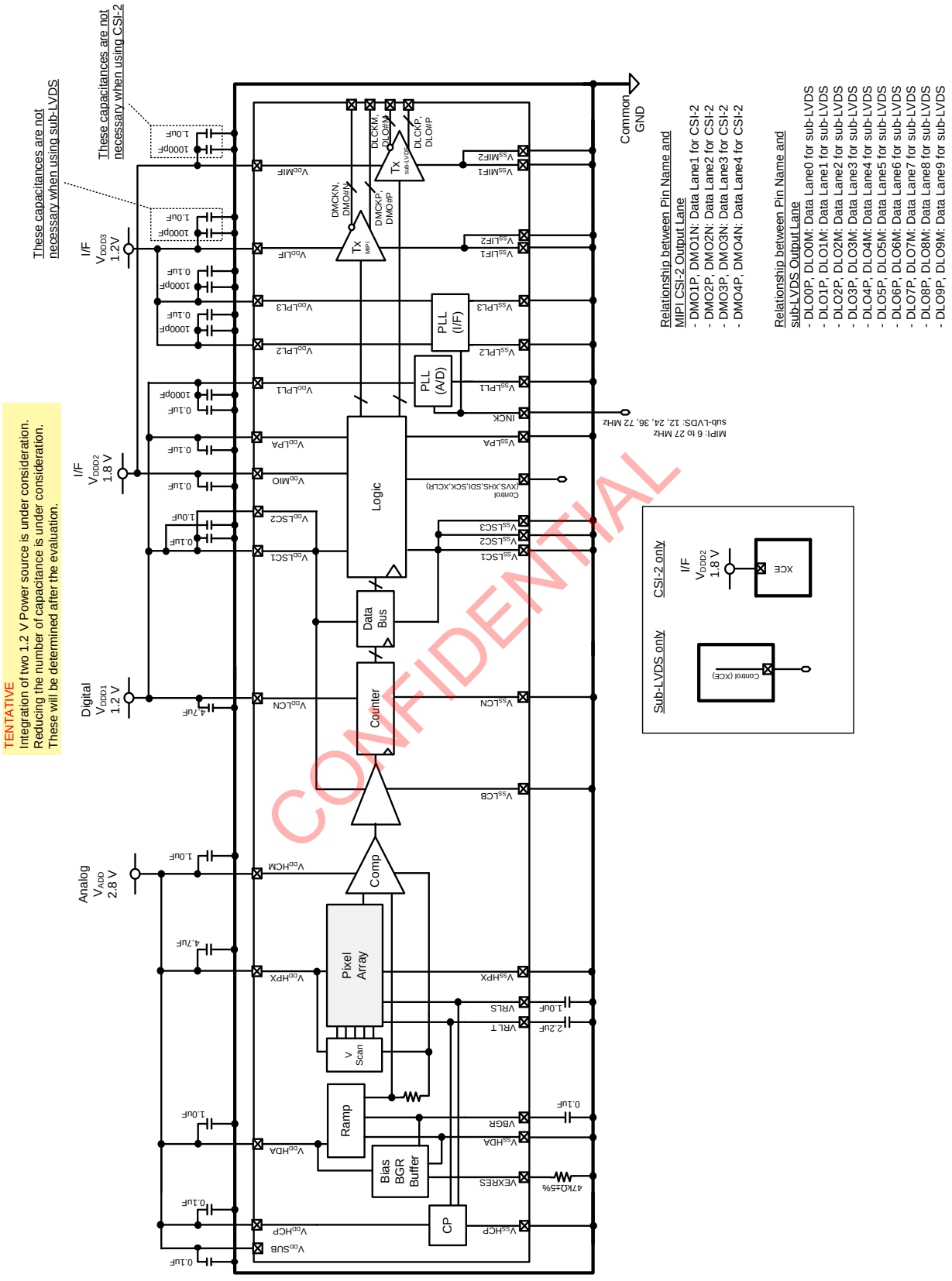
Symbol	Equivalent circuit
DMOxP DMOxN (x = 1 to 4) DMCKP DMCKN	
VEXRES	
BIASRES VBGR	
DLOxP DLOxM (x = 1 to 4) DLCKP DLCKM	

☐ External pins

Description of Special Symbol

Symbol	Equivalent circuit
P *1	

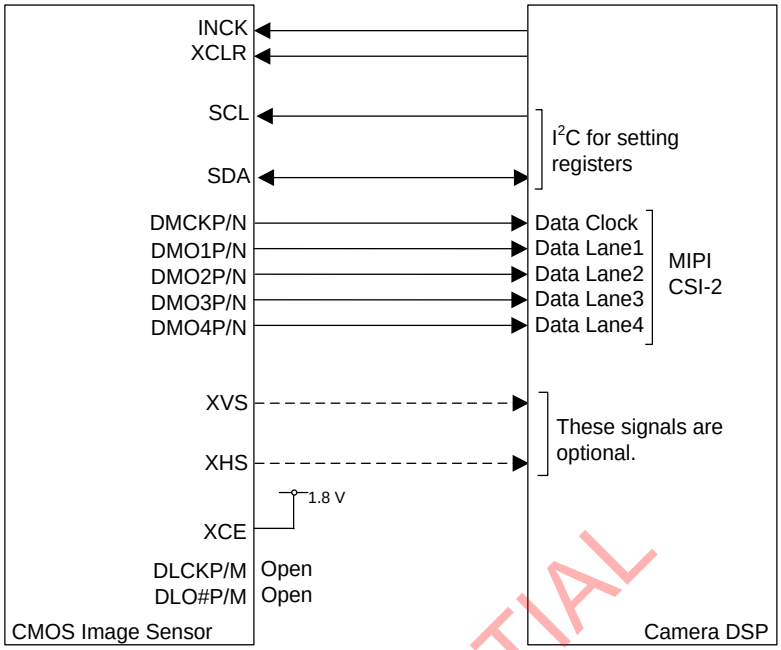
Peripheral Circuit



Peripheral Circuit

System Outline

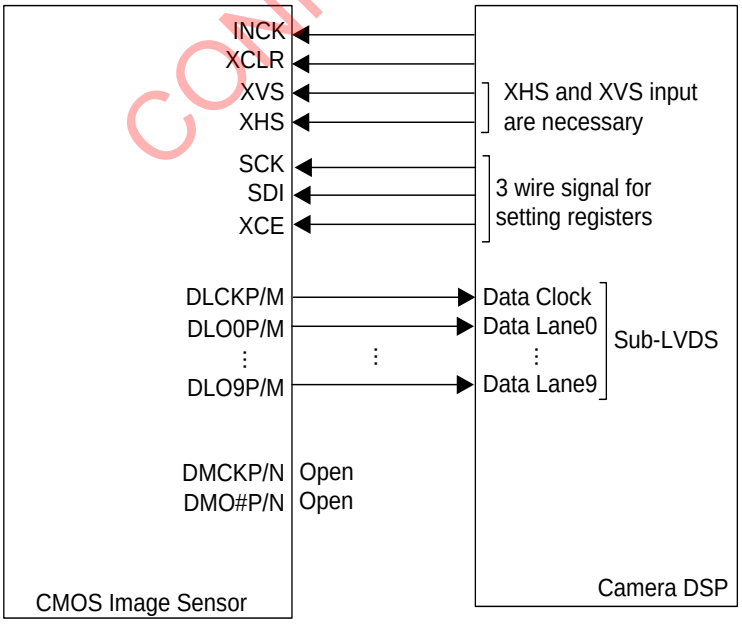
When using CSI-2



* I^2C communication only can be used when using MIPI CSI-2
* Sensor Master operation only

System Outline When Using CSI-2

When using Sub-LVDS



* 3-wire serial communication only can be used when using Sub-LVDS
* Sensor Slave operation only

System Outline When Using Sub-LVDS

Electrical Characteristics when using CSI-2

1. DC Characteristics (CSI-2)

Current Consumption and Gain Variable Range (CSI-2)

(V_{ADD} = 2.8 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, V_{DDD3} = 1.2 V, Tj = 60 ˚C, Reference Gain (0 dB)
All pixel scan mode (MODE0), 29.97 frame/s)

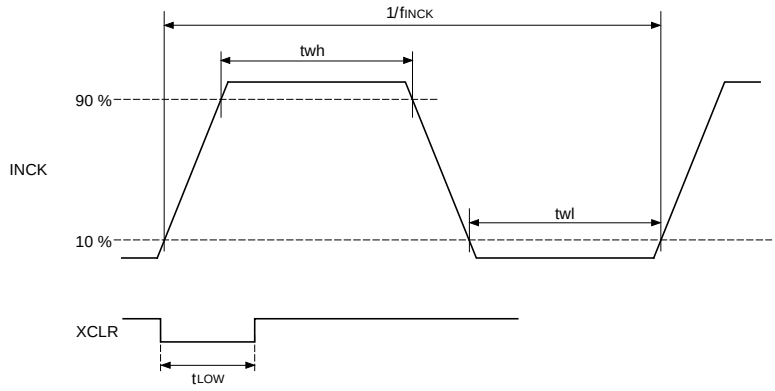
Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	TBD	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	TBD	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	TBD	mA	
Current consumption (Digital 3)	I_{DDD3}	—	—	TBD	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	TBD	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	TBD	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	TBD	μA	In the dark
Standby current (Digital 3)	$I_{DDD3STB}$	—	—	TBD	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage (CSI-2)

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP	V_{ADD}	2.70	2.80	2.90	V
	Digital 1	V_{DD}LCN, V_{DD}LSC1 to 2, V_{DD}LPL1, V_{DD}LPA	V_{DDD1}	1.10	1.20	1.30	V
	Digital 2	V_{DD}MIO, V_{DD}MIF	V_{DDD2}	1.70	1.80	1.90	V
	Digital 3	V_{DD}LPL2 to 3, V_{DD}LIF	V_{DDD3}	1.10	1.20	1.30	V
Digital input voltage		SDA, SCL	V_{IH1}	0.7 × V_{DDD2}	—	1.9	V
			V_{IL1}	–0.3	—	0.3 × V_{DDD2}	V
		XCLR, INCK	V_{IH2}	0.65 × V_{DDD2}	—	V_{DDD2} + 0.3	V
			V_{IL2}	–0.3	—	0.35 × V_{DDD2}	V
Digital output voltage		XHS, XVS	V_{HVOUT}	—	V_{DDD2}	—	V

2. AC Characteristics (CSI-2)

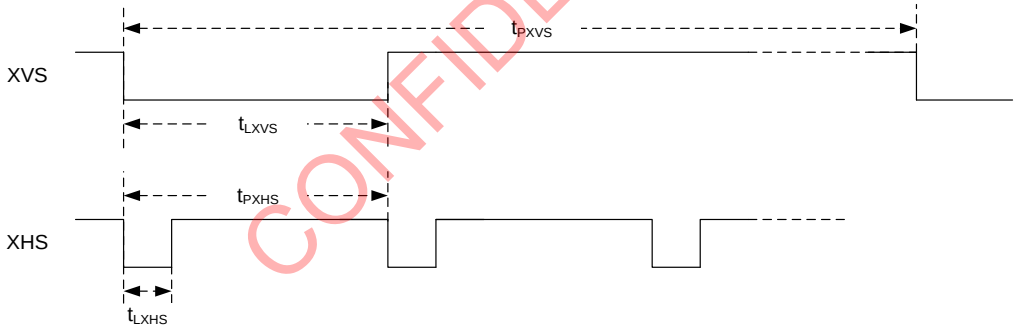
INCK, XCLR (CSI-2)



INCK, XCLR (CSI-2)

Item	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{INCK}	6	—	27	MHz
INCK Low level pulse width	twl	5	—	—	ns
INCK High level pulse width	twh	5	—	—	ns
Clock duty	—	40	50	60	%
XCLR Low level pulse width	t_{LOW}	100	—	—	ns

XHS, XVS (Output) (CSI-2)

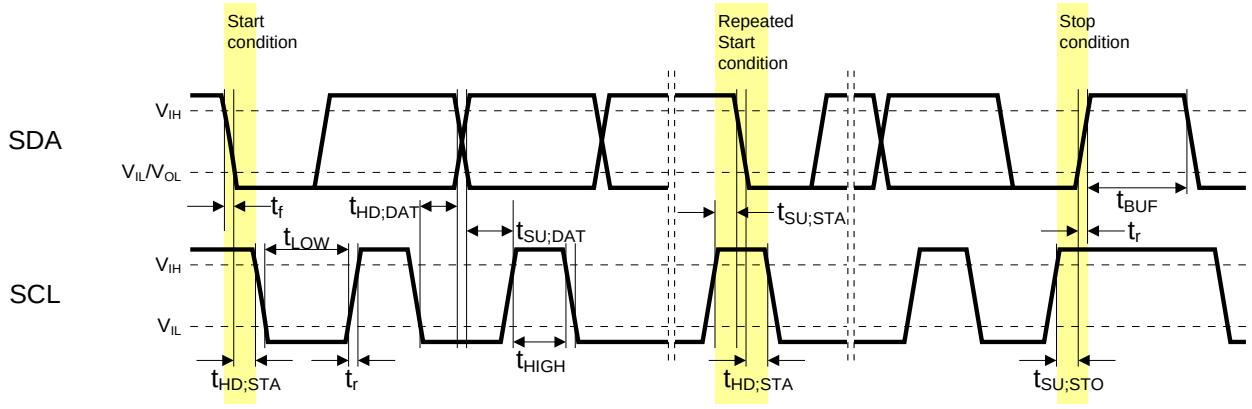


XHS, XVS Output (CSI-2)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{LXHS}		222		ns	16 clk@72MHz
XHS pulse period	t_{PXHS}		HMAX[*1]		clk@72MHz	
XVS Low level pulse width	t_{LXVS}		t_{PXHS}		clk@72MHz	
XVS pulse period	t_{PXVS}		HMAX[*1] × VMAX[*2]		clk@72MHz	

[*1] The value set as HMAX (address 30F6h, bit [7:0] and address 30F7h, bit [7:0])
[*2] The value set as VMAX (address 30F8h, bit [7:0], address 30F9h, bit [7:0] and address 30FAh, bit [3:0]).

I²C Communication (CSI-2)



I²C Communication (CSI-2)

I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	−0.3	—	0.3 × V_{DDD2}	V	
High level input voltage	V_{IH}	0.7 × V_{DDD2}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × V_{DDD2}	V	V_{DDD2} < 2 V, Sink 3 mA
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × V_{DDD2} to 0.3 × V_{DDD2}
Input current (SCL, SDA, XCLR, INCK)	Ii	-10	—	10	µA	0.1 × V_{DDD2} to 0.9 × V_{DDD2}
Input capacitance of SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

DMCKP / DMCKN, DMO (CSI-2)

Detailed explanation of CSI-2 interface is in following two documents, "MIPI Alliance Standard for Camera Serial Interface2(CSI-2) Version 1.1" and "MIPI Alliance Specification for D-PHY Version 1.1".
Four data output Lanes are applied from MIPI Alliance Standard for Camera Serial Interface2(CSI-2) Version 1.1.

Electrical Characteristics When Using Sub-LVDS

1. DC Characteristics (Sub-LVDS)

Current Consumption and Gain Variable Range (Sub-LVDS)

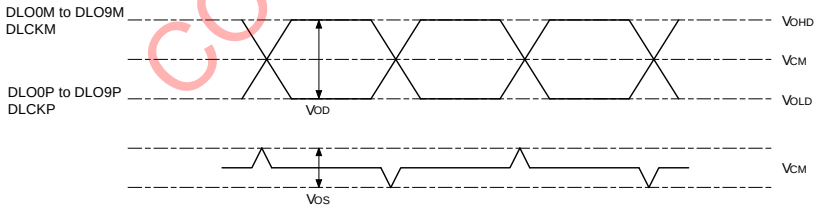
(V_{ADD} = 2.8 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, Tj = 60 ˚C, Reference Gain (0 dB)
All pixel scan mode (MODE0), 29.97 frame/s)

Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Current consumption (Analog)	I_{ADD}	—	—	TBD	mA	
Current consumption (Digital 1)	I_{DDD1}	—	—	TBD	mA	
Current consumption (Digital 2)	I_{DDD2}	—	—	TBD	mA	
Current consumption (Digital 3)	I_{DDD3}	—	—	TBD	mA	
Standby current (Analog)	I_{ADDSTB}	—	—	TBD	μA	In the dark
Standby current (Digital 1)	$I_{DDD1STB}$	—	—	TBD	mA	In the dark
Standby current (Digital 2)	$I_{DDD2STB}$	—	—	TBD	μA	In the dark
Standby current (Digital 3)	$I_{DDD3STB}$	—	—	TBD	μA	In the dark
PGA gain variable range	PGAG	0	—	27	dB	

Supply Voltage and I/O Voltage (Sub-LVDS)

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	V_{DD}SUB, V_{DD}HCM, V_{DD}HPX, V_{DD}HDA, V_{DD}HCP	V_{ADD}	2.70	2.80	2.90	V
	Digital 1	V_{DD}LCN, V_{DD}LSC1 to 2, V_{DD}LPL1, V_{DD}LPA	V_{DDD1}	1.10	1.20	1.30	V
	Digital 2	V_{DD}MIO, V_{DD}MIF	V_{DDD2}	1.70	1.80	1.90	V
	Digital 3	V_{DD}LPL2 to 3, V_{DD}LIF	V_{DDD3}	1.10	1.20	1.30	V
Digital input voltage		SCK, SDI, XCE, XHS, XVS, XCLR, INCK	V_{IH1}	0.7 × V_{DDD2}	—	1.9	V
			V_{IL1}	–0.3	—	0.3 × V_{DDD2}	V
Digital input leak cuurent		SCK, SDI, XCE, XHS, XVS, XCLR, INCK	I_{LI}	–10	—	10	uA

LVDS Output DC Characteristics (Sub-LVDS)



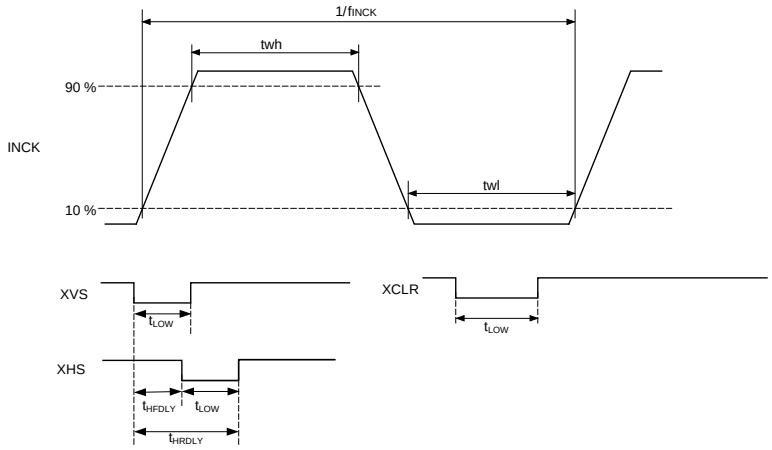
LVDS Output DC Characteristics (Sub-LVDS)

(Termination resistance: 100 Ω, LVDS current: 1.5 mA)

Item	Pins	Item	Symbol	Min.	Typ.	Max.	Unit
Digital output voltage	DLO0P to DLO9P, DLO0M to DLO9M, DLCKP, DLCKM	Amplitude voltage	V_{OD}	100	150	200	mV
		Common voltage	V_{CM}	V_{DDD2}/2 – 100	V_{DDD2}/2	V_{DDD2}/2 + 100	mV
		Common voltage fluctuation	V_{OS}	—	20	—	mV
		High level output voltage	V_{OHD}	V_{CM} + 50	V_{CM} + 75	V_{CM} + 100	mV
		Low level output voltage	V_{OLD}	V_{CM} – 100	V_{CM} – 75	V_{CM} – 50	mV
		Difference between amplitude voltage channels	V_{ODP}	—	—	50	mV
		Difference between common voltage channels	V_{OSP}	—	—	50	mV

2. AC Characteristics (Sub-LVDS)

INCK, XCLR, XVS (input), XHS (input) (Sub-LVDS)

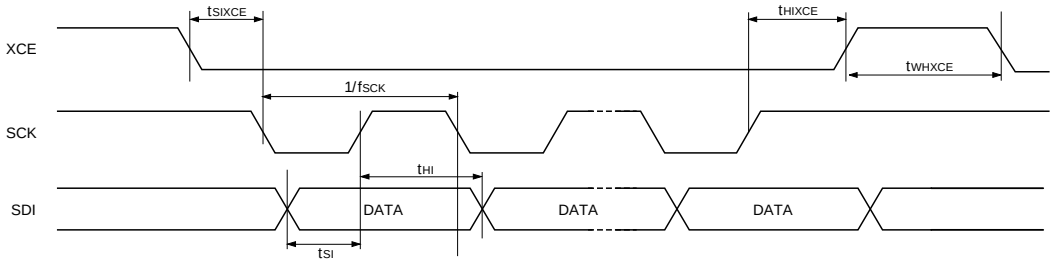


INCK, XCLR, XVS (input), XHS (input) (Sub-LVDS)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	71.0	72.0	73.0	MHz	INCK 72 MHz setting
		35.5	36.0	36.5	MHz	INCK 36 MHz setting
		23.7	24.0	24.3	MHz	INCK 24 MHz setting
		11.9	12.0	12.1	MHz	INCK 12 MHz setting
INCK Low level pulse width	twl	5	—	—	ns	
INCK High level pulse width	twh	5	—	—	ns	
Clock duty	—	40	50	60	%	
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	
XVS Low level pulse width	t_{LOW}	55	—	167	ns	
XHS Low level pulse width	t_{LOW}	55	—	167	ns	
XVS fall – XHS fall width	t_{HFDLY}	0	—	—	ns	
XVS fall – XHS rise width	t_{HRDLY}	55	—	167	ns	

Serial Communication (Sub-LVDS)

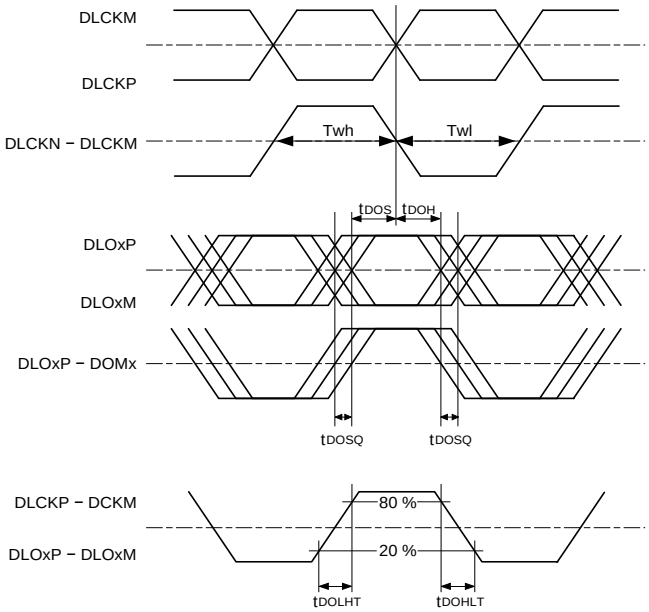
Serial Control Interface Timing



Serial Control Interface Timing (Sub-LVDS)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	—	36	MHz
SDI input setup time	t_{SI}	7	—	—	ns
SDI input hold time	t_{HI}	7	—	—	ns
XCE input setup time	t_{SIXCE}	10	—	—	ns
XCE input hold time	t_{HIXCE}	10	—	—	ns
XCE High level pulse width	t_{WHXCE}	27			ns

Sub-LVDS Output (Sub-LVDS)



Note) "x" stands for the number of 0 to 9 and the time chart is specified for all output channels.

Sub-LVDS Output

(Termination resistance: 100 Ω, load capacitance: 0 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DO skew time (including jitter)	t_{DOSQ}	—	—	361	ps	Data rate 288 MHz DDR
DO setup time	t_{DOS}	420	—	—	ps	Data rate 288 MHz DDR
DO hold time	t_{DOH}	420	—	—	ps	Data rate 288 MHz DDR
DO rise time	t_{DOLHT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DO fall time	t_{DOHLT}	—	500	—	ps	Simulated value with load capacitance (4 pF)
DCK duty cycle	D_{DCDCK}	45	50	55	%	
DCK pulse width	Twh, Twl	1319	—	—	ps	Including period jitter

Spectral Sensitivity Characteristics (CSI-2 and Sub-LVDS)

(Excludes lens characteristics and light source characteristics)

TBD

Image Sensor Characteristics (CSI-2 and Sub-LVDS)

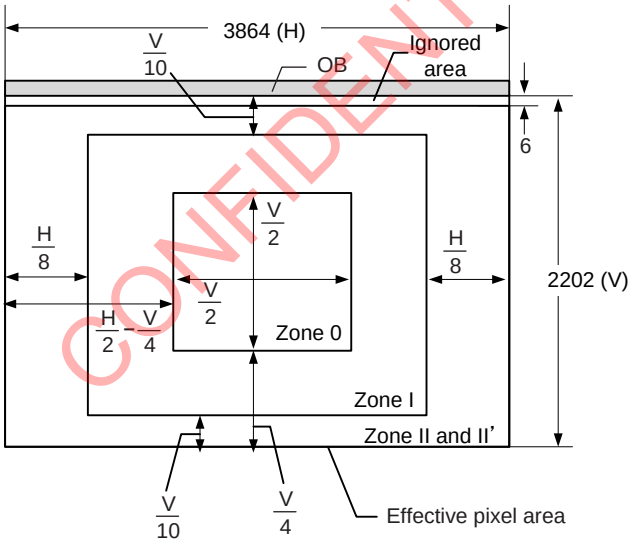
(V_{ADD} = 2.8 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, V_{DDD3} = 1.2 V, Tj = 60 ˚C, 29.97 frame/s, Reference Gain (0 dB))

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	TBD	TBD	TBD	digit*1	1	1/30 s integration conversion value Zone 0
Sensitivity ratio	R	Rr	TBD	—	TBD	%	1	Zone 0
	B	Rb	TBD	—	TBD	%	1	
Saturation signal		Vsat	TBD	—	—	digit*1	2	Zone 0 to II’
Dark signal		Vdt	0	—	TBD	digit*1	3	1/30 s integration conversion value Zone 0 to II’
Dark signal shading		ΔVdt	0	—	TBD	digit*1	4	1/30 s integration conversion value Zone 0 to II’

*1 Shows digit when 12-bit output. 1 digit ≈ TBD mV when 12-bit output (1 digit ≈ TBD mV when 10-bit output).

1. Zone Definition of Image Sensor Characteristics

Zone definition of image sensor characteristics and reference position during dark signal measurement are shown below.



Zone Definition of Image Sensor Characteristics and Reference Position during Dark Signal Measurement

Zone Definition of Image Sensor Characteristics

Image Sensor Characteristics Measurement Method (CSI-2 and Sub-LVDS)

1. Measurement Conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
(2) In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

2. Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

3. Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance –TBD mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, Sensitivity ratio
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/TBD s, measure the Gr, Gb, R and B signal outputs (VGr, VGb, VR and VB) at the center of the screen which is zone 0, and substitute the values into the following formula

VG = (VGr + VGb) / 2
Sg = VG × TBD/30 [digit]
Rr = VR/VG × 100 [%]
Rb = VB/VG × 100 [%]

2. Saturation signal
Set the measurement condition to the standard imaging condition II. Adjust the luminous intensity to 20 times the intensity with the average value of the G (= (Gr + Gb)/2) signal output, TBD digit when 10-bit output (TBD digit when 12-bit output). Measure the minimum values of the Gr, Gb, R and B signals when shooting in rolling shutter mode.

3. Dark signal
   Measure the average value (Vdt [digit]) of the signal output in zone 0 to zone II' in the light-obstructed state. Define the average value of the signal output accumulated in 1 frame period (t1v) as Vdt1V and the average value of the signal output accumulated in the shortest period (1H period: t1h) as Vdt1H, and then substitute the values into the following formula.

   $Vdt = (Vdt1V – Vdt1H) / (t1v – t1h) /30$ [digit]

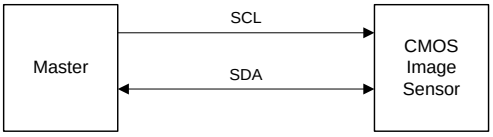
4. Dark signal shading
   Following the item 4, measure the maximum value (Vdmax [digit]) and minimum value (Vdmin [digit]) of the dark signal output, and substitute the values into the following formula.

   $\Delta Vdt = Vdmax – Vdmin$ [digit]

Setting Registers Using I²C Communication (When Using CSI-2)

Description of Setting Registers When Using I²C Communication

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R / W[*1]

[*1] R/W is data direction bit

R / W

R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

Pin Connection of Serial Communication Operation Specifications When Using I²C Communication

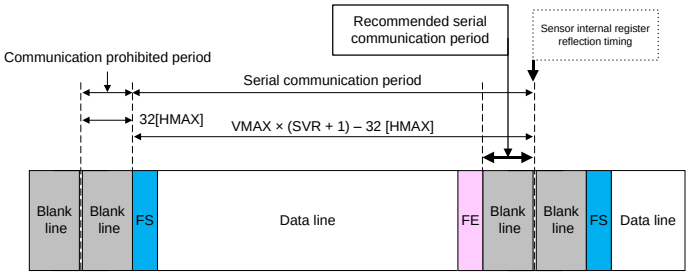
The pin connection of serial communication method conforms to the Camera Control Instance (CCI). CCI is an I²C fast-mode compatible interface, and the data transfer protocol is I²C standard.
This pin connection of serial communication circuit can be used to access the control-registers and status-registers of the sensor.

I²C pin description

Symbol	Pin No.	Remarks
SCL	E1	Serial clock input
SDA	E2	Serial data communication

Register Communication Timing When Using I²C Communication

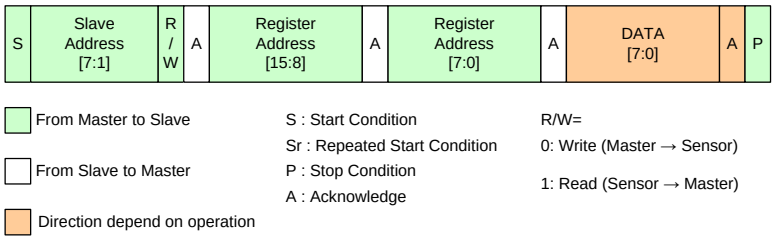
In I²C communication system, register setting can be performed during the period when communication is from the following figure “VMAX × (SVR + 1) − 32[HMAX]”.
Perform I²C communication within “FS of next frame − 32[HMAX]” period (recommended serial communication period) after FE period end to prevent noise. However, for non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), then register communication can be performed other than during the recommended serial communication period of those frames.



Register Communication Timing When Using I²C Communication

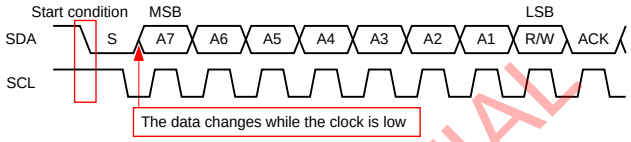
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

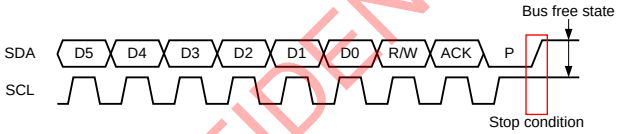


I²C Communication Protocol

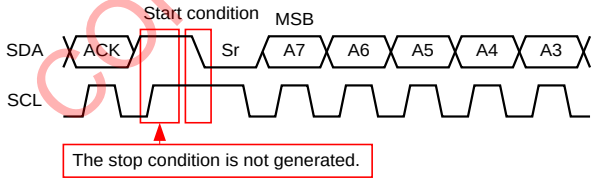
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) is transferred. Data is transferred at the clock cycle of SCL. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

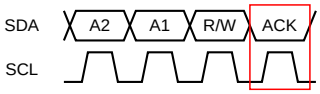


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge and release (does not drive) SDA.



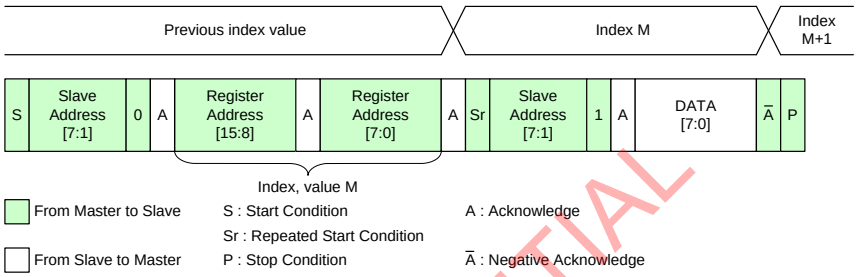
Acknowledge

Register Write and Read

This sensor supports to four read operations and two write operations.
In addition, INCK signal must be driven during the I^2C serial communication period.

Single Read from Random Location

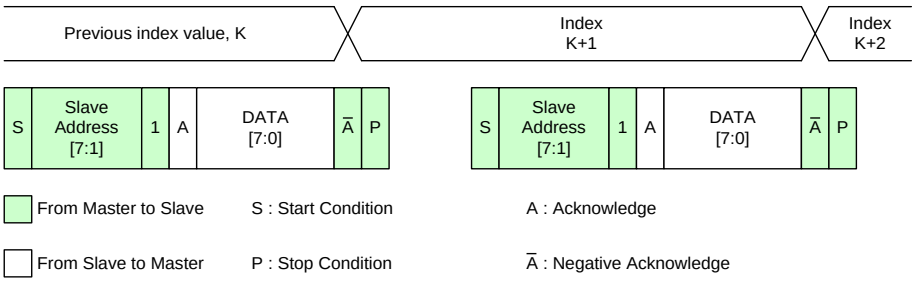
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data,it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

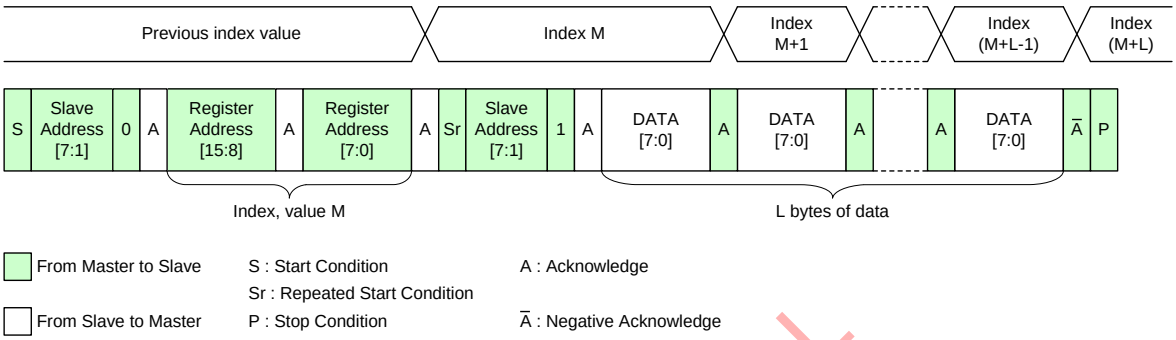
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

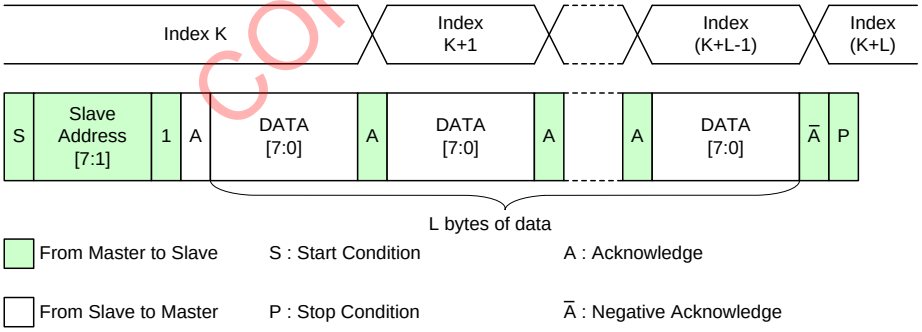
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

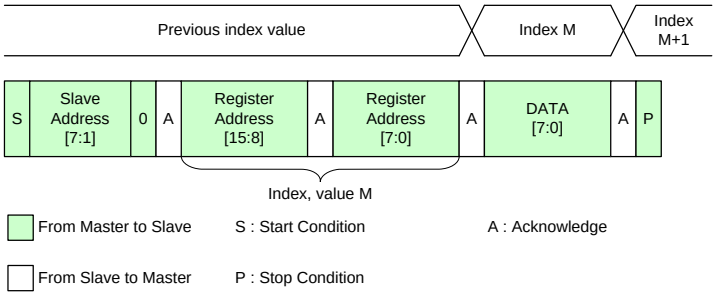
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

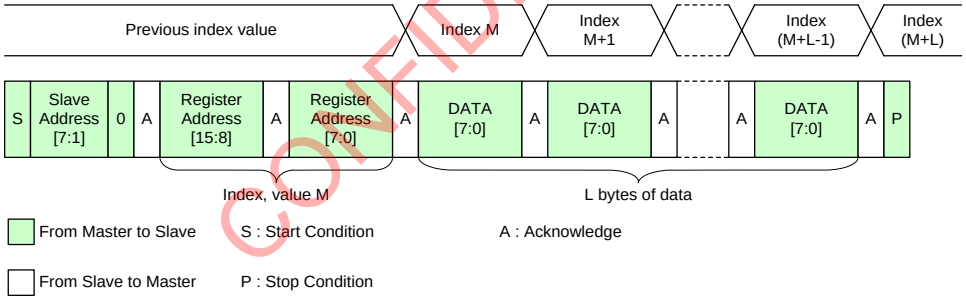
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



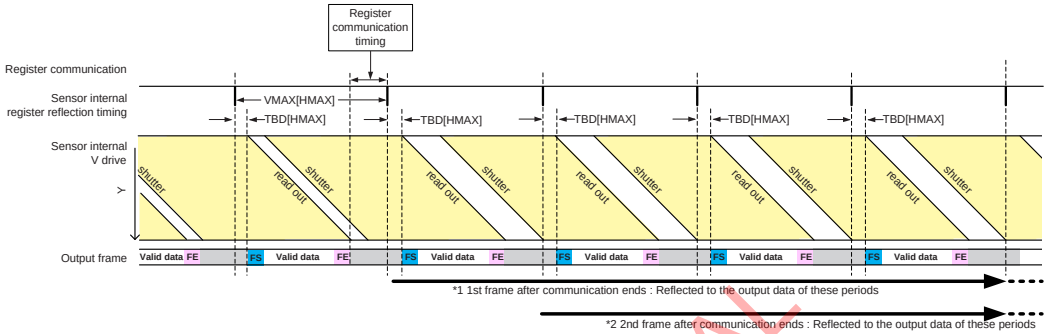
Sequential Write Starting from Random Location

Register Value Reflection Timing to Output Data (CSI-2)

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Explanation
*1 1st frame after communication ends	The communication contents are reflected to the output data from 1st frame after communication ends.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from 2nd frame after communication ends.
Immediately	The communication contents are reflected immediately.

For which reflection timing of each register, see “Register Map” on pages TBD.



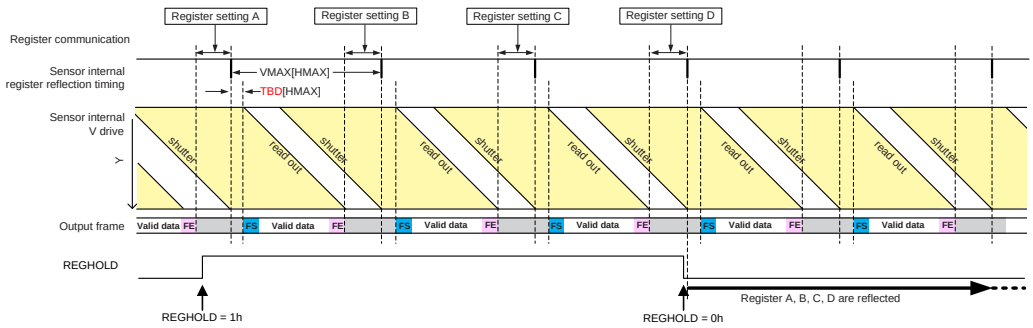
Register Value Reflection Timing to Output Data (CSI-2)

Register Hold Setting (CSI-2)

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD for the registers of which reflection timing is frame unit (*1 and *2).
Registers are set when REGHOLD = 1h, and REGHOLD is set to “0h” during communication period just before the frame the registers are reflected from.
Register hold function is invalid for the registers of which reflection timing is immediately. Therefore these registers are reflected immediately when even though REGHOLD = 1h.

REGHOLD Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
REGHOLD	302Dh	—	[0]	0h	Normal communication Reflecting register setting when register settings are held
				1h	Register setting hold



Example of REGHOLD operation (CSI-2)

Setting Registers Using Serial Communication (When Using Sub-LVDS)

Setting Registers Using Serial Communication (Sub-LVDS)

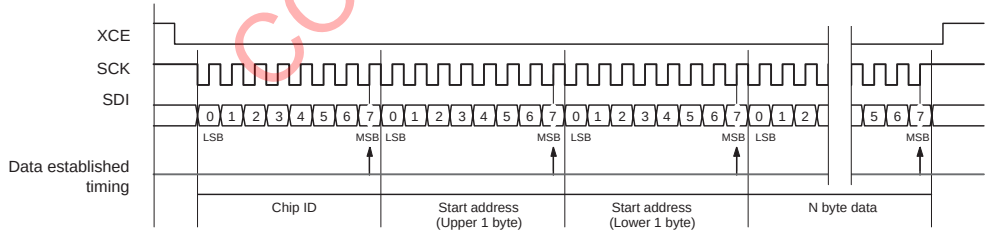
Sensor operation is controlled by the register settings. Follow the procedure below and make the register settings by serial communication.

1. Set XCE Low to enable the chip's serial communication function.
2. Transmit serial data (SDI) synchronized with SCK 1 bit at a time from the lower bits.
3. Transmit the Chip ID (fixed value: 81h) in the first byte.
4. Transmit the address value of the register to be set in the second and third bytes.
5. Transmit the register setting value to the address designated by the second and third bytes in the fourth byte.
6. Transmit the register setting value to the address following the address designated by the second and third bytes in the fifth byte.
7. Transmit the register setting values to subsequent addresses in order thereafter.
8. Set XCE High to end serial communication.

The sensor clears the Chip ID and address setting data by setting XCE High.
Therefore, the Chip ID and address settings must also be made when the next serial communication is performed.
Continuous write across upper bytes is prohibited. When writing across upper bytes, first complete the above sequence, and then perform communication again. In addition, when jumping to a discontinuous address, also first complete the above sequence, and then perform communication again.
Perform serial communication within the 6XHS period (recommended serial communication period) after the fall of XVS to avoid affecting the image quality.
Settings made by serial communication are basically updated immediately each time 1 byte of setting values is transmitted. However, in some exceptional cases (electronic shutter setting, etc.), register setting values are updated immediately before the start of readout immediately after the recommended serial communication period (7th XHS).
For details, see “Register Map” on pages TBD and “1. Register Value Reflection Timing to Output Data” on page TBD.

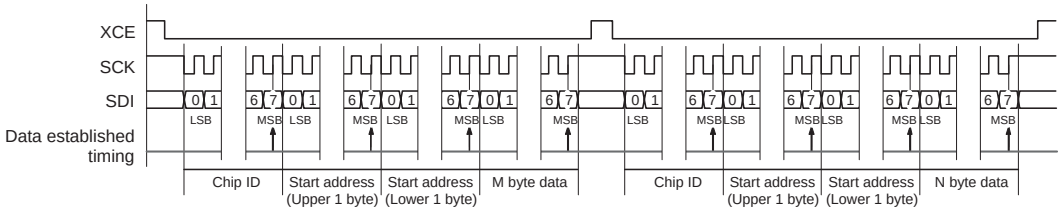
Note) 1. Communication is always accepted.
2. Communication should be completed within the recommended serial communication period to prevent noise. However, this restriction does not apply during the readout period of non-picture frames in which noise is ignored (immediately after power-on or immediately after switching the drive mode, etc.), so register communication can be performed other than during the communication period of those frames.

Example of Serial Communication Timing 1



Example of Serial Communication 1

Example of Serial Communication Timing 2



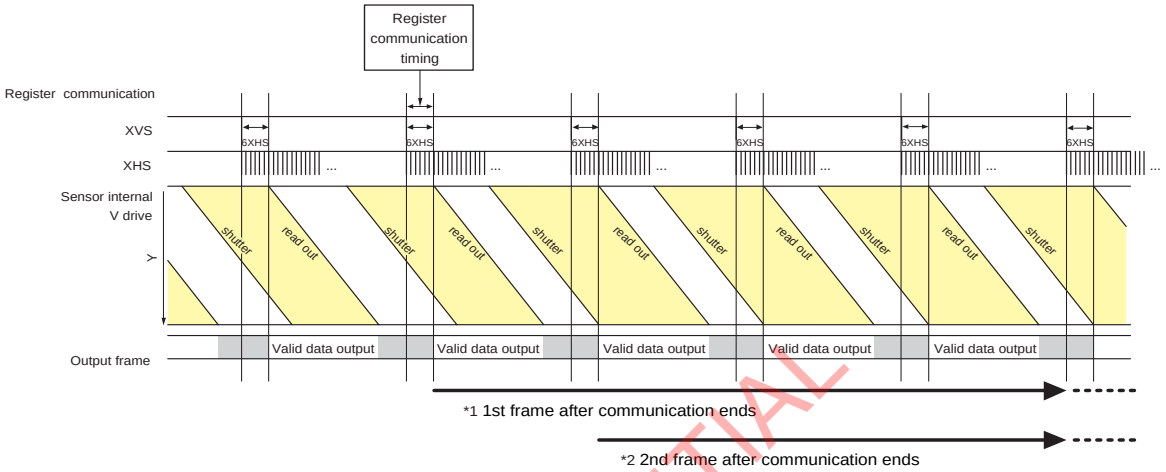
Example of Serial Communication 2

Register Value Reflection Timing to Output Data (Sub-LVDS)

The register values established by register communication are reflected to the output data at the following timings.

Reflection timing	Description
*1 1st frame after communication ends	The communication contents are reflected to the output data from the V period during which communication was performed.
*2 2nd frame after communication ends	The communication contents are reflected to the output data from the next V period after the V period during which communication was performed.

For which reflection timing of each register, see “Register Map” on pages TBD.



Register Value Reflection Timing to Output Data (Sub-LVDS)

Register Map

Address		Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2	Sub-LVDS						
3000h	0000h	[0]	1h	Immediately	STANDBY	0h : Normal operation 1h : Overall standby	Setting range: 0h to 1h
		[1]	1h	Immediately	STBLOGIC	0h: Normal operation 1h: Digital circuit standby other than serial communication block	Setting range: 0h to 1h
		[2]	0h			—	Set the default value.
		[3]	0h	Immediately	STBMIPI	0h: CSI-2 on 1h: CSI-2 standby	CSI-2: set to 0h Sub-LVDS: set to 1h
		[4]	1h	Immediately	STBDV	0h: Normal operation 1h: Frequency demultiplier standby	Setting range: 0h to 1h
		[7:5]	0h			—	Set the default value.
3001h	0001h	[3:0]	0h			—	Set the default value.
		[4]	0h	*1	CLPSQRST	When changing form 0h to 1h: Resets the internal clamp circuit operation mode	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
		[7:5]	0h			—	Set the default value.
—	0002h	[0]	0h	*1	SSBRK	Sub-LVDS only When changing form 0h to 1h: Interrupt enable	Setting range: 0h to 1h After the interrupt, the value is automatically returned to 0h.
		[7:1]	00h			—	Set the default value.
—	0003h	[3:0]	7h	*1	STBLVDS	Sub-LVDS only 0h: 10ch, 1h: 8ch, 2h: 6ch, 3h: 4ch, 4h: 2ch, 5h: 1ch 7h: All channel standby	Setting range: 0h to 5h, 7h
		[7:4]	3h	*1	LANESEL	Sub-LVDS only 0h: 10ch, 1h: 8ch, 2h: 6ch, 3h: 4ch, 4h: 2ch, 5h: 1ch 7h: All channel standby	Setting range: 0h to 5h, 7h
3004h	0004h	[7:0]	03h	*1	MDSEL1	Mode select 1	Set the value according to each readout mode register setting.
3005h	0005h	[7:0]	31h	*1	MDSEL2	Mode select 2	Set the value according to each readout mode register setting.
3006h	0006h	[7:0]	00h	*1	MDSEL3	Mode select 3	Set the value according to each readout mode register setting.
3007h	0007h	[7:0]	09h	*1	MDSEL4	Mode select 4	Set the value according to each readout mode register setting.
3008h	0008h	[0]	0h	*1	SMD	0h: Rolling shutter 1h: Global reset shutter	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
—	0009h	[0]	0h	Immediately	DCKRST	Sub-LVDS only When changing form 0h to 1h: Clock phase reset of Sub-LVDS	Setting range: 0h to 1h After the reset, the value is automatically returned to 0h.
		[7:1]	00h			—	Set the default value.
300Ah	000Ah	[7:0]	000h	*1	PGC	Analog gain setting	Setting range: 000h to 7A5h
300Bh	000Bh	[2:0]					
		[7:3]	00h			—	Set the default value.

Address		Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2	Sub-LVDS						
300Ch	000Ch	[7:0]	0008h	*2	SHR	Specifies the integration start horizontal period	Setting range is shown in ”Description of Registers”
300Dh	000Dh	[7:0]					
300Eh	000Eh	[7:0]	0000h	*2	SVR	Specifies the integration shutdown vertical period	Setting range: 0000h to FFFFh
300Fh	000Fh	[7:0]					
3012h	0012h	[3:0]	0h	*1	DGAIN	Digital gain setting 0h: 0dB, 1h: +6dB, 2h: +12dB, 3h: +18dB	Setting range: 0h to 3h
		[7:4]	0h			—	Set the default value.
3018h	—	[1:0]	3h	Immediately	SYNCDRV	CSI-2 only XHS/XVS pulse output enable 2h: XHS/XVS is output 3h: XHS/XVS is Hi-Z	Refer to the “Standby Cancel Sequence” when using XHS/XVS output
		[7:2]	28h			—	Set the default value.
301Ah	001Ah	[0]	0h	*2	MDVREV	0h : Vertical direction normal readout 1h : Vertical direction inversion readout	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
302Dh	—	[0]	0h	Immediately	REGHOLD	CSI-2 only Register setting hold function	Setting range is shown in ”Description of Registers”
		[7:1]	00h			—	Set the default value.
3037h	0037h	[0]	0h	*1	HTRIMMING_EN	Horizontal arbitrary cropping enable	Setting range is shown in ”Description of Registers”
		[7:1]	00h			—	Set the default value.
3038h	0038h	[7:0]	00h	*1	HTRIMMING_START	Horizontal cropping start position	Setting range is shown in ”Description of Registers”
3039h	0039h	[4:0]	00h				
		[7:5]	0h			—	Set the default value.
303Ah	003Ah	[7:0]	00h	*1	HTRIMMING_END	Horizontal cropping end position + 1	Setting range is shown in ”Description of Registers”
303Bh	003Bh	[4:0]	00h				
		[7:5]	0h			—	Set the default value.
303Eh	003Eh	[1:0]	2h	Immediately	SYS_MODE	Select use Interface 0h, 1h: Sub-LVDS 2h: MIPI1.44Gbps	Refer to the “Standby Cancel Sequence” Setting range: 0h to 2h
		[7:2]	00h			—	Set the default value.
3045h	0045h	[7:0]	32h	Immediately	BLKLEVEL	Digital black level offset setting	Setting range: 0h to FFh 10-bit readout mode: 1 digit/1h 12-bit readout mode: 4 digit/1h
30DDh	00DDh	[0]	0h	*1	VWIDCUTEN	Vertical arbitrary cropping enable	Setting range is shown in ”Description of Registers”
		[7:1]	00h			—	Set the default value.
30DEh	00DEh	[7:0]	000h	*1	VWIDCUT	Width of vertical arbitrary cropping	Setting range is shown in ”Description of Registers”
30DFh	00DFh	[2:0]					
		[7:3]	00h			—	Set the default value.
30E0h	00E0h	[7:0]	000h	*1	VWINPOS	Start position of vertical arbitrary cropping (two's complement)	Setting range is shown in ”Description of Registers”
30E1h	00E1h	[2:0]					
		[7:3]	00h			—	Set the default value.

Address		Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2	Sub-LVDS						
30E2h	00E2h	[7:0]	00h	Immediately	VCUTMODE	Mode setting register	Set the value according to each readout mode register setting.
—	00E6h	[7:0]	00h	Immediately	PLL_CKEN	Sub-LVDS only Clock control setting	Refer to the ”Standby Cancel Sequence”
—	00E8h	[7:0]	00h	Immediately	PACKEN	Sub-LVDS only Clock control setting	Refer to the ”Standby Cancel Sequence”
30EEh	00EEh	[7:0]	00h	*1	PSMOVEN	Mode setting	Setting range is shown in ”Description of Registers”
30F4h	—	[0]	1h	Immediately	XMSTA	CSI-2 only Master mode operation 0h: Master mode start 1h: Master mode stop	Refer to the ”Standby Cancel Sequence”
		[7:1]	00h			—	Set the default value.
30F6h	—	[7:0]	0104h	*1	HMAX	CSI-2 only Horizontal drive period length	Setting range is shown in ”Description of Registers”
30F7h	—	[7:0]					
30F8h	—	[7:0]	00905h	*1	VMAX	CSI-2 only Vertical drive period length	Setting range is shown in ”Description of Registers”
30F9h	—	[7:0]					
30FAh	—	[3:0]					
30FAh	—	[7:4]	00h			—	Set the default value.
310Bh	010Bh	[0]	1h	immediately	STBPL_IF	PLL standby control register for IF	Refer to the ”Standby Cancel Sequence”
		[3:1]	0h			—	Set the default value.
		[4]	1h	immediately	STBPL_AD	PLL standby control register for AD	Refer to the ”Standby Cancel Sequence”
		[7:5]	0h			—	Set the default value.
3111h	0111h	[0]	0h	immediately	SLEEP	Low power consumption drive in exposure time	Setting range: 0h to 1h
		[7:1]	00h			—	Set the default value.
3120h	0120h	[7:0]	0080h	immediately	PLRD1	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3121h	0121h	[7:0]					
3122h	0122h	[7:0]	03h	Immediately	PLRD2	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3129h	0129h	[7:0]	0Dh	immediately	PLRD3	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
312Ah	012Ah	[7:0]	00h	immediately	PLRD4	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
312Dh	012Dh	[7:0]	03h	immediately	PLRD5	Input clock frequency setting register	Setting range is shown in ”Description of Registers”
3130h	—	[7:0]	02E2h	*1	WRITE_VSIZE	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
3131h	—	[4:0]					
		[7:5]	0h			—	Set the default value.
3132h	—	[7:0]	02DEh	*1	Y_OUT_SIZE	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
3133h	—	[4:0]					
		[7:5]	0h			—	Set the default value.
3304h	—	[7:0]	0005h	immediately	PSMIPI1	CSI-2 only Timing setting for CSI-2	Set to TBDh
3305h		[7:0]					
3306h	—	[7:0]	0005h	immediately	PSMIPI2	CSI-2 only Timing setting for CSI-2	Set to TBDh
3307h		[7:0]					

Address		Bit assign-ment	Default value	Reflection timing	Register name	Function	Remarks
CSI-2	Sub-LVDS						
—	032Ch	[7:0]	00FFh	immediately	PSLVDS1	Sub-LVDS only Timing setting for Sub-LVDS	Refer to “Description of Register” for the setting value.
	032Dh	[7:0]					
—	034Ah	[7:0]	00FFh	immediately	PSLVDS2	Sub-LVDS only Timing setting for Sub-LVDS	Refer to “Description of Register” for the setting value.
	034Bh	[7:0]					
3590h	—	[7:0]	0005h	immediately	PSMIPI3	CSI-2 only Timing setting for CSI-2	Set to TBDh
3591h		[7:0]					
—	05B6h	[7:0]	00FFh	immediately	PSLVDS3	Sub-LVDS only Timing setting for Sub-LVDS	Refer to “Description of Register” for the setting value.
	05B7h	[7:0]					
—	05B8h	[7:0]	00FAh	immediately	PSLVDS4	Sub-LVDS only Timing setting for Sub-LVDS	Refer to “Description of Register” for the setting value.
	05B9h	[7:0]					
3686h	—	[7:0]	0004h	immediately	PSMIPI4	CSI-2 only Timing setting for CSI-2	Set to TBDh
3687h		[7:0]					
3A41h	—	[5:0]	04h	*1	MDSEL5	CSI-2 only Mode setting	Set the value according to each readout mode register setting.
		[7:6]	0h			—	Set the default value.

1. Description of Register

Total Standby Control (CSI-2 and Sub-LVDS)

All sensor operation is stopped and the standby mode that reduces power consumption is established by setting the overall standby control register STANDBY to “1h”.
(Standby mode is established immediately after reset.)
The serial communication block operates even in standby mode, so standby mode can be canceled by setting “0h” in the STANDBY register.

STANDBY Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
STANDBY	3000h	0000h	[0]	0h	Normal operation
				1h	Overall standby

Digital Circuit Standby Control (CSI-2 and Sub-LVDS)

When power-on, set the digital circuit standby control register STBLOGIC according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBLOGIC Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
STBLOGIC	3000h	0000h	[1]	0h	Normal operation
				1h	Digital circuit standby other than serial communications block

Frequency Demultiplier Standby Control (CSI-2 and Sub-LVDS)

When power-on, set the frequency demultiplier standby control register STBDV according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

STBDV Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
STBDV	3000h	0000h	[4]	0h	Normal operation
				1h	Frequency demultiplier standby

Clamp Reset (CSI-2 and Sub-LVDS)

The internal clamp circuit operation status is reset by the clamp reset register CLPSQRST. Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the reset process, so there is no need to write “0h”.

CLPSQRST Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
CLPSQRST	3001h	0001h	[4]	Changed from 0h to 1h	Resets the internal clamp circuit operation status

Input Frequency Setting (CSI-2 and Sub-LVDS)

The input clock frequency can be set arbitrarily by setting input clock setting register PLRD1, PLRD2, PLRD3, PLRD4 and PLRD5.
Set this registers according to the recommended sequence during power-on or when canceling standby mode.

Input Frequency Setting Registers

Name	CSI-2 Address	Sub-LVDS Address	Bit	Function
PLRD1 [7:0]	3120h	0120h	[7:0]	Input clock frequency setting register
PLRD1 [15:8]	3121h	0121h	[7:0]	
PLRD2 [7:0]	3122h	0122h	[7:0]	Input clock frequency setting register
PLRD3 [7:0]	3129h	0129h	[7:0]	Input clock frequency setting register
PLRD4 [7:0]	312Ah	012Ah	[7:0]	Input clock frequency setting register
PLRD5 [7:0]	312Dh	012Dh	[7:0]	Input clock frequency setting register

PLRD1 to PLRD5 Setting (CSI-2)

		Register value				
		PLRD1	PLRD2	PLRD3	PLRD4	PLRD5
Input clock frequency [MHz]*1	6	TBD	TBD	TBD	TBD	TBD
	12	TBD	TBD	TBD	TBD	TBD
	18	00A0h	01h	68h	01h	02h
	24	TBD	TBD	TBD	TBD	TBD

*1 Consult your Sony sales representative concerning other input frequency settings.

PLRD1 to PLRD5 Setting (Sub-LVDS)

		Register value				
		PLRD1	PLRD2	PLRD3	PLRD4	PLRD5
Input clock frequency [MHz]*1	12	TBD	TBD	TBD	TBD	TBD
	24	TBD	TBD	TBD	TBD	TBD
	36	TBD	TBD	TBD	TBD	TBD
	72	0080h	03h	68h	03h	02h

Vertical Direction Readout Inversion (CSI-2 and Sub-LVDS)

The direction of vertical readout order can be set by the vertical direction readout inversion register MDVREV. See “Optical Black Array and Readout Scan Direction” for details of readout image.

MDVREV Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
MDVREV	301Ah	001Ah	[0]	0h	Vertical direction normal readout
				1h	Vertical direction inversion readout

Analog Gain (CSI-2 and Sub-LVDS)

The analog gain value can be set by setting the analog gain register PGC. Set the lower 8 bits and the upper 3 bits, for total of 11 bits.

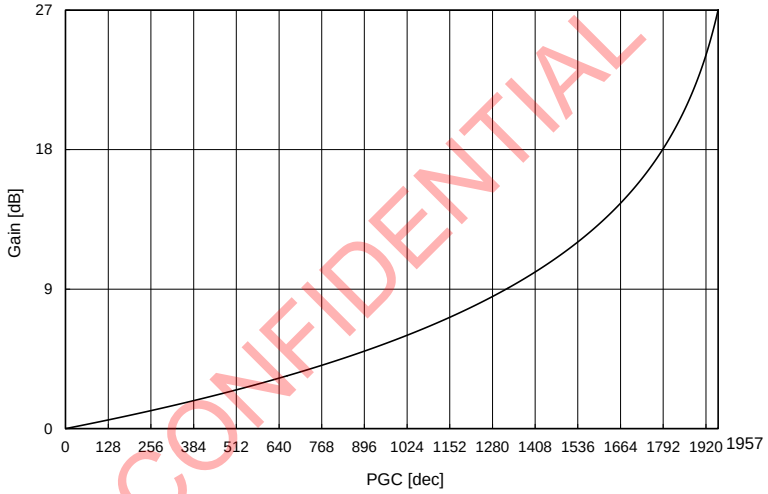
PGC Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
PGC [7:0]	300Ah	000Ah	[7:0]	0h to 7A5h (0d to 1957d)	Analog gain setting
PGC [10:8]	300Bh	000Bh	[2:0]		

In addition, the figure below shows the relationship between the register setting value and the gain value. When the register setting value is “0h (0d)”, the gain value is 0 dB (minimum settable value), and when “7A5h (1957d)”, the gain value is approximately 27 dB (maximum settable value).

Relation Formula

Gain [dB] = –20log{(2048 – PGC [10:0]) /2048}



Relationship between Register Setting Value and Set Gain Value

Digital Gain (CSI-2 and Sub-LVDS)

The digital gain applied to the data after pixel binning can be set by the digital gain setting register DGAIN.

DGAIN Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
DGAIN [3:0]	300Ah	000Ah	[3:0]	0h	Digital gain setting value = 0 dB
				1h	Digital gain setting value = +6 dB
				2h	Digital gain setting value = +12 dB
				3h	Digital gain setting value = +18 dB

Digital Black Level Offset (CSI-2 and Sub-LVDS)

The black level offset applied to the data after digital gain processing by the DGAIN register is set by the digital black level offset setting register BLKLEVEL.
Note that the offset unit changes according to the readout drive mode.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 digit. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 digits.

BLKLEVEL Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
BLKLEVEL [7:0]	3045h	0045h	[0]	00h to FFh	Digital black level offset setting

Vertical Arbitrary Cropping (CSI-2 and Sub-LVDS)

Arbitrary cropping in vertical direction can be enabled by setting vertical arbitrary cropping enable register VWIDCUTEN, and arbitrary cropping in vertical direction can be performed by designating cropping position of vertical direction to setting cropping width of vertical direction register VWINPOS and VWIDCUT. See “Vertical Arbitrary Cropping Function” on page TBD for details.

VWIDCUTEN, VWIDCUT, VWINPOS Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Function
VWIDCUTEN	30DDh	00DDh	[0]	Vertical arbitrary cropping enable
VWIDCUT [7:0]	30DEh	00DEh	[7:0]	Width of vertical arbitrary cropping
VWIDCUT [10:8]	30DFh	00DFh	[2:0]	
VWINPOS [7:0]	30E0h	00E0h	[7:0]	Start position of vertical arbitrary cropping (two's complement)
VWINPOS [10:8]	30E1h	00E1h	[2:0]	

Horizontal Arbitrary Cropping (CSI-2 and Sub-LVDS)

Arbitrary cropping in horizontal direction can be enabled by setting horizontal arbitrary cropping enable register HTRIMMING_EN, and arbitrary cropping in horizontal direction can be performed by designating cropping position of horizontal direction to setting cropping position of horizontal direction register HTRIMMING_START and HTRIMMING_END. See “Horizontal Arbitrary Cropping Function” on page TBD for details.

HTRIMMING_EN, HTRIMMING_START, HTRIMMING_END Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Function
HTRIMMING_EN	3037h	0037h	[0]	Horizontal arbitrary cropping enable
HTRIMMING_START [7:0]	3038h	0038h	[7:0]	Horizontal cropping start position
HTRIMMING_START [12:8]	3039h	0039h	[4:0]	
HTRIMMING_END [7:0]	303Ah	003Ah	[7:0]	Horizontal cropping end position +1
HTRIMMING_END [12:8]	303Bh	003Bh	[4:0]	

Readout Drive Mode (CSI-2 and Sub-LVDS)

The readout drive mode of this sensor can be switched by setting the readout drive mode register MDSEL1 to 5, vertical arbitrary cropping registers, horizontal arbitrary cropping registers, VCUTMODE, HMAX and VMAX, WRITE_VSIZE, Y_OUT_SIZE, PSMOVEN, PSLVDS. When changing the mode, make the setting according to “Register Settings for Each Readout Drive Mode” on pages TBD.

Readout Drive Pulse Timing (CSI-2 and Sub-LVDS)

When power-on, set the readout drive pulse timing registers PLSTMG and PSMIPI1 to 4 (MIPI only) which are shown in the following table as the initialization registers. See the standby cancel sequence for timing of sending.

Timing Setting for CSI-2

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value
PSMIPI1 [7:0]	3304h	—	[7:0]	Set to TBDh
PSMIPI1 [15:8]	3305h	—	[7:0]	
PSMIPI2 [7:0]	3306h	—	[7:0]	Set to TBDh
PSMIPI2 [15:8]	3307h	—	[7:0]	
PSMIPI3 [7:0]	3590h	—	[7:0]	Set to TBDh
PSMIPI3 [15:8]	3591h	—	[7:0]	
PSMIPI4 [7:0]	3686h	—	[7:0]	Set to TBDh
PSMIPI4 [15:8]	3687h	—	[7:0]	
PLSTMG TBD	TBD	—	[7:0]	TBD

Timing Setting for Sub-LVDS

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value
PLSTMG TBD	—	TBD	[7:0]	TBD

Sleep (CSI-2 and Sub-LVDS)

SLEEP register reduces the power consumption during the integration time. See “Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation” and “Low Power Consumption Drive in Exposure Time When Using Global Reset Shutter Operation”.

SLEEP Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
SLEEP	3111h	0111h	[0]	0h	Normal operation
				1h	Circuit standby

PLL Standby Control (CSI-2 and Sub-LVDS)

When power-on, set the PLL standby control registers STBPL_IF and STBPL_AD according to the standby cancel sequence. These registers are valid only when STANDBY = 0h.

STBPL_IF and STBPL_AD Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Function
STBPL_IF	310Bh	010Bh	[0]	PLL standby control register for IF
STBPL_AD	310Bh	010Bh	[4]	PLL standby control register for AD

CSI-2 Standby Control (CSI-2 only)

CSI-2 can be standby by CSI-2 standby register STBMIPI.

STBMIPI Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
STBMIPI	3000h	—	[3]	0h	Normal operation
				1h	CSI-2 standby

Master Mode Operation Control (CSI-2 only)

When power-on, set the master mode operation control register XMSTA according to the standby cancel sequence. This register is valid only when STANDBY = 0h.

XMSTA Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
XMSTA	30F4h	—	[0]	0h	Master mode start
				1h	Master mode stop

Horizontal Drive Period Length and Vertical Drive Period Length (CSI-2 only)

When using CSI-2, Horizontal drive period length (Unit: Number of 72MHz clock) and vertical drive period length (Unit: Number of horizontal drive period) can be set by horizontal drive period length setting register HMAX and vertical drive period length setting register VMAX.

HMAX, VMAX Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
HMAX [7:0]	30F6h	—	[7:0]	Setting range is shown in ”Description of Registers”	Horizontal drive period length
HMAX [15:8]	30F7h	—	[7:0]		
VMAX [7:0]	30F8h	—	[7:0]	Setting range is shown in ”Description of Registers”	Vertical drive period length
VMAX [15:8]	30F9h	—	[7:0]		
VMAX [19:16]	30FAh	—	[3:0]		

Calculating formula of vertical drive period (1 frame) is shown below.

Vertical drive period length [s] = VMAX value × (SVR value + 1) × HMAX value/ (72×10^6)

See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page TBD for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Break Mode (Sub-LVDS only)

XVS can be subsampled according to SVR. This XVS subsampling operation can be stopped and then restarted from the start of the exposure period using the break mode register SSBRK (address 0002h, bit [0]).
This register automatically returns to “0h” after the break process, so there is no need to write “0h”.

SSBRK Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
SSBRK	—	0002h	[0]	Change from 0h to 1h	Interrupt enable

Sub-LVDS Clock Output Phase Fixed (Sub-LVDS only)

The clock phase relative to the sync code start data in the Sub-LVDS data output is fixed by the Sub-LVDS clock output phase fixing register DCKRST. Make this setting according to the recommended sequence during power-on or when canceling standby mode.
This register automatically returns to “0h” after the phase fixing process, so there is no need to write “0h”.

DCKRST Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
DCKRST	—	0009h	[0]	Change from 0h to 1h	Clock phase reset of Sub-LVDS

Sub-LVDS Standby Control (Sub-LVDS only)

This sensor can set the Sub-LVDS to standby mode according to the setting value by setting the Sub-LVDS standby control register STBLVDS.

STBLVDS Setting

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
STBLVDS [3:0]	—	0003h	[3:0]	0h	10 ch
				1h	8 ch
				2h	6 ch
				3h	4 ch
				4h	2 ch
				5h	1 ch
				Fh	All channel standby

Sub-LVDS Standby Control (Sub-LVDS only)

dec	bin	hex	Function	DLO0	DLO1	DLO2	DLO3	DLO4	DLCK	DLO5	DLO6	DLO7	DLO8	DLO9
STBLVDS[3:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	STBY	Active	Active	Active	STBY	Active	Active	Active
2d	0010b	2h	6 ch	STBY	Active	Active	STBY	Active	Active	Active	STBY	Active	Active	STBY
3d	0011b	3h	4 ch	STBY	STBY	Active	STBY	Active	Active	Active	STBY	Active	STBY	STBY
4d	0100b	4h	2 ch	STBY	STBY	STBY	STBY	Active	Active	Active	STBY	STBY	STBY	STBY
5d	0101b	5h	1 ch	STBY	STBY	STBY	STBY	Active	Active	STBY	STBY	STBY	STBY	STBY
15d	1111b	Fh	All Standby	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY	STBY

Number of LVDS Output Channels Selection (Sub-LVDS only)

This sensor can set the number of output channels according to the setting value by setting the number of Sub-LVDS output channels selection register LANESEL.

LANESEL Setting (Sub-LVDS only)

Name	CSI-2 Address	Sub-LVDS Address	Bit	Register value	Function
LANESEL [3:0]	—	0003h	[7:4]	0h	10 ch
				1h	8 ch
				2h	6 ch
				3h	4 ch
				4h	2 ch
				5h	1 ch

Number of Sub-LVDS Channels Control (Sub-LVDS only)

dec	bin	hex	Function	DLO0	DLO1	DLO2	DLO3	DLO4	DLCK	DLO5	DLO6	DLO7	DLO8	DLO9
LANESEL[3:0]														
0d	0000b	0h	10 ch	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
1d	0001b	1h	8 ch	Active	Active	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Active	Active
2d	0010b	2h	6 ch	Fixed Low	Active	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Active	Fixed Low
3d	0011b	3h	4 ch	Fixed Low	Fixed Low	Active	Fixed Low	Active	Active	Active	Fixed Low	Active	Fixed Low	Fixed Low
4d	0100b	4h	2 ch	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Active	Active	Active	Fixed Low	Fixed Low	Fixed Low	Fixed Low
5d	0101b	5h	1 ch	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Active	Active	Fixed Low	Fixed Low	Fixed Low	Fixed Low	Fixed Low

2. Register Setting for Each Readout Drive Mode

The register setting for each readout drive mode available with this sensor is shown in the table below. These registers should be change according to the mode to use. Set the register to the following value.

Description of Register Setting for Each Readout Drive Mode (CSI-2)

Address (CSI-2)	Bit Assignment	Register Name	Readout mode No. *1						
			0	1	2	3	4	5	6
3004h	[7:0]	MDSEL1	00h	01h	02h	02h	02h	03h	04h
3005h	[7:0]	MDSEL2	07h	01h	27h	21h	61h	31h	31h
3006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h	00h
3007h	[7:0]	MDSEL4	02h	02h	11h	11h	19h	09h	02h
300Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)						
300Fh	[7:0]								
301Ah	[0]	MDVREV	0h: vertical direction normal /1h: inverted						
	[7:1]		00h						
30E2h	[7:0]	VCUTMODE	00h	01h	02h	02h	02h	03h	04h
30F6h	[7:0]	HMAX	Setting horizontal drive period length (72MHz clock unit)*2						
30F7h	[7:0]								
30F8h	[7:0]	VMAX	Setting vertical drive period length (unit: HMAX ×72MHz clock)*						
30F9h	[7:0]								
30FAh	[3:0]								
	[7:4]		0h	0h	0h	0h	0h	0h	0h
30EEh	[7:0]	PSMOVEN	1h	1h	1h	1h	1h	1h	1h
3130h	[7:0]	WRITE_VSIZE	08AAh	0886h	044Eh	044Eh	044Eh	02E2h	0226h
3131h	[4:0]								
	[7:5]		0h	0h	0h	0h	0h	0h	0h
3132h	[7:0]	Y_OUT_SIZE	089Ah	087Eh	0446h	0446h	0446h	02DEh	0222h
3133h	[4:0]								
	[7:5]		0h	0h	0h	0h	0h	0h	0h
3A41h	[5:0]	MDSEL5	10h	08h	08h	08h	08h	04h	04h
	[7:6]		0h	0h	0h	0h	0h	0h	0h

*1 See “Readout Drive Modes” on pages TBD for details of readout mode No.

*2 See “Horizontal/Vertical Operation Period in Each Readout Drive Mode” on page TBD and “ Frame Rate Adjustment” on pages TBD for setting range of HMAX and VMAX in each readout mode, and example of standard setting.

Description of Register Setting for Each Readout Drive Mode (Sub-LVDS)

Address (Sub-LVDS)	Bit Assignment	Register Name	Readout mode No. *1						
			0	1	2	3	4	5	6
0003h	[3:0]	STBLVDS	2h	0h	3h	2h	2h	3h	3h
	[7:4]	LANESEL	2h	0h	3h	2h	2h	3h	3h
0004h	[7:0]	MDSEL1	00h	00h	02h	02h	02h	03h	04h
0005h	[7:0]	MDSEL2	07h	01h	27h	21h	61h	31h	31h
0006h	[7:0]	MDSEL3	00h	00h	00h	00h	00h	00h	00h
0007h	[7:0]	MDSEL4	02h	02h	11h	11h	19h	09h	02h
000Eh	[7:0]	SVR	According to exposure time (See “Frame Rate Adjustment”)						
000Fh	[7:0]								
001Ah	[0]	MDVREV	0h: vertical direction normal /1h: inverted						
	[7:1]		00h						
00E2h	[7:0]	VCUTMODE	00h	00h	02h	02h	02h	03h	04h
00EEh	[7:0]	PSMOVEN	1h	1h	1h	1h	1h	1h	1h
032Ch	[7:0]	PSLVDS1	Set to (XVS period[XHS] – TBD)						
032Dh	[7:0]								
034Ah	[7:0]	PSLVDS2	Set to (XVS period[XHS] – TBD)						
034Bh	[7:0]								
05B6h	[7:0]	PSLVDS3	Set to (XVS period[XHS] – TBD)						
05B7h	[7:0]								
05B8h	[7:0]	PSLVDS4	Set to (XVS period[XHS] – TBD)						
05B9h	[7:0]								

Readout Drive Modes (CSI-2 and Sub-LVDS)

1. Readout Drive Modes

The table below describes the readout drive modes that can be used to operate this sensor.
All of the modes listed in the table below support vertical direction inversion operation (MDVREV = 0h/1h).

Description of Readout Drive Modes

Readout Mode No.	Readout drive mode	Mode description
0	All-pixel scan mode (12-bit)	All pixels are readout with 12-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
1	All-pixel scan mode (10-bit)	All pixels are readout with 10-bit output. This mode can be used together with the global reset shutter function according to the SMD register setting.
2	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning, 12-bit)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
3	Horizontal/vertical 2/2-line binning (Horizontal and vertical weighted binning, 10-bit)	Horizontal and vertical direction 2-line weighted binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
4	Horizontal/vertical 2/2-line binning Low power consumption drive	Horizontal and vertical direction 2-line binning readout of pixels of the same color at the all-pixel scan area. (See the image of binning)
5	Vertical 2/3 subsampling binning horizontal 3 binning	2 of every 3 lines in the vertical direction at the all-pixel scan area are added. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)
6	Vertical 2/8 subsampling horizontal 3 binning	2 of every 8 lines in the vertical direction at the all-pixel scan area are subsampled. Then, 3 pixels of the same color in the horizontal direction are added and output. (See the image of binning)

Imaging Conditions in Each Readout Drive Mode (CSI-2)

Readout mode No.	Imaging conditions					
	Number of MIPI output lanes [lane]	Number of A/D conversion bits [bit]	RAW10/ RAW12	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	4	12	RAW12	3840	2160	Approximately 8.29 M Pixels
1	4	10	RAW10	3840	2160	Approximately 8.29 M Pixels
2	4	12	RAW12	1920	1080	Approximately 2.07 M Pixels
3	4	10	RAW10	1920	1080	Approximately 2.07 M Pixels
4	4	10	RAW10	1920	1080	Approximately 2.07 M Pixels
5	4	10	RAW10	1280	720	Approximately 0.92 M Pixels
6	4	10	RAW10	1280	540	Approximately 0.69 M Pixels

Imaging Conditions in Each Readout Drive Mode (Sub-LVDS)

Readout mode No.	Imaging conditions					
	Number of Sub-LVDS output channels [ch]	Number of A/D conversion bits [bit]	Output data bit length [bit]	Number of horizontal recording pixels	Number of vertical recording pixels	Number of recording pixels
0	6	12	12	3840	2160	Approximately 8.29 M Pixels
1	10	10	10	3840	2160	Approximately 8.29 M Pixels
2	4	12	12	1920	1080	Approximately 2.07 M Pixels
3	6	10	10	1920	1080	Approximately 2.07 M Pixels
4	6	10	10	1920	1080	Approximately 2.07 M Pixels
5	4	10	10	1280	720	Approximately 0.92 M Pixels
6	4	10	10	1280	540	Approximately 0.69 M Pixels

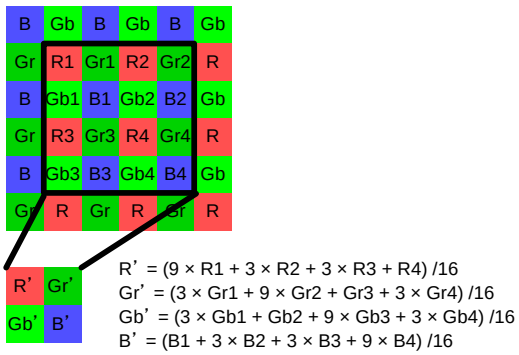
2. Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

The table below shows the relationship between the A/D conversion resolution, number of binning pixels, internal arithmetic processing, and number of output bits in each readout mode.
Note that the number of output bits differs in each mode. In addition the number of output bits is 10 bits. So the weight of 1 digit is 4 times greater than during 12-bit output.

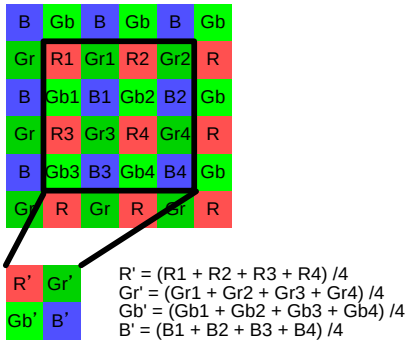
Relationship between Arithmetic Processing and the Number of Output Bits in Each Readout Drive Mode

Readout mode No.	A/D conversion resolution	Vertical pixel processing	Horizontal pixel processing	Total Number of binning pixels	Internal arithmetic processing	Number of output bits
0	12 bits	—	—	—	—	10 bits + 2 bits [*1]
1	10 bits	—	—	—	—	10 bits
2	12 bits	2 binning	2 binning	4 pixels	9/16, 3/16, 3/16, 1/16 (weighted binning [*3])	10 bits + 2 bits [*2]
3	10 bits	2 binning	2 binning	4 pixels	9/16, 3/16, 3/16, 1/16 (weighted binning [*3])	10 bits
4	10 bits	2 binning	2 binning	4 pixels	1/4	10 bits
5	10 bits	2/3 subsampling binning	3 binning	6 pixels	1/6	10 bits
6	10 bits	2/8 subsampling	3 binning	3 pixels	1/3	10 bits

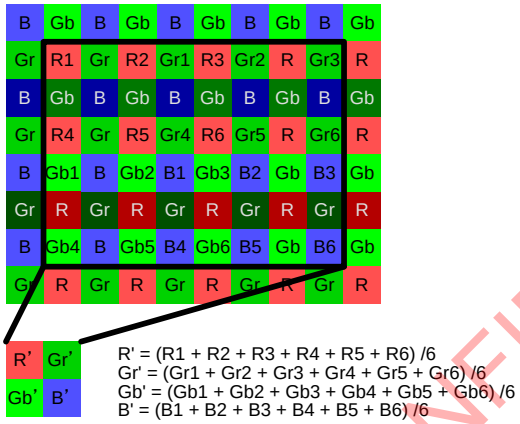
[*1] A/D conversion is performed with a resolution 4 times that of 10-bit A/D conversion, and the results are output in 12 bits regarded as a 10-bit integer item and a 2-bit decimal item.
[*2] Division is performed by internal arithmetic processing, then the results are output in 12 bits with the integer item in the upper 10 bits and the decimal item in the lower 2 bits.
[*3] See “Binning Image” for details of weighted binning in the following figures.



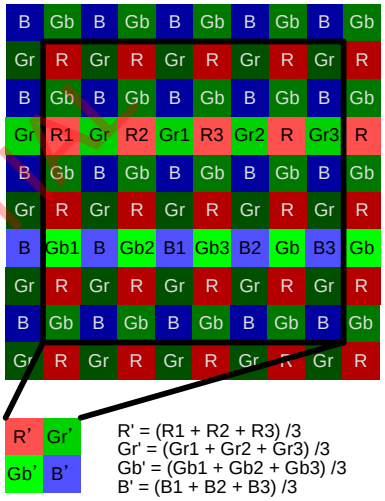
Horizontal/Vertical 2/2-line Binning
(Horizontal and vertical weighted binning)
Binning Image



Horizontal/Vertical 2/2-line Binning
(no weighted binning)
Binning Image



Vertical 2/3 Subsampling Binning
Horizontal 3 Binning
Binning Image



Vertical 2/8 Subsampling
Horizontal 3 Binning
Binning Image

Note) White letters in the diagram indicate pixels which are not read out.

Image Data Output Format When Using CSI-2

Frame Format (CSI-2)

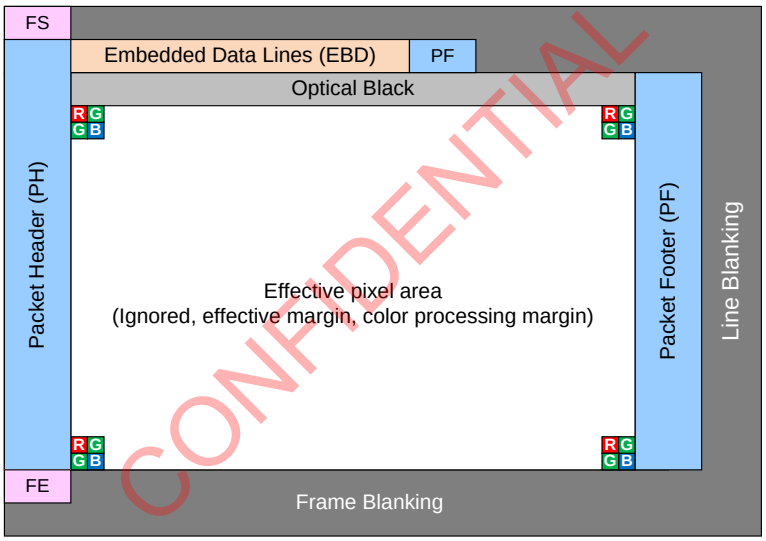
Each line of each image frame is output like the General Frame Format to CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Description
00h	Frame Start Code	FS
01h	Frame End Code	FE
12h	Embedded Data	Embedded data
2Bh	RAW10	When output data bit length is 10-bits
2Ch	RAW12	When output data bit length is 12-bits
37h	Optical Black Data	Vertical Optical Black line data

Frame Structure (CSI-2)

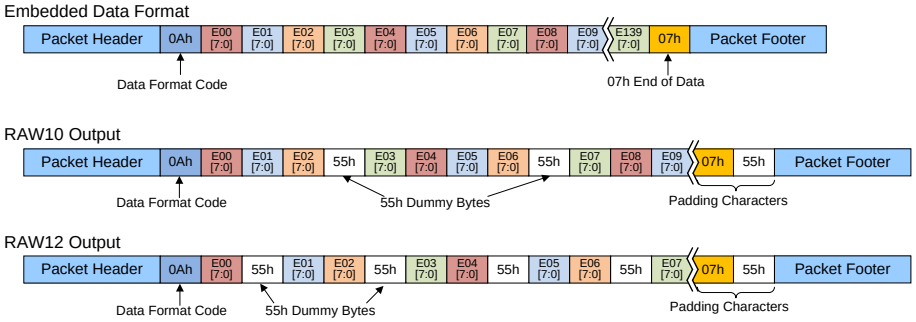
The figure below shows the image frame structure.



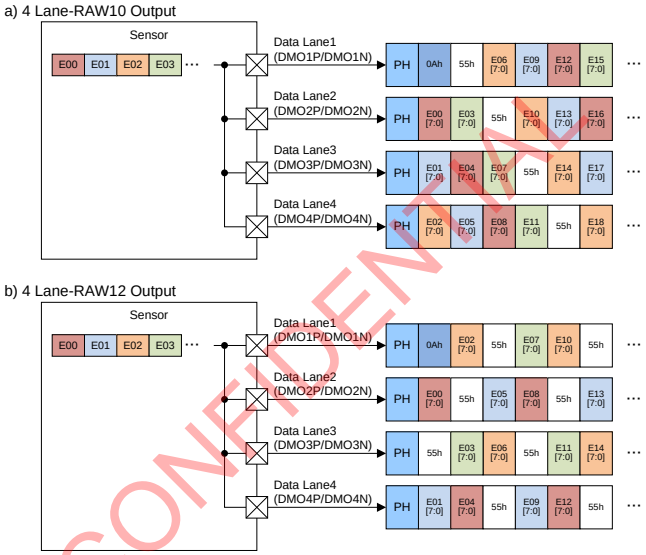
Frame Structure (CSI-2)

Embedded Data Line (CSI-2)

The Embedded data line is output in a line following the sync code FS.
In RAW10 mode, 55h dummy bytes are inserted after outputting 4 bytes of data each.
In RAW12 mode, 55h dummy bytes are inserted after outputting 2 bytes of data each.



The each format of 4 Lane is shown below.



Output Format of Embedded 4 Lane (CSI-2)

Specific Output (CSI-2)

Output timing	bit	Transfer data	Description
E00 to E05	[7:0]	—	(Ignored)
E06	[0]	SMD	
	[7:1]	—	(Ignored)
E07	[7:0]	PGC	
E08	[2:0]		
	[7:3]	—	(Ignored)
E09	[7:0]	SHR	
E10	[7:0]		
E11	[7:0]	SVR	
E12	[7:0]		
E13 to E14	[7:0]	—	(Ignored)
E15	[3:0]	DGAIN	
	[4]	MDVREV	
	[7:5]	—	(Ignored)

Output timing	bit	Transfer data	Description
E16	[7:0]	BLKLEVEL	
E17 to E24	[7:0]	—	(Ignored)
E25	[0]	HTRIMMING_EN	
	[7:1]	—	(Ignored)
E26	[7:0]	HTRIMMING_START	
E27	[4:0]		
	[7:5]	—	(Ignored)
E28	[7:0]	HTRIMMING_END	
E29	[4:0]		
	[7:5]	—	(Ignored)
E30	[0]	VWIDCUTEN	
	[7:1]	—	(Ignored)
E31	[7:0]	VWINPOS	
E32	[3:0]		
	[7:4]	—	(Ignored)
E33	[7:0]	VWIDCUT	
E34	[2:0]		
	[7:3]	—	(Ignored)
E35 to E139	[7:0]	—	(Ignored)

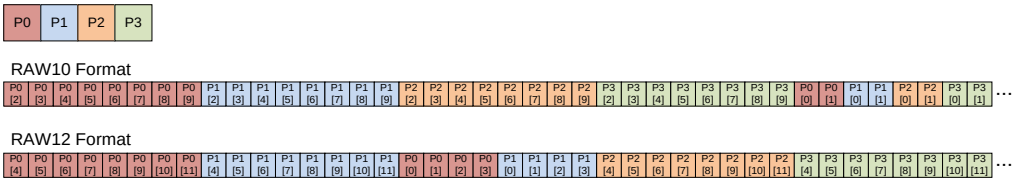
CSI-2 serial Output Setting (CSI-2)

The output formats of this sensor support the following modes.

CSI-2 serial data output 4 Lane, RAW10 and RAW12

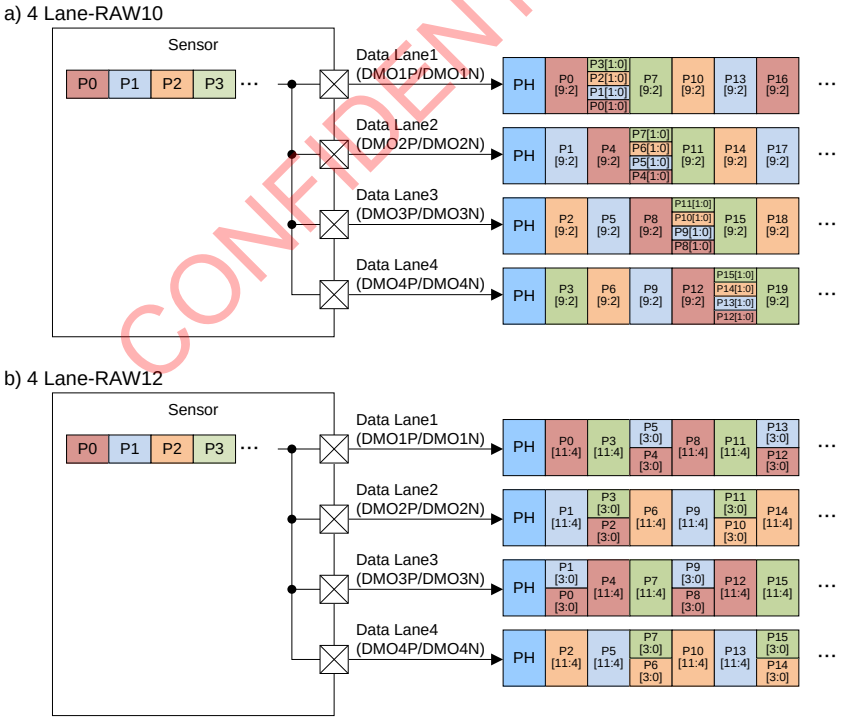
The image data is output from the CSI-2 output pin. The DMO1P/DMO1N are called the Lane1 data signal, the DMO2P/DMO2N are called the Lane2 data signal, the DMO3P/DMO3N are called the Lane3 data signal and the DMO4P/DMO4N are called the Lane4 data signal. In addition, the clock signals are output from DMCKP/DMCKN of the CSI-2 pins.
In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The bit rate maximum value is 1.440 Gbps/Lane.

The formats of RAW10 and RAW12 are shown below.



Example of formats of RAW10 and RAW12

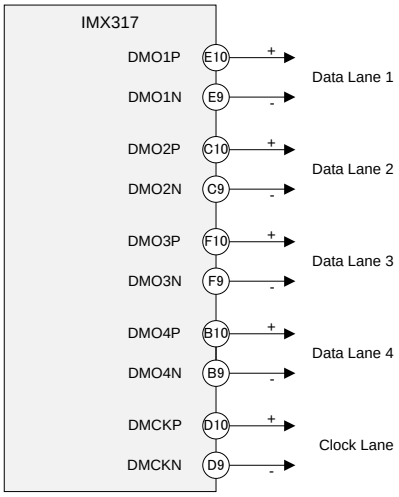
The each format of 4 Lane are shown below.



Output Format of 4 Lane (CSI-2)

MIPI Transmitter (CSI-2)

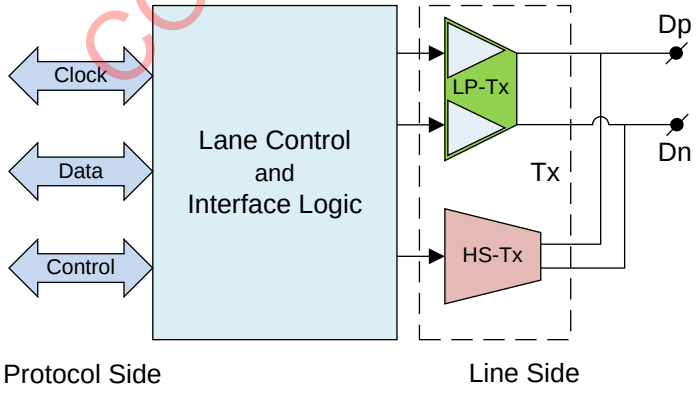
Output pins (DMO1P to DMO4P, DMO1N to DMO4N, DMCKP, DMCKN) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1
・MIPI Alliance Specification for D-PHY Version 1.1

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver.
The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1.440Gbps/Lane.



Universal Lane Module Functions

Detailed Specification of Each Mode (CSI-2)

1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Horizontal Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Horizontal operation period (Number of pixels conversion)						HMAX register minimum value
	Front ignored area	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	0	0	12	3840	12	0	493
1	0	0	12	3840	12	0	263
2	0	0	6	1920	6	0	493
3	0	0	6	1920	6	0	260
4	0	0	6	1920	6	0	260
5	0	0	4	1280	4	0	260
6	0	0	4	1280	4	0	260

Vertical Operation Period in Each Readout Drive Mode (CSI-2)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)						Min VBLK *3	VMAX register minimum value
	Front OB	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel		
0	16	6	18	2160	18	0	13	4451
1	16	6	4	2160	4	0	13	4379
2	8	6	4	1080	4	0	13	2219
3	8	6	4	1080	4	0	13	2219
4	8	6	4	1080	4	0	13	2219
5	4	6	4	720	4	0	13	1491
6	4	2	2	540	2	0	9	1111

*1 When vertical direction normal readout.
*2 When vertical direction inverted readout.
*3 Unit: HMAX ×72MHz clock. It includes FS and FE line. When VMAX is set to a nearby minimum value, set the value not to be less than the necessary VBLK value for DSP (Normally 10 to 20 lines is needed).

2. Frame Rate Adjustment (CSI-2)

The formula for frame rate calculation is shown below.

Frame rate [frame/s] = (72×10^6) / {HMAX register value × VMAX register value × (SVR register value + 1) }

The frame rate can be changed by changing HMAX and VMAX register values as long as these are set to minimum value or larger. HMAX changes the line blanking period. VMAX changes the frame blanking period.
The examples of setting for each readout drive mode are shown in the table below. Set HMAX and VMAX considering ISP image processing time.
The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See “Electronic Shutter Timing” for details.

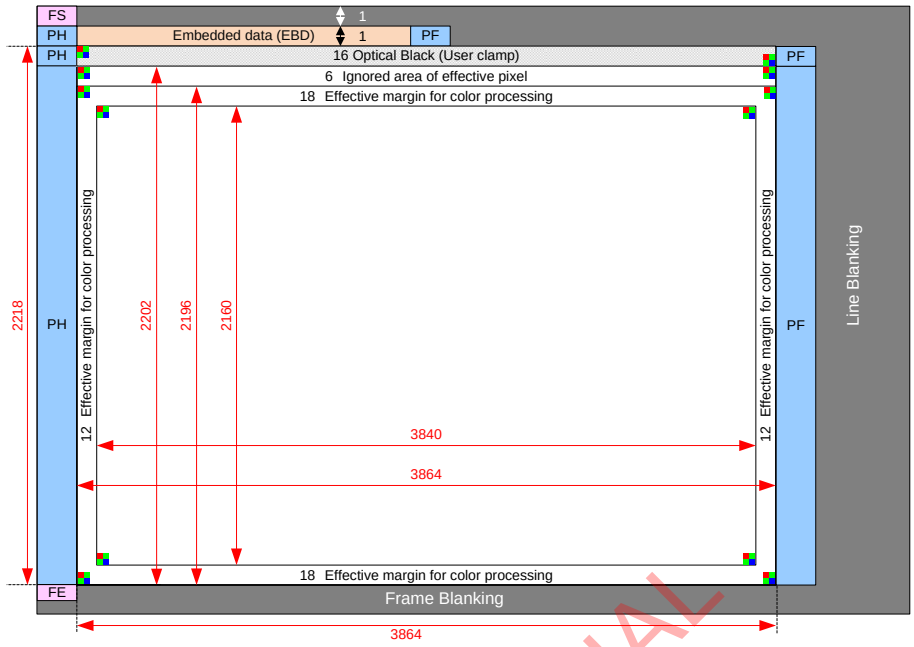
Examples of HMAX, VMAX and Frame Rate (CSI-2)

Readout mode No.	HMAX*1 min value	VMAX*2 min value	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				HMAX*1 [dec]	VMAX*2 [dec]	SVR	Frame frequency [frame/s]	HMAX*1 [dec]	VMAX*2 [dec]	SVR	Frame frequency [frame/s]
0	493	4451	32.81	493	4872	0	29.98*3	500	5760	0	25.00
1	263	4379	62.52	263	4550	0	60.17*3	288	5000	0	50.00
2	493	2219	65.82	493	2436	0	59.95*3	500	2880	0	50.00
3	260	2219	124.80	260	2310	0	119.88	288	2500	0	100.00
4	260	2219	124.80	260	2310	3	29.97	288	2500	3	25.00
5	260	1491	185.73	260	2310	0	119.88	288	2500	0	100.00
5 (60fps)				260	2310	1	59.94	288	2500	1	50.00
6	260	1111	249.26	260	1154	0	239.97	288	1250	0	200.00
6 (30fps)				260	1154	7	29.97	288	1250	7	25.00

*1 The value set as HMAX (address 30F6h, bit [7:0] and address 30F7h, bit [7:0]).
*2 The value set as VMAX (address 30F8h, bit [7:0], address 30F9h, bit [7:0] and address 30FAh, bit [3:0]).
*3 This frame rate is not compatible for NTSC

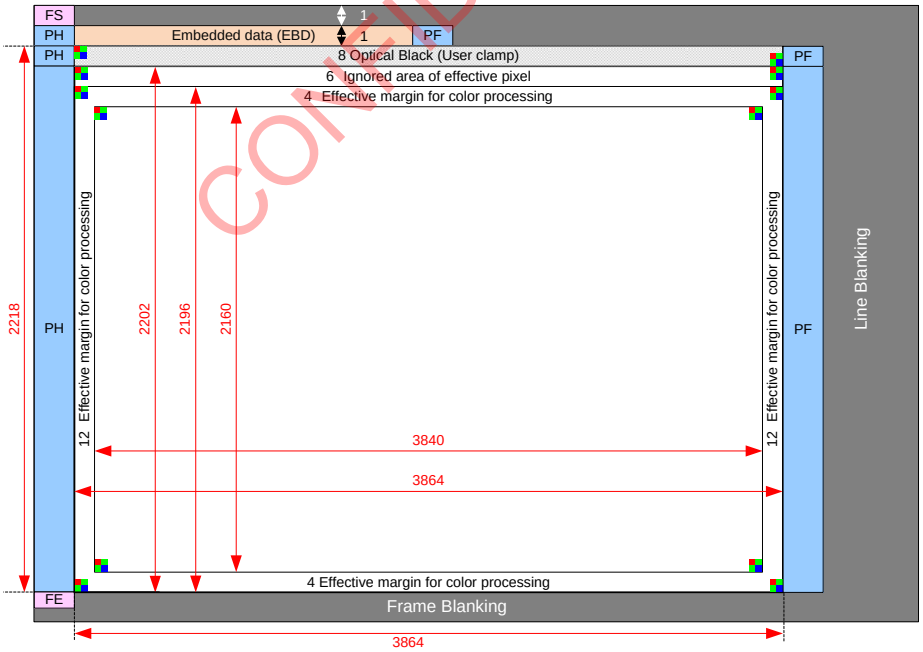
3. Image Data Output Format (CSI-2)

(CSI-2) MODE0: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)



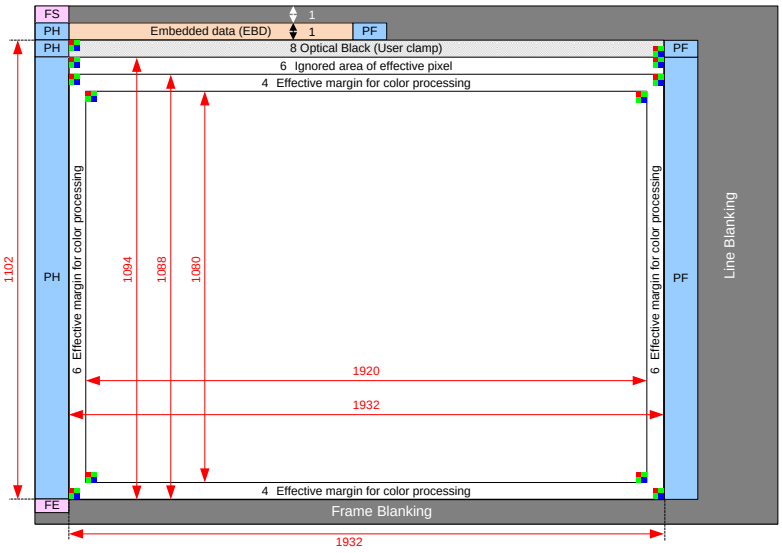
Readout Pixel Image Diagram (3840 × 2160)

(CSI-2) MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)



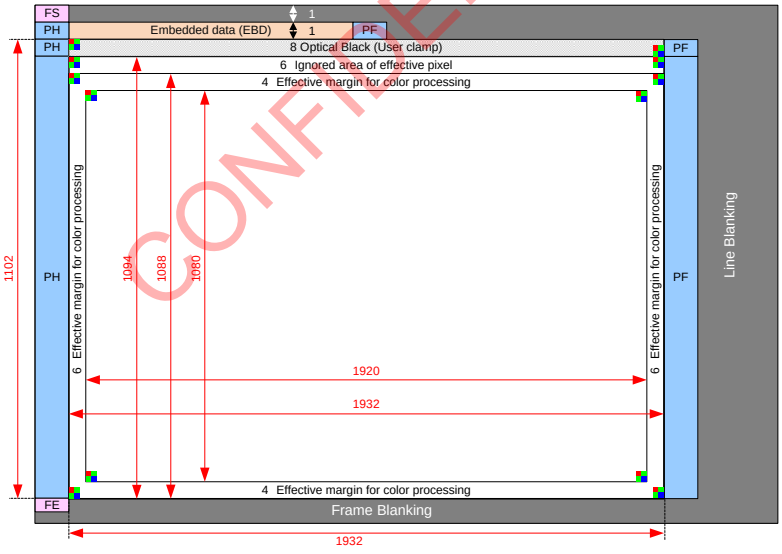
Readout Pixel Image Diagram (3840 × 2160)

(CSI-2) MODE2: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(12-bit A/D conversion, 12-bit length output)



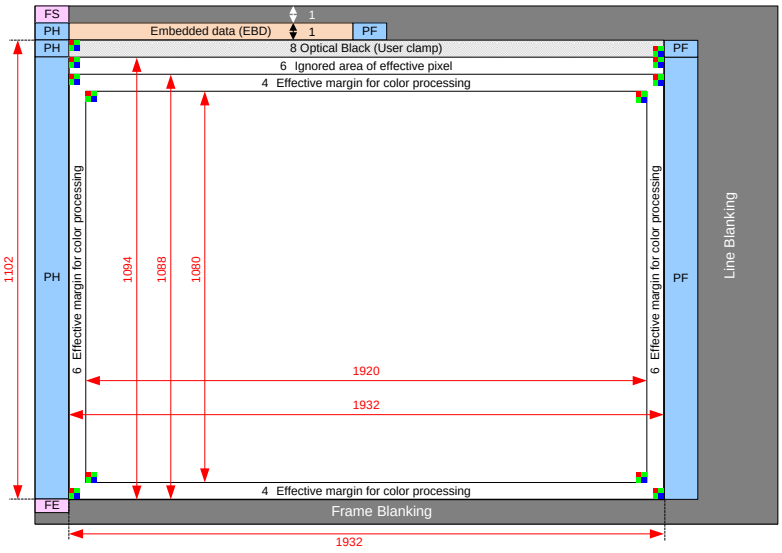
Readout Pixel Image Diagram (1920 × 1080)

(CSI-2) MODE3: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(10-bit A/D conversion, 10-bit length output)



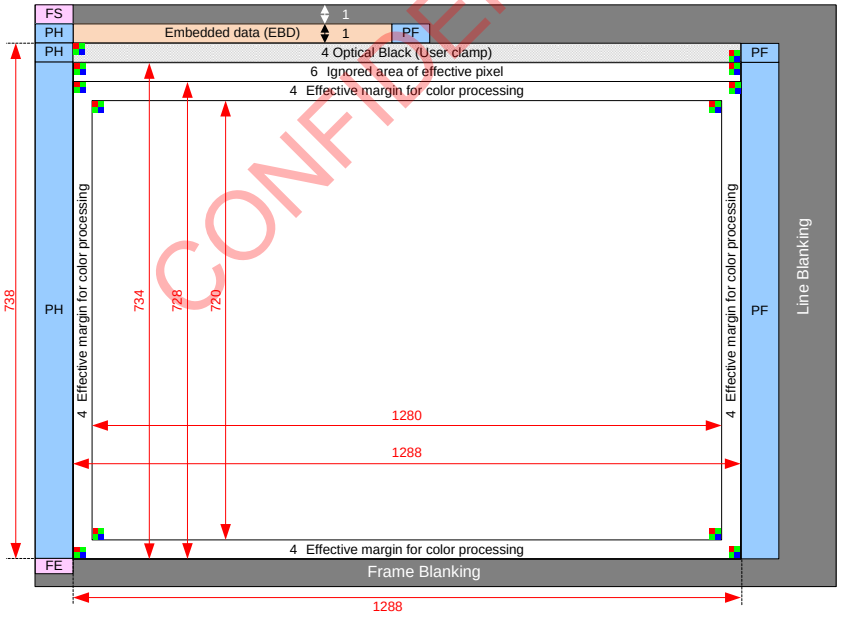
Readout Pixel Image Diagram (1920 × 1080)

(CSI-2) MODE4: Horizontal/vertical 2/2-line binning low power consumption drive (10-bit A/D conversion, 10-bit length output)



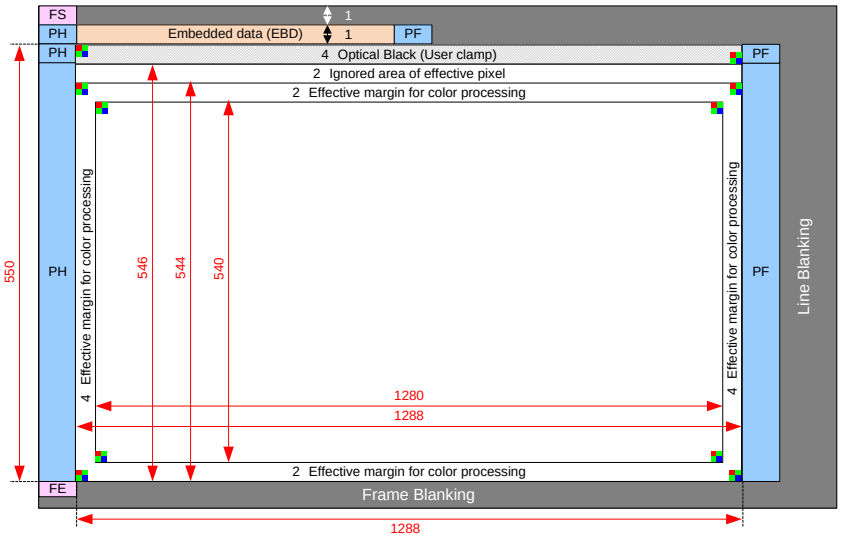
Readout Pixel Image Diagram (1920 × 1080)

(CSI-2) MODE5: Vertical 2/3 subsampling binning horizontal 3 binning (10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (1280 × 720)

(CSI-2) MODE6: Vertical 2/8 subsampling horizontal 3 binning
(10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (1280 × 540)

Vertical Arbitrary Cropping Function (CSI-2)

Vertical cropping region of this sensor can be arbitrarily changed by registers.

TBD

Horizontal Arbitrary Cropping Function (CSI-2)

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

TBD

Electronic Shutter Timing When Using CSI-2

1. SHR, SVR, SMD Setting When Using CSI-2

1-1. SHR, SVR Setting (CSI-2)

The exposure start timing can be designated by setting the electronic shutter timing register SHR.
Note that this setting value unit is 1[HMAX][*1] period regardless of the readout drive mode.
In addition, 1 frame period can be extended at VMAX period unit according to the SVR register.
(1 frame cycle is (SVR value + 1) times as long as VMAX period.)

[*1] Setting value of register HMAX × 72MHz clock

Shutter Control Register (CSI-2)

Name	CSI-2 Address	Bit	Function
SHR [7:0]	300Ch	[7:0]	Specifies the integration start horizontal period
SHR [15:8]	300Dh	[7:0]	
SVR [7:0]	300Eh	[7:0]	Specifies the integration shutdown vertical period
SVR [15:8]	300Fh	[7:0]	
HMAX [7:0]	30F6h	[7:0]	Horizontal drive period length
HMAX [15:8]	30F7h	[7:0]	
VMAX [7:0]	30F8h	[7:0]	Vertical drive period length
VMAX [15:8]	30F9h	[7:0]	
VMAX [19:16]	30FAh	[3:0]	

Shutter Setting (CSI-2)

Register	Register Value		Function
SHR	12 to {(SVR value + 1) × VMAX value – 4}	Readout mode No.0, 1 All-pixel scan mode (12 bits) All-pixel scan mode (10 bits)	Specifies the integration start horizontal period
	8 to {(SVR value + 1) × VMAX value – 4}	Readout mode No.2, 3, 4 Horizontal/vertical 2/2-line binning mode (horizontal and vertical weighted binning) 12 bits, 10 bits, Low power consumption drive	
	8 to {(SVR value + 1) × VMAX value − 4}	Readout mode No.5 Vertical 2/3 subsampling binning horizontal 3 binning mode	
	4 to {(SVR value + 1) × VMAX value − 2}	Readout mode No.6 Vertical 2/8 subsampling horizontal 3 binning mode	
	0 to {(SVR value + 1) × VMAX value − 130}	Global reset shutter mode (SMD = 1) (12 bits)	
	0 to {(SVR value + 1) × VMAX value − 130}	Global reset shutter mode (SMD = 1) (10 bits)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

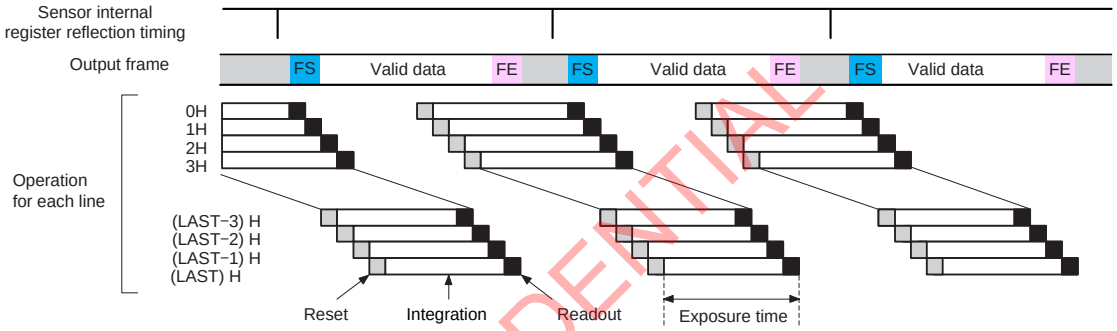
Note)
1. See ”Integration Time in Each Readout Drive Mode” on page TBD for the integration time calculation formula.
2. The SVR register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 3008h, bit [0]).

1-2. Electronic Shutter Drive Mode (CSI-2)

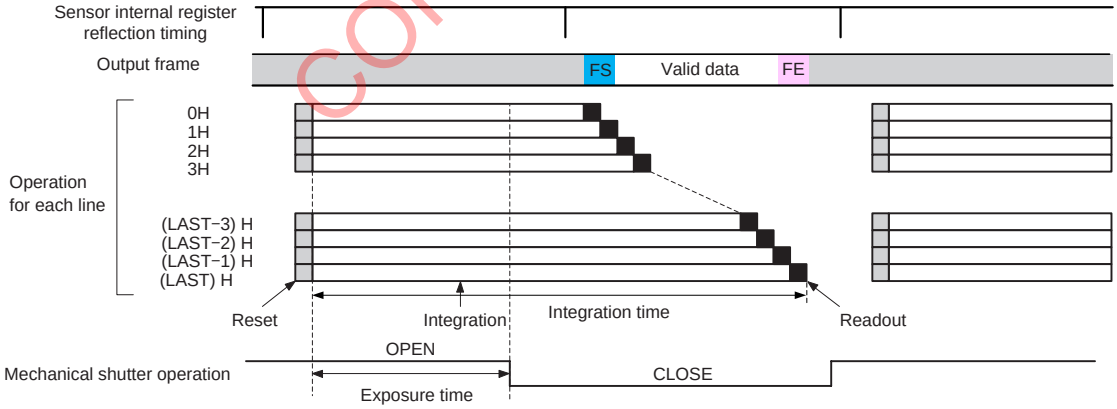
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD. Rolling shutter operation performs pixel reset and integration sequentially in line units. Global reset shutter operation resets all pixels at once and then starts integration after that.
("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.)
The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.
Using XVS output sync signal from sensor as trigger signal is recommended in the case of synchronizing global reset shutter timing of sensor and mechanical shutter timing outside of sensor is needed for fine adjustment of integration time.
Consult your Sony sales representative concerning to use XVS output signal.

SMD Setting

Name	CSI-2 Address	Bit	Register value	Function
SMD	3008h	[0]	0h	Rolling shutter (normal shutter mode)
			1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

2. Integration Time in Each Readout Drive Mode and Mode Changes When Using CSI-2

2-1. Integration Time in Each Readout Drive Mode (CSI-2)

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR and SVR. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

◆Integration time of normal readout drive mode

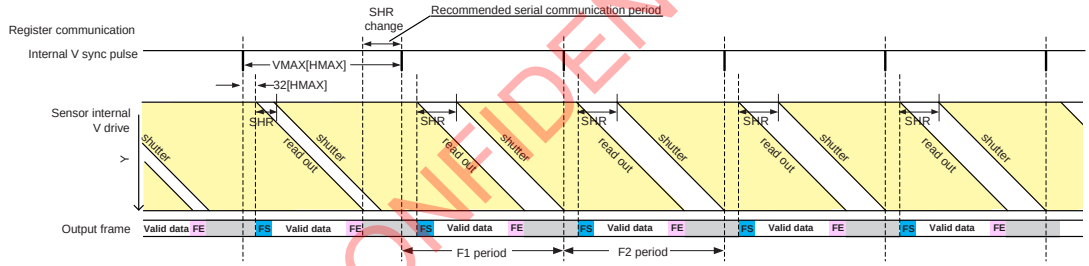
Integration Time [s] = [{VMAX value × (SVR value + 1) – SHR value}
× HMAX value + Number of clocks per internal offset period] / (72 x 10^6)

* See the following tables for the numbers of clocks per internal offset period.
* See “Electronic Shutter Timing” on page TBD of the SHR register setting range.

Number of clocks per internal offset period (TENTATVE)

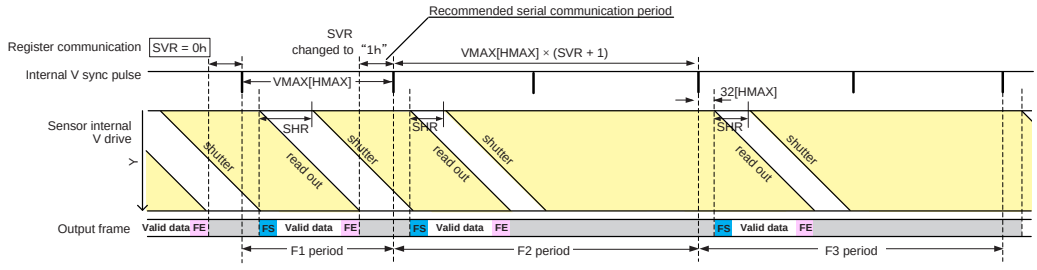
Readout mode No.	0	1	2	3	4	5	6
Number of clocks per internal offset period	169	112	112	112	112	112	112

The figure below shows operation when SHR is being changed and REGHOLD is 0h. The F1 and F2 periods in the figure below are two continuous frames. The SHR value which is set in the recommended serial communication period[*1] just before F1 period is updated internally at the end of the communication period and then output data which reflect the new setting is output in the F2 period. Note that the SHR setting and output are offset by a frame.
[*1] Refer to "Register Communication Timing".



SHR Change Sequence (CSI-2)

The internal vertical drive period which is set by the VMAX register can be subsampled by the SVR register. Its period is (SVR value + 1) times as long as VMAX period. Therefore the frame rate is multiplied by 1/ (SVR value + 1).
The figure below shows the operation when the SVR register is being changed from “0h” to “1h” and REGHOLD is 0h. The SVR value, which is set in the recommended serial communication period[*1] just before F2 period, is updated internally at the end of the communication period and then applied from the shutter operation in the F2 period. The output data which reflect the changing of SVR is output in the F3 period.
The image data of the F1 period before the SVR value is changed is output as valid data in the F2 period.
[*1] Refer to "Register Communication Timing".



SVR Change Sequence (CSI-2)

2-2. Operation when Changing the Readout Drive Mode (CSI-2)

When changing input INCK or CSI-2 output frequency, follow the below procedure.

1st step: Enter the sensor standby mode
2nd step: Change the frequency during standby mode.
3rd step: Follow the standby cancel sequence to resume the normal operation.

When changing input INCK frequency, don't input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low. Then set the state of XCLR to High, following the item of "Power on sequence" in the section of "Power on / off sequence" in page 88. Execute “Standby Cancel Sequence” again because the register settings become default state after system reset.

The following mode change cases are treated as a mode transition on this sensor and one frame of invalid data is generated.

1. Changing the readout mode setting
2. Changing the vertical direction readout setting
3. Changing the vertical arbitrary cropping setting

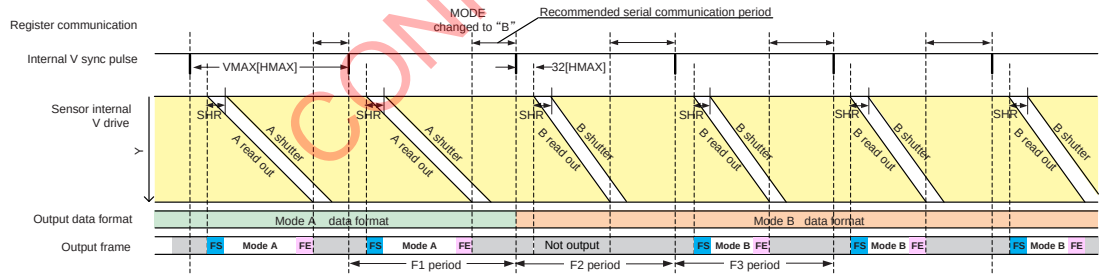
* Changing the horizontal arbitrary cropping setting is not treated as mode transition and no invalid data is generated.

The figure below shows the mode transition sequence, Mode A to Mode B, in case that the mode transition is performed in three continuous frames, F1 to F3, and REGHOLD is 0h.

(1) Set the register setting for Mode B in the recommended serial communication period[*1] just before F2 period. The F2 period data is not output.
(2) Valid data which reflect the new setting is output from the next frame (F3 period).

[*1] Refer to "Register Communication Timing"

In addition, note that when the output data length differs between Mode A and Mode B, the new data format is output from the start of F2 period in which the setting is changed to Mode B.

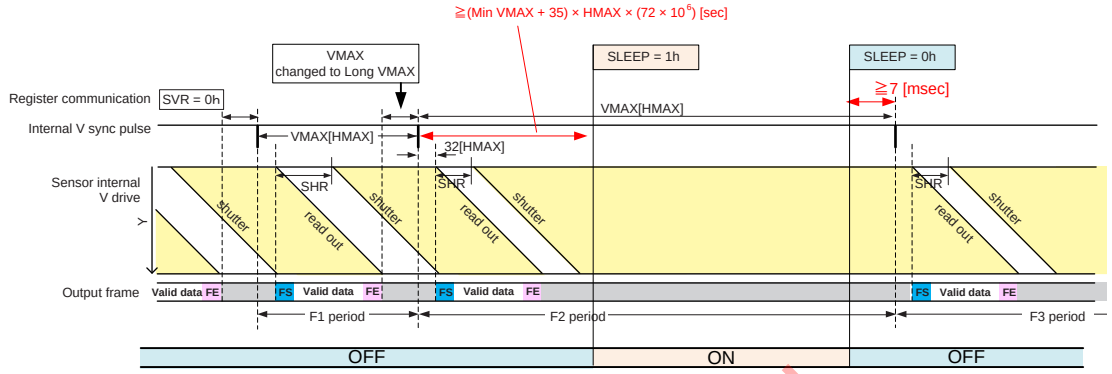


Mode Transition (CSI-2)

2-3. Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation (CSI-2)

To extend the integration time, VMAX register is available other than SVR register. VMAX register extends V period. SLEEP register can reduce power consumption during integration time when using large VMAX. To change to low power consumption drive, set SLEEP register to 1h after (VMAX value + 35) × HMAX value × (72 x 10^6) [sec] or more in the frame of changing the register SMD from 0h to 1h.
And for readout, set SLEEP to 0h before 7 ms of readout frame in order to cancel low power consumption mode.

When using SVR ≥ 1h, this sequence is not necessary.

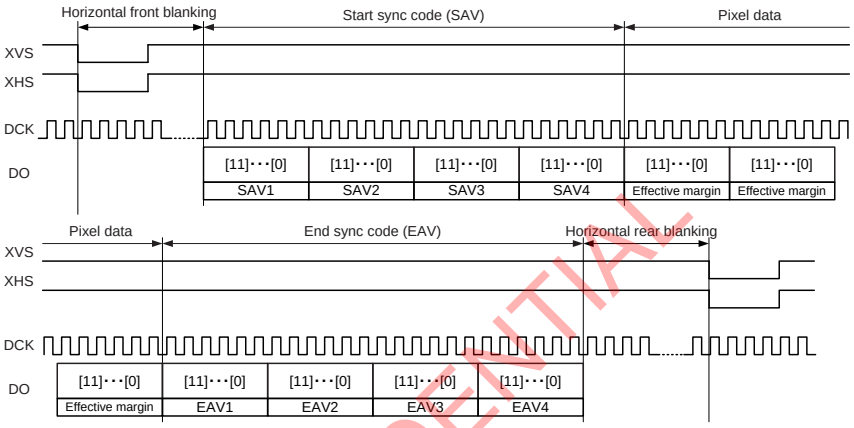


Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation (CSI-2)

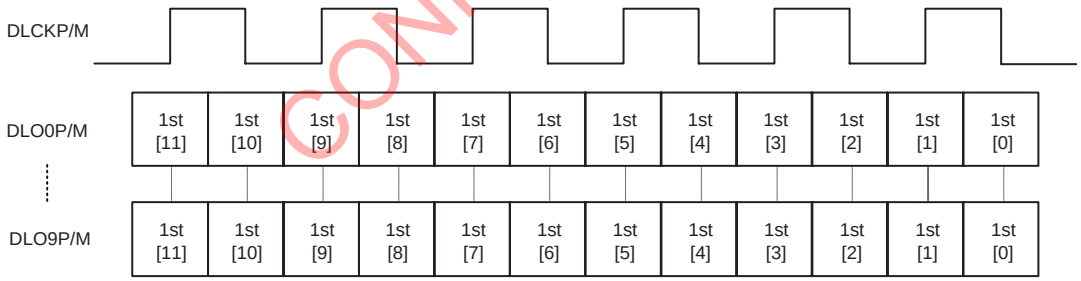
Image Data Output Format When Using Sub-LVDS

1. Sync Signals and Data Output Timing (Sub-LVDS)

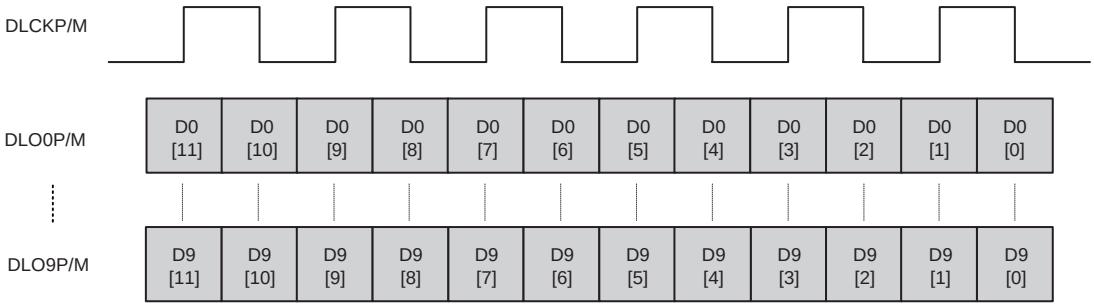
The figure below shows the sync signal and data output timing during 12-bit length serial output for this sensor.
The horizontal and vertical timing of the output data are controlled by the XVS and XHS sync signals. Timing control is performed at the falling edge of both the XVS and XHS signals. The data is output in order from the start sync code (SAV) after the horizontal front blanking period after the falling edge.
See “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages TBD for the detailed blanking length and number of OB pixels. The length of horizontal front blanking pixels varies greatly according to the mode as described in “Minimum Horizontal Operation Period in Each Readout Drive Mode” on pages TBD, so using the sync code as the trigger is recommended for the recording pixel start timing.
The sync code details are shown below.
In addition, the length of horizontal rear blanking changes when the XHS period is changed.



Sync Signal and Data Output Timing



Serial Data Details (Sync Code Block)



Serial Data Details (Pixel Data Block)

Sync code details

LVDS output bit No.		Sync code (4 words)				
12-bit output	10-bit output	1st word	2nd word	3rd word	4th word	
11	9	1	0	0	1	
10	8	1	0	0	0	
9	7	1	0	0	V	1: Blanking line 0: Except blanking line
8	6	1	0	0	H	1: End sync code 0: Start sync code
7	5	1	0	0	P3	Protection bits
6	4	1	0	0	P2	
5	3	1	0	0	P1	
4	2	1	0	0	P0	
3	1	1	0	0	0	
2	0	1	0	0	0	
1	—	1	0	0	0	
0	—	1	0	0	0	

		Protection bits			
V	H	P3	P2	P1	P0
0	0	0	0	0	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

Sync code details (hexadecimal notation) 12-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	FFFh	000h	000h	AB0h
	End sync code (EAV)				B60h
Except blanking line	Start sync code (SAV)				800h
	End sync code (EAV)				9D0h

Sync code details (hexadecimal notation) 10-bit output

		1st word	2nd word	3rd word	4th word
Blanking line	Start sync code (SAV)	3FFh	000h	000h	2ACh
	End sync code (EAV)				2D8h
Except blanking line	Start sync code (SAV)				200h
	End sync code (EAV)				274h

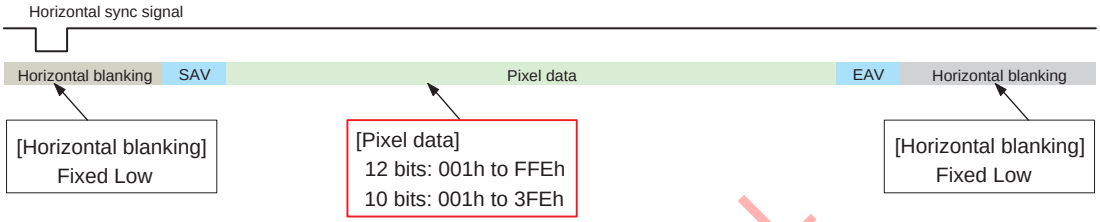
2. Output Range of LVDS Output Data (Sub-LVDS)

The table below shows the decimal point position, output bit length and output range of the output data in each readout mode. Note that the value of the first word of the sync code (3FFh, FFFh) and the maximum data value do not overlap in any readout mode.

Data output range in each readout mode

Readout mode No.	LVDS output		
	Decimal point position	Output bit length [bit]	Output range [hex]
0	2	12	001h to FFEh
1 to 6	0	10	001h to 3FEh

Output value during horizontal blanking period is fixed to Low (all 0).



Readout Drive Timing

Detailed Specification of Each Mode (Sub-LVDS)

1. Horizontal/Vertical Operation Period in Each Readout Drive Mode (Sub-LVDS)

Horizontal Operation Period in Each Readout Drive Mode (Sub-LVDS)

Readout mode No.	Data rate [MHz]	Horizontal blanking period [DCK]*2*3	Horizontal operation period (Number of pixels conversion)						XHS minimum period [INCK]*2*4
			Front OB	Front ignored area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	576 (288DDR*1)	399 to 405	0	0	12	3840	12	0	493
1		374 to 380	0	0	12	3840	12	0	260
2		399 to 405	0	0	6	1920	6	0	493
3		374 to 380	0	0	6	1920	6	0	260
4		374 to 380	0	0	6	1920	6	0	260
5		374 to 380	0	0	4	1280	4	0	260
6		374 to 380	0	0	4	1280	4	0	260

*1 DDR: Double Data Rate
*2 If XHS period is shorter than the (XHS minimum period + horizontal front blanking), the data from the previous line may be output during the horizontal front blanking period.
*3 Number of LVDS output signal DCK clock
*4 Number of clocks in conversion of INCK = 72 MHz.

Vertical Operation Period in Each Readout Drive Mode (Sub-LVDS)

Readout mode No.	Number of lines per vertical operation period (output data 1H conversion)							XVS minimum period [XHS]
	Vertical front blanking	Front OB (User Clamp)	Front ignore area of effective pixel	Front effective margin for color processing	Recommended recording pixels	Rear effective margin for color processing	Rear ignored area of effective pixel	
0	26	16	6	18	2160	18	0	4462
1	26	16	6	18	2160	18	0	4462
2	22	8	6	4	1080	4	0	2226
3	22	8	6	4	1080	4	0	2226
4	22	8	6	4	1080	4	0	2226
5	22	4	6	4	720	4	0	1498
6	18	4	2	2	540	2	0	1118

2. Frame Rate Adjustment (Sub-LVDS)

The formula for frame rate calculation is shown below.

Frame rate [frame/s] = (72 x 10^6) / { XHS period [INCK] × XVS period [XHS] × (SVR register value + 1) }

The frame rate can be changed by changing XHS period and XVS period as long as these are set to minimum value or larger. Larger XHS period results in longer horizontal blanking period. Larger XVS period results in longer vertical blanking period. The examples of setting for each readout drive mode are shown in the table below. Set XHS period and XVS period considering ISP image processing time.
The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. When using SVR = 1h, the frame rate becomes half. See “Electronic Shutter Timing” for details.

H Period and Number of XHS Pulses, V Period and XVS Pulses (Sub-LVDS)

Readout mode No.	H period (number of XHS pulses) *1	V period (number of XVS pulses) *2
0	2	1
1	2	1
2	2	1
3	2	1
4	2	4 (SVR = 3h)
5	2	1
6	2	1

*1 Number of XHS pulses required to output the data for one line
*2 Number of XVS pulses required to output the data for one frame

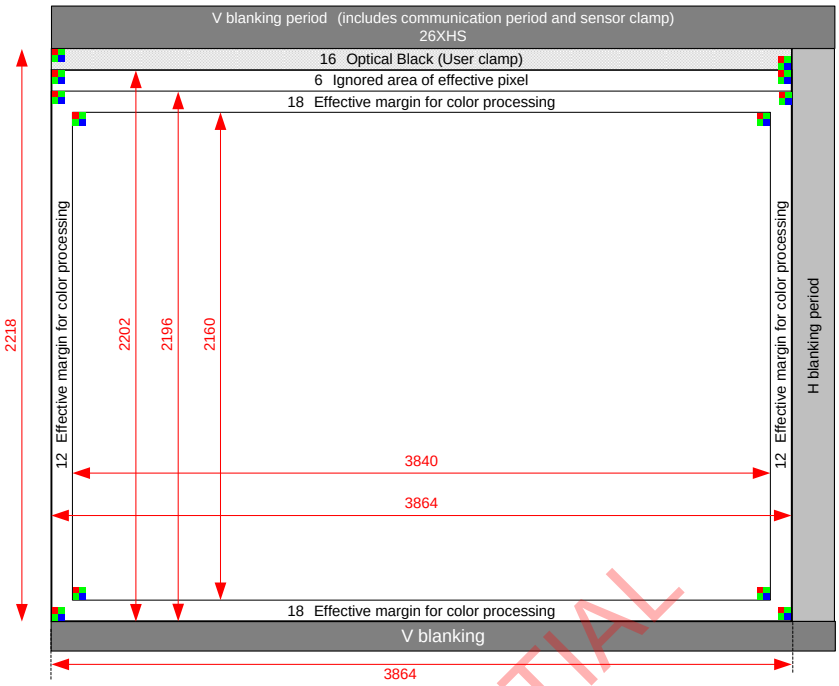
Examples of HMAX, VMAX and Frame Rate (Sub-LVDS)

Readout mode No.	XHS period (INCK) *1	XVS period (number of XHS pulses)	Max frame frequency [frame/s]	NTSC compatible drive				PAL compatible drive			
				XHS period (INCK) *1	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]	XHS period (INCK) *1	XVS period (number of XHS pulses)	SVR	Frame frequency [frame/s]
0	493	4462	32.73	528	4550	0	29.97	576	5000	0	25.00
1	260	4462	62.06	264	4550	0	59.94	288	5000	0	50.00
2	493	2226	65.61	520	2310	0	59.94	576	2500	0	50.00
3	260	2226	124.40	264	2275	0	119.88	288	2500	0	100.00
4	260	2226	124.40	264	2275	3	29.97	288	2500	3	25.00
5	260	1498	184.86	364	1650	0	119.88	375	1920	0	100.00
5 (60fps)				364	1650	1	59.94	375	1920	1	50.00
6	260	1118	247.70	260	1155	0	239.76	288	1250	0	200.00
6 (30fps)				260	1155	7	29.97	288	1250	7	25.00

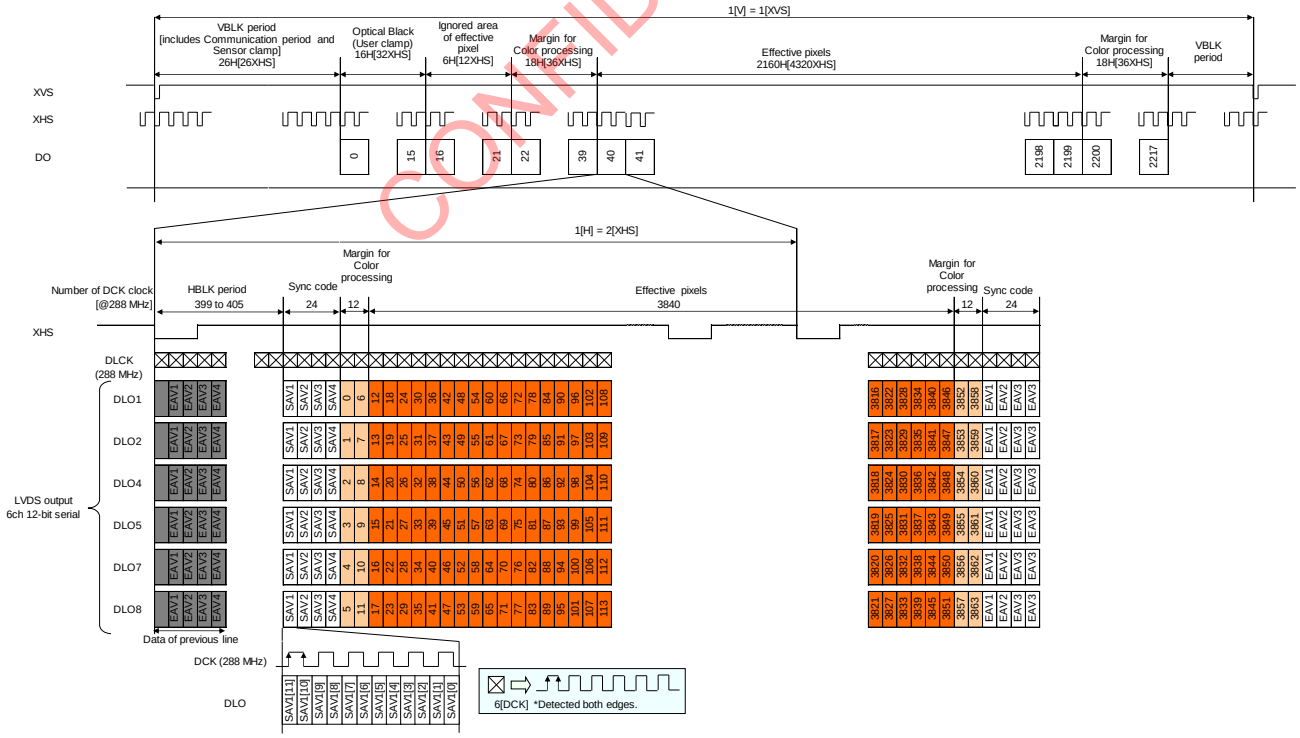
*1 Number of clocks in conversion of INCK = 72 MHz

3. Image Data Output Format (Sub-LVDS)

(Sub-LVDS) MODE0: All-pixel scan mode (12-bit A/D conversion, 12-bit length output)

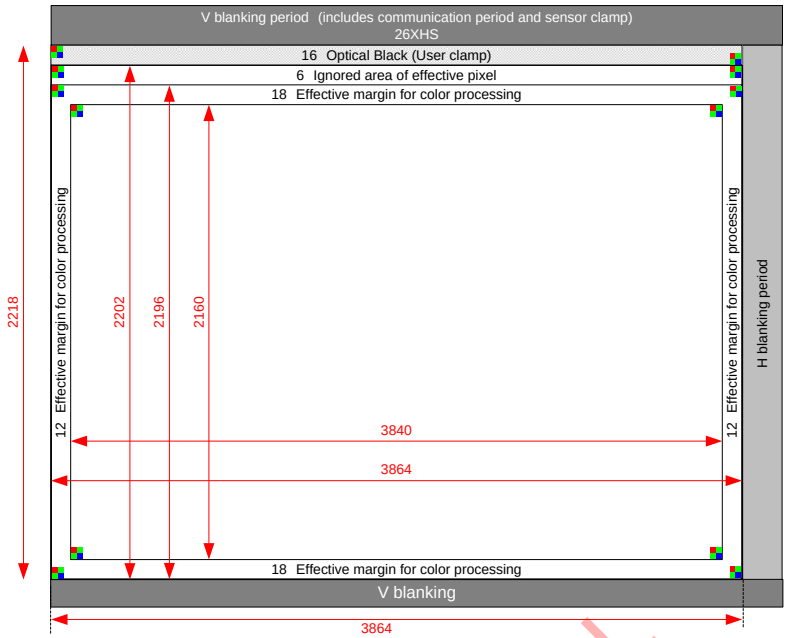


Readout Pixel Image Diagram (3840 × 2160)

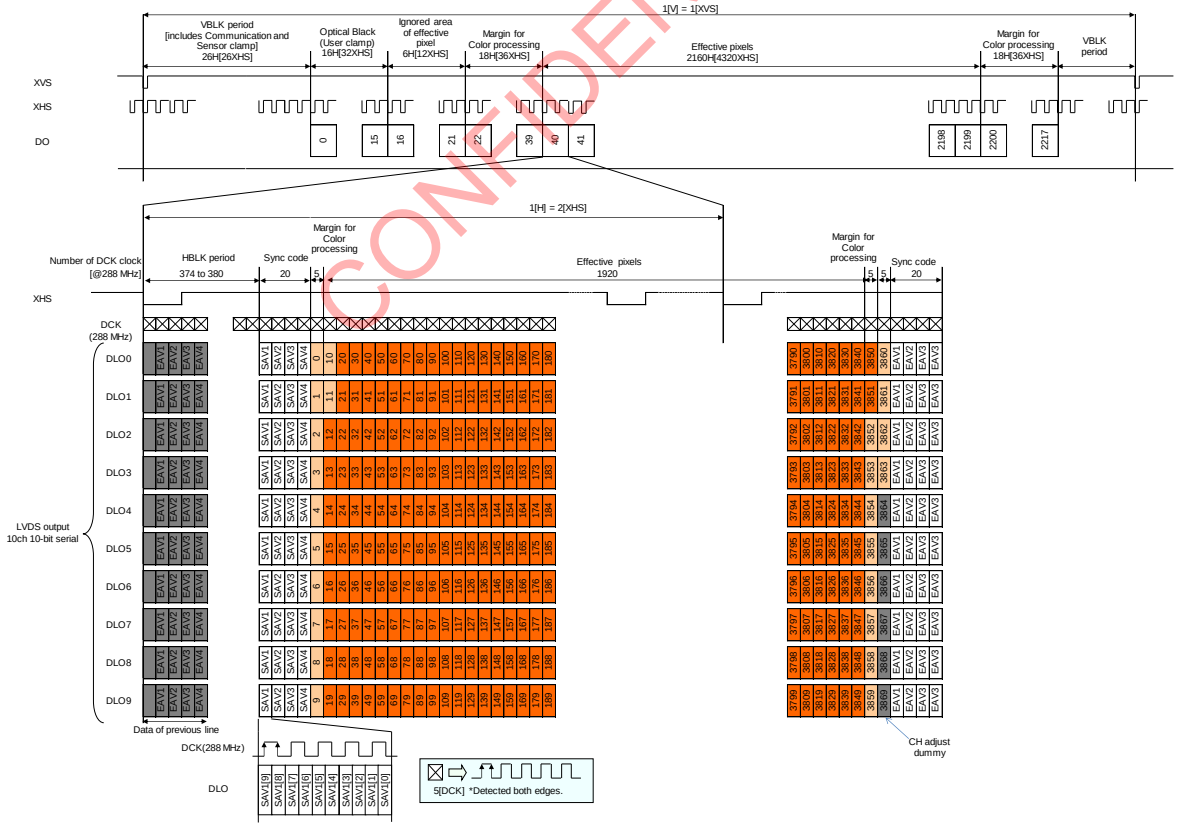


Readout Drive Timing

(Sub-LVDS) MODE1: All-pixel scan mode (10-bit A/D conversion, 10-bit length output)

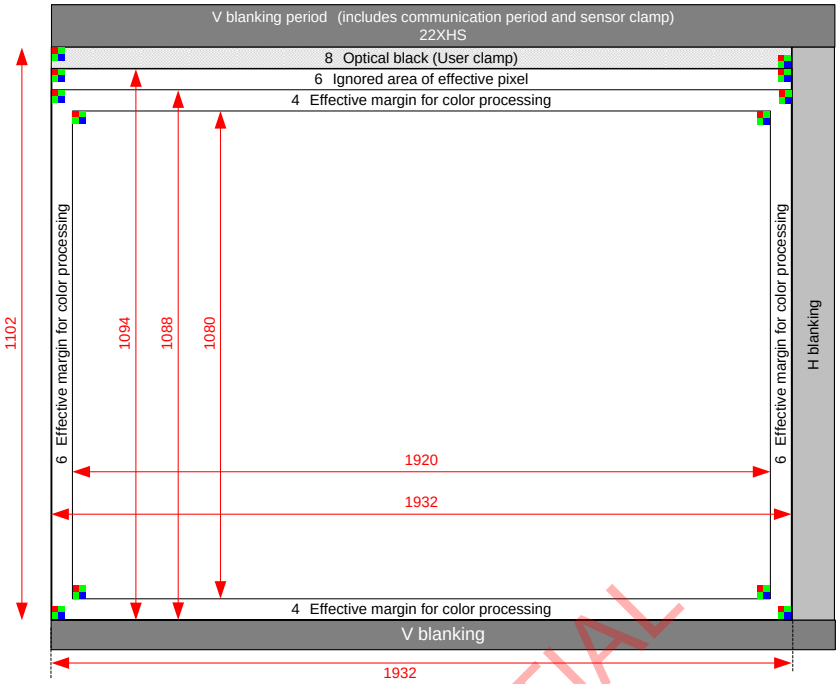


Readout Pixel Image Diagram (3840 × 2160)

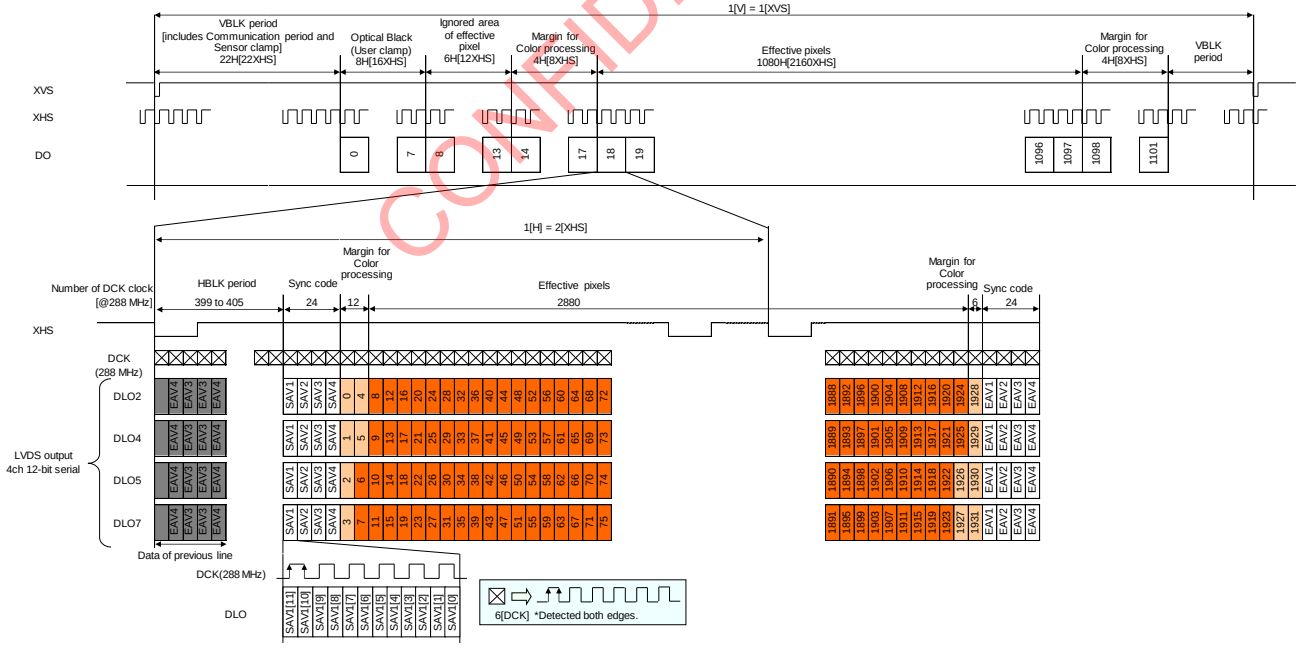


Readout Drive Timing

(Sub-LVDS) MODE2: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(12-bit A/D conversion, 12-bit length output)

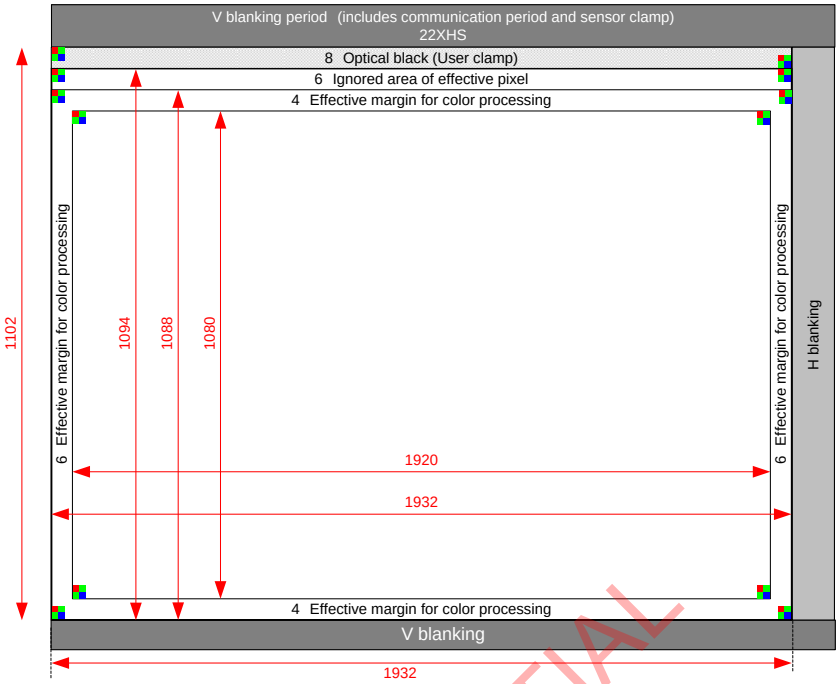


Readout Pixel Image Diagram (1920 × 1080)

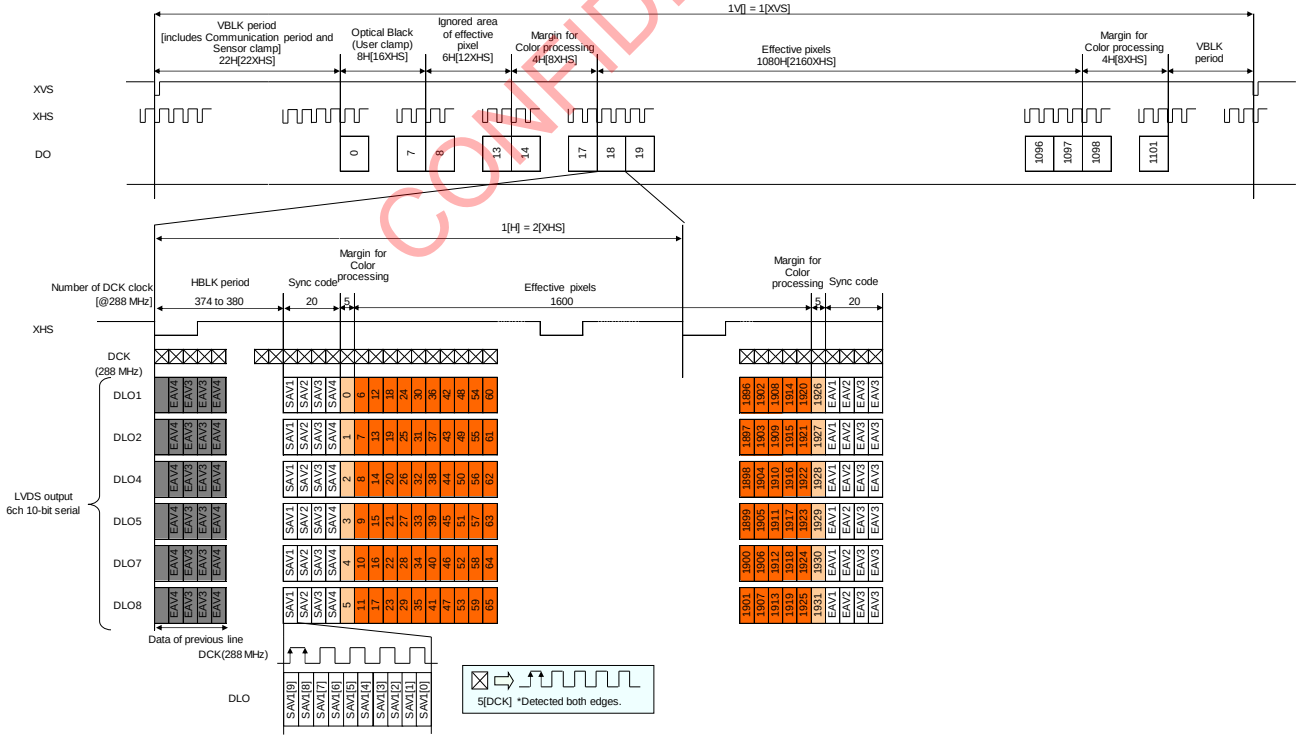


Readout Drive Timing

(Sub-LVDS) MODE3: Horizontal/vertical 2/2-line binning (horizontal and vertical weighted binning)
(10-bit A/D conversion, 10-bit length output)

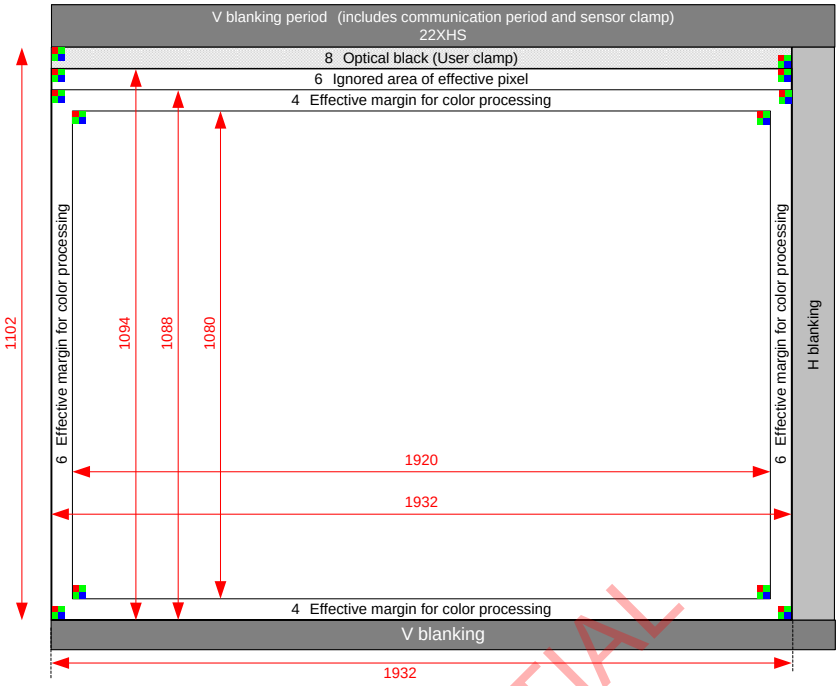


Readout Pixel Image Diagram (1920 × 1080)

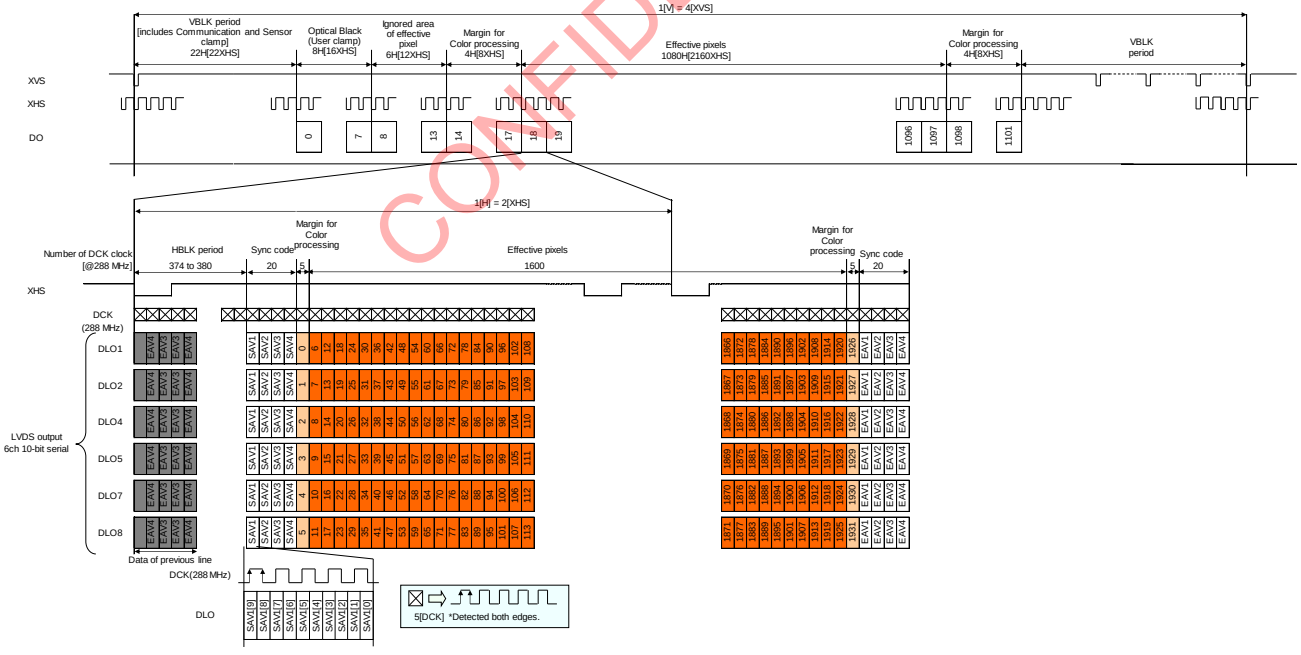


Readout Drive Timing

(Sub-LVDS) MODE4: Horizontal/vertical 2/2-line binning low power consumption drive (10-bit A/D conversion, 10-bit length output)

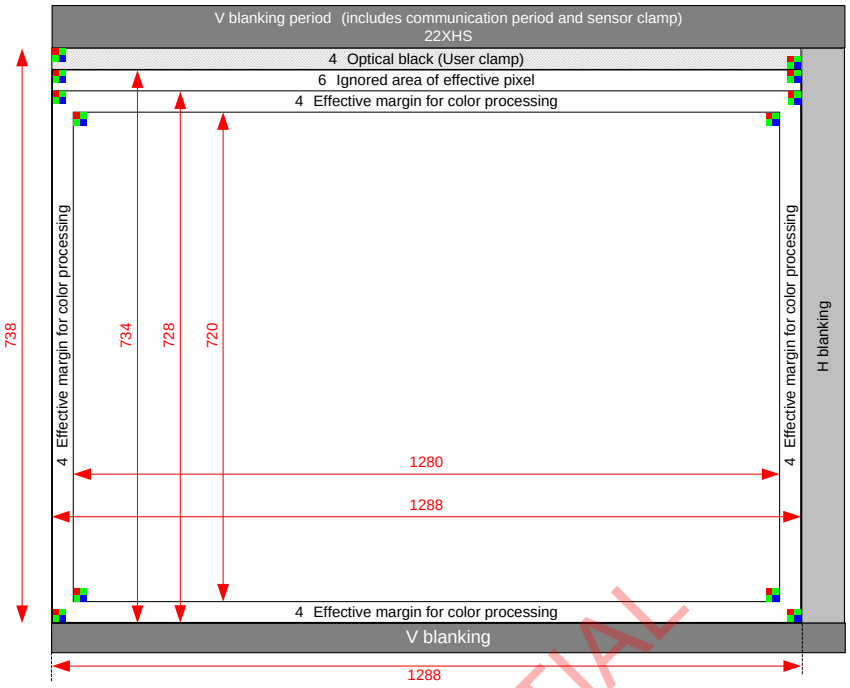


Readout Pixel Image Diagram (1920 × 1080)

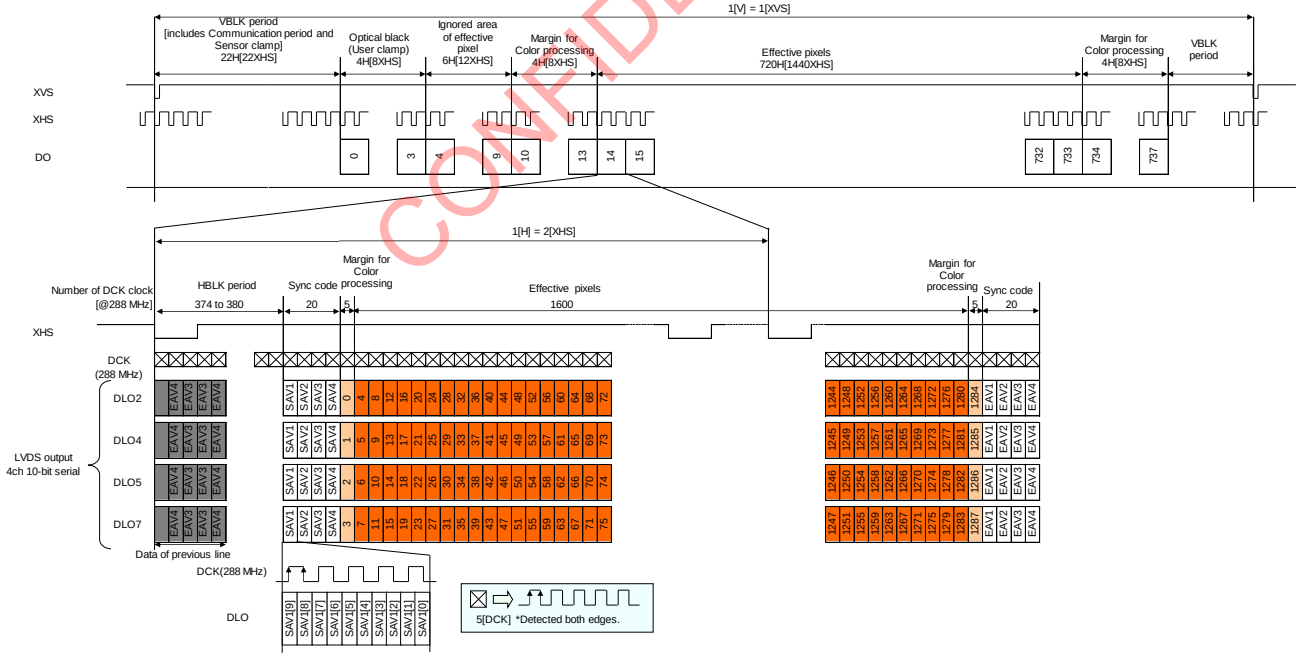


Readout Drive Timing (SVR = 3h)

(Sub-LVDS) MODE5: Vertical 2/3 subsampling binning horizontal 3 binning (10-bit A/D conversion, 10-bit length output)

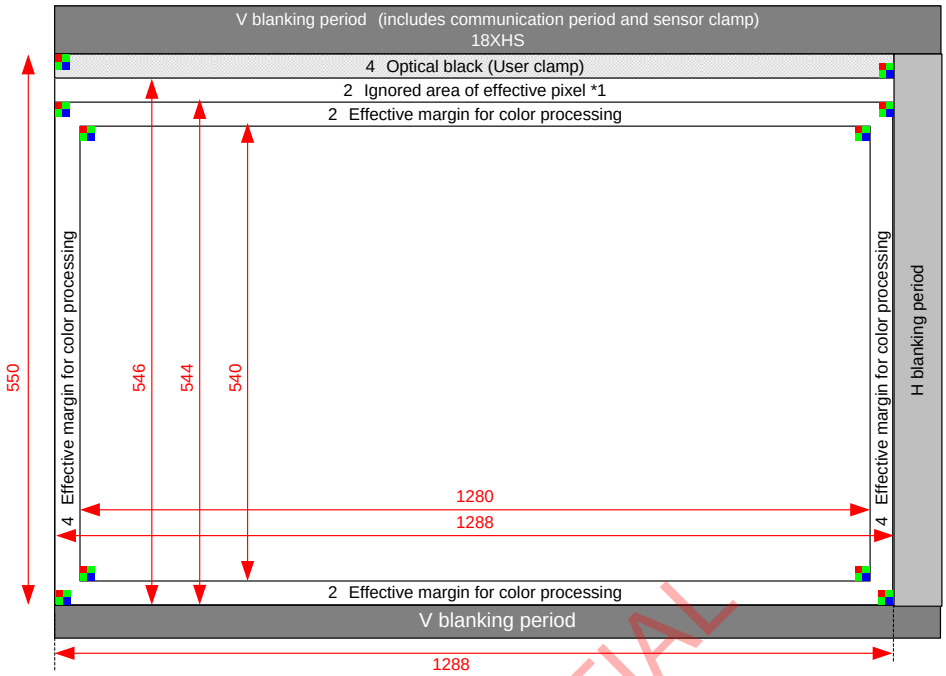


Readout Pixel Image Diagram (1280 × 720)

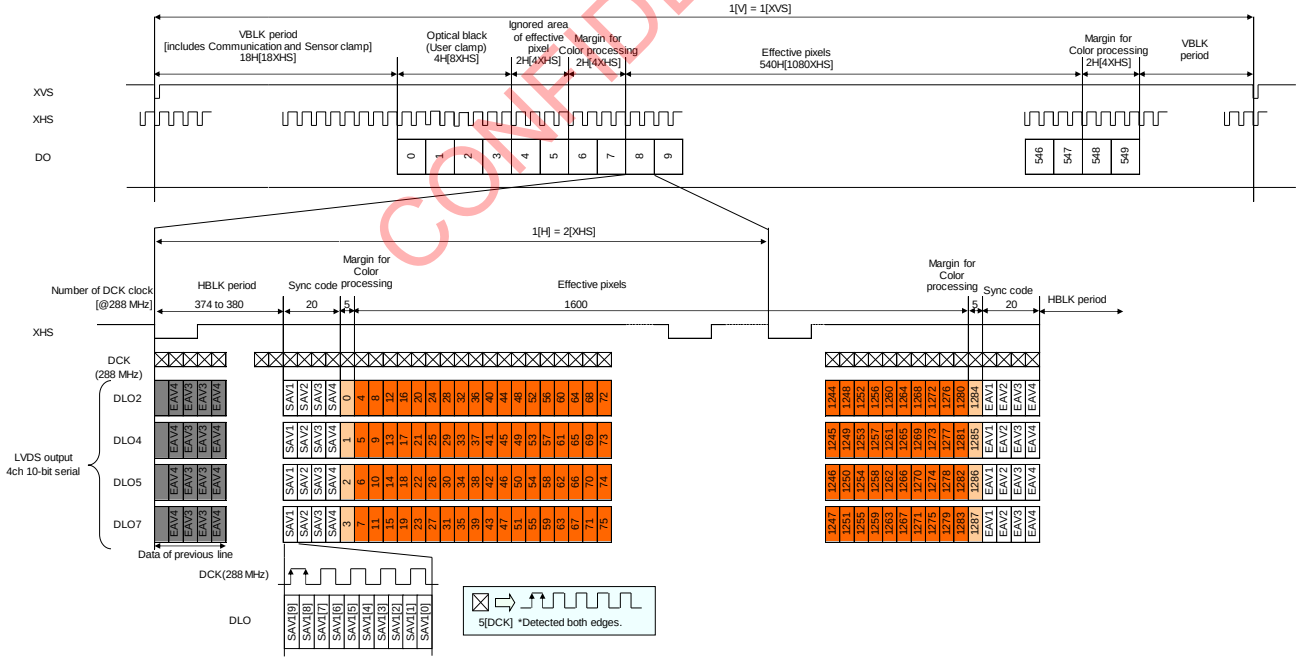


Readout Drive Timing

(Sub-LVDS) MODE6: Vertical 2/8 subsampling horizontal 3 binning (10-bit A/D conversion, 10-bit length output)



Readout Pixel Image Diagram (1280 × 540)



Readout Drive Timing

Vertical Arbitrary Cropping (Sub-LVDS)

Vertical cropping region of this sensor can be arbitrarily changed by registers.

TBD

Horizontal arbitrary cropping function (Sub-LVDS)

Horizontal cropping region of this sensor can be arbitrarily changed by registers.

TBD

Electronic Shutter Timing When Using Sub-LVDS

1. SHR, SVR Setting (Sub-LVDS)

The exposure start timing can be designated by setting the electronic shutter timing register SHR.
Note that this setting value unit is 1XHS period regardless of the readout drive mode. In addition, the vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal period inside is (SVR value + 1) times as long as XVS signal period.

Shutter Setting (Sub-LVDS)

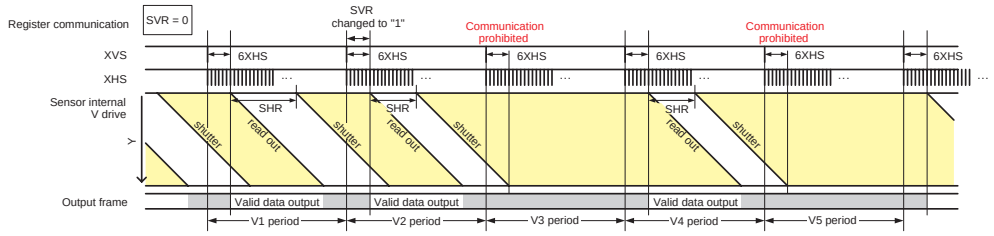
Name	Sub-LVDS Address	Bit	Function
SHR [7:0]	000Ch	[7:0]	Specifies the integration start horizontal period
SHR [15:8]	000Dh	[7:0]	
SVR [7:0]	000Eh	[7:0]	Specifies the integration shutdown vertical period
SVR [15:8]	000Fh	[7:0]	

Register	Register Value		Function
SHR	12 to {(SVR value + 1) × Number of XHS pulses per frame − 4}	Readout mode No.0, 1 All-pixel scan mode (12 bits) All-pixel scan mode (10 bits)	Specifies the integration start horizontal period
	8 to {(SVR value + 1) × Number of XHS pulses per frame − 4}	Readout mode No.2, 3, 4 Horizontal/vertical 2/2-line binning mode AD 12bits, AD 10bits, Low power consumption	
	8 to {(SVR value + 1) × Number of XHS pulses per frame − 4}	Readout mode No.5 Vertical 2/3 subsampling binning horizontal 3 binning mode	
	4 to {(SVR value + 1) × Number of XHS pulses per frame − 2}	Readout mode No.6 Vertical 2/8 subsampling horizontal 3 binning mode	
	0 to {(SVR value + 1) × Number of XHS pulses per frame − 130}	Global reset shutter mode (SMD = 1) (12 bits)	
	0 to {(SVR value + 1) × Number of XHS pulses per frame − 130}	Global reset shutter mode (SMD = 1) (10 bits)	
SVR	0h to FFFFh *Note 2.		Specifies the integration shutdown vertical period

Note)
1. See ”Integration Time in Each Readout Drive Mode” on page TBD for the integration time calculation formula.
2. The SVR register definition areas are guaranteed as sensor functions, but the characteristics are not guaranteed.
3. SMD is the electronic shutter drive mode register (address 0008h, bit [0]).

2. SVR Operation (Sub-LVDS)

Example of Electronic Shutter Operation when using Sub-LVDS is shown below.



Example of SVR operation

Note) In vertical sync signal subsampling periods (Example of SVR Operation: V3 and V5 periods), communication is prohibited during the normal communication period (the 6XHS period after the vertical sync signal XVS is input), except in the following case.

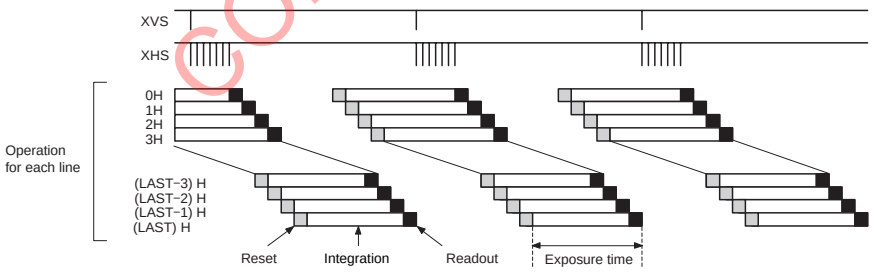
1. When stopping vertical sync signal subsampling using the break mode register SSBRK.

3. Electronic Shutter Drive Mode (Sub-LVDS)

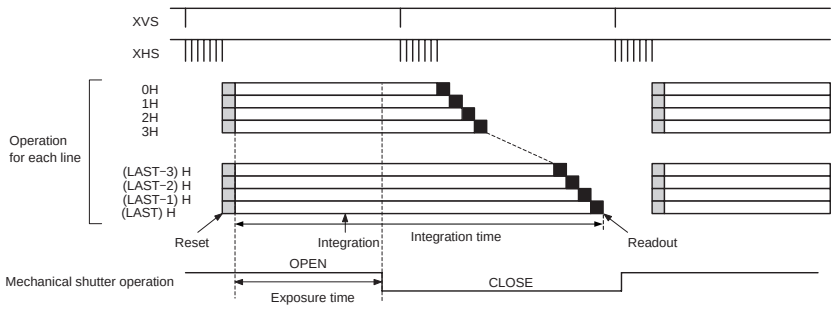
Global reset shutter operation can be performed by setting the electronic shutter drive mode register SMD. Rolling shutter operation performs pixel reset and integration sequentially in line units in sync with the XHS signal. Global reset shutter operation resets all pixels at once and then starts integration after that.
("Integration" is the state of a pixel between the reset and the readout. Pixels accumulate all the power of input light.)
The mechanical shutter must also be used during global reset shutter operation to make the exposure time the same for all pixels.

SMD Setting

Name	CSI-2 Address	Bit	Register value	Function
SMD	0008h	[0]	0h	Rolling shutter (normal shutter mode)
			1h	Global reset shutter



Rolling Shutter Operation



Global Reset Shutter Operation

4. Integration Time in Each Readout Drive Mode and Mode Changes When Using Sub-LVDS

4-1. Integration Time in Each Readout Drive Mode (Sub-LVDS)

The integration time for this sensor's output data is set using the electronic shutter timing setting registers SHR, SVR and SPL. The formulas and constants used to calculate the integration time are shown below.
In addition, the frame rate can be reduced by setting the SVR register to “1” or more.

◆Integration time of normal readout drive mode (Sub-LVDS)

Integration Time [s] = [{Number of XHS per XVS period × (SVR value + 1) – (SHR value)}
× Number of clock per XHS Period + Number of clocks per internal offset period]
/ (INCK frequency [Hz] × INCK multiply rate)

* Number of clock per XHS Period is in conversion of INCK = 72 MHz.
* See the following tables for the numbers of clocks per internal offset period and INCK multiply rate.
* See “Electronic Shutter Timing” on page TBD for the SHR register setting range.

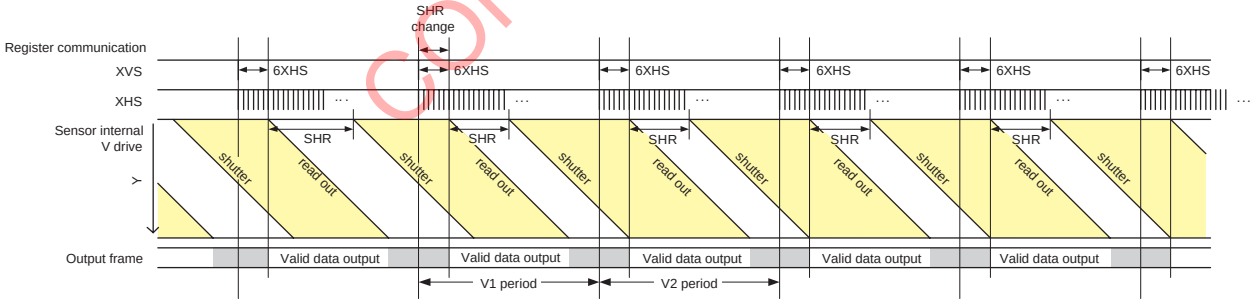
Number of clocks per internal offset period (Sub-LVDS) (TENTATIVE)

Readout mode No.	0	1	2	3	4	5	6
Number of clocks per internal offset period	169	112	112	112	112	112	112

INCK multiply rate (Sub-LVDS)

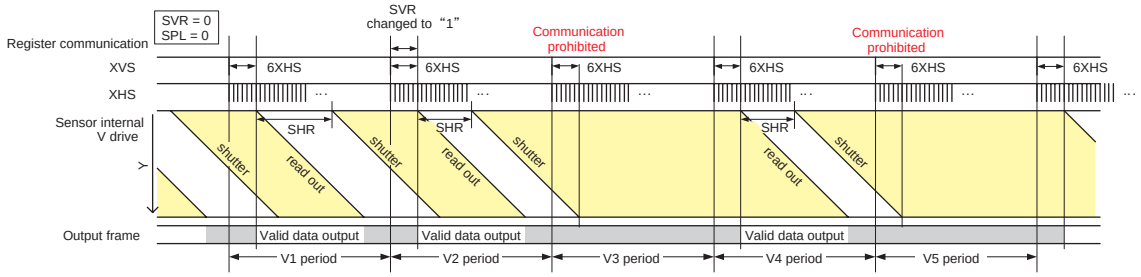
INCK frequency setting [MHz]	72	36	24	12
INCK multiply rate	1	2	3	6

The figure below shows operation when changing SHR. The V1 and V2 periods in the figure below are two continuous XVS periods. The SHR value set within the first 6XHS periods (recommended serial communication period) of V1 is updated internally at the end of the 6XHS periods, and then output data which reflect the new setting is output in the V2 period. Note that the SHR setting and output are offset by 1XVS period.



SHR Change Sequence (Sub-LVDS)

The vertical sync signal XVS can be subsampled inside the sensor according to the SVR register. The vertical sync signal period inside the sensor is (SVR value + 1) times as long as XVS signal period. Therefore the frame rate is multiplied by 1/(SVR value + 1) according to the SVR value.
The figure below shows the operation when changing the SVR register. The example in the figure below shows the update timing when SPL = 0 and the SVR value is changed from “0” to “1”. The SVR value set within the first 6XHS periods (recommended serial communication period) of V2 is updated internally at the end of the 6XHS periods, and then applied from the shutter operation in the V2 period. Readout operation is not performed in the V3 period, and output data which reflect the changing of SVR is output in the V4 period.
The image data of the V1 period before the SVR value is changed is output as valid data in the V2 period.
In addition, note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V3 period (the frame during which readout operation is not performed)



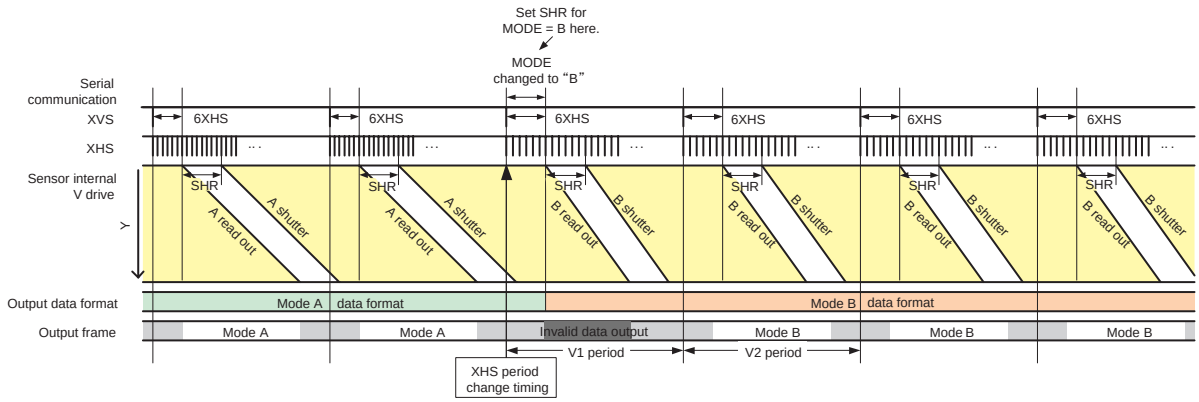
SVR Change Sequence (Sub-LVDS)

4-2. Operation when Changing the Readout Drive Mode (Sub-LVDS)

The following change cases are treated as mode transition on this sensor.

1. Changing the readout mode setting
2. Changing the vertical direction readout inversion setting

One frame of invalid data is always generated when changing the readout drive mode.
The figure below shows the mode transition sequence (Mode A to Mode B). The output data is invalid in the frame (V1 period in figure when SVR = 0) in which the setting is changed to Mode B. Valid data which reflect the new setting is output from the next frame (V2 period).
If the XHS period for Mode A and Mode B differs, change XHS period at the timing shown in the figure below (V1 head).
In addition, note that when the output data length or the output data rate differ in Mode A and Mode B, the new data format is output from the start of the 7th XHS of the frame (V1 period) in which the setting is changed to Mode B.



Mode Transition (Sub-LVDS)

4-3. Recommended Global Reset Shutter Operation Sequence (Sub-LVDS)

The recommended global reset shutter operation sequence is shown below. Operation in this mode spans plural XVS periods. Global reset shutter is performed in the first XVS period, and the data is output in following other XVS periods.
The exposure time can be adjusted by varying the XVS input period. However, the minimum XVS period is 14XHS periods. In addition, the mechanical shutter must also be used to make the exposure time the same for all pixels. See “Electronic Shutter Timing” on page TBD for the SHR register setting range.

Recommended Operating Sequence for Global Reset Shutter (Sub-LVDS)

Operation item	Description	Explanatory diagram
Normal	When performing global reset shutter partway through rolling shutter operation	Global reset shutter normal operation
Continuous	When performing global reset shutter operation continuously	Global reset shutter continuous operation

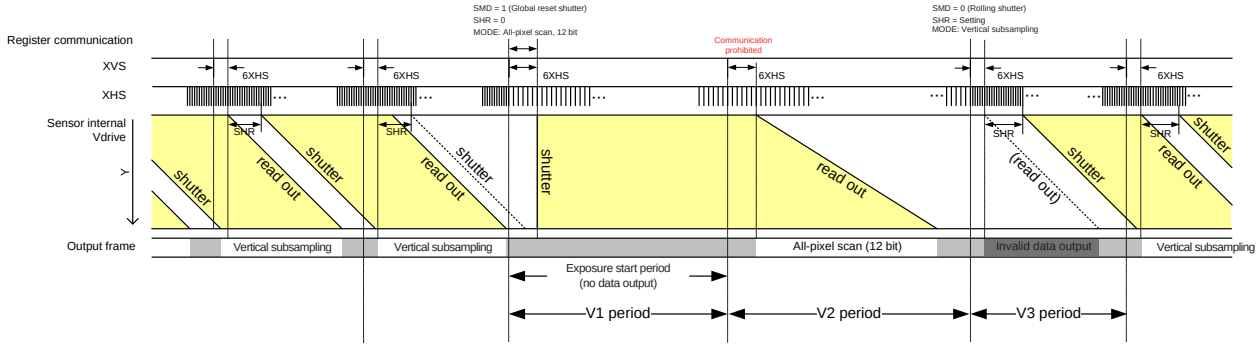
Normal Operation

Operation when performing global reset shutter + all-pixel scan (12 bits) one time partway through rolling shutter operation is shown below.
Vertical subsampling mode is described as a typical example of rolling shutter operation, but the transition operation is the same for all modes that use rolling shutter.
V1 to V3 in the figure below are three continuous XVS periods. When the global reset shutter settings (SMD = 1, register setting for all-pixel scan mode (12 bits)) are made within the first 6XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the 6XHS period. Global reset shutter readout data is output during the V2 period.
Communication to return to the original mode (SMD = 0, register setting for vertical subsampling mode, SHR should also be changed as necessary) is performed at the start of the V3 period.
The output data for the frame immediately after that (the V3 period in the figure) is invalid.
Note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) of the V2 period. The table below shows the integration start time of the exposure start period (V1 period).

Integration Start Time of the Exposure Start Period (Sub-LVDS) TENTATIVE

Readout mode No.	Integration start time of the exposure start period (XVS reference)
0	Approx. 491 [INCK] after the (6 + SHR) XHS period ends *1
1	Approx. 258 [INCK] after the (6 + SHR) XHS period ends *1

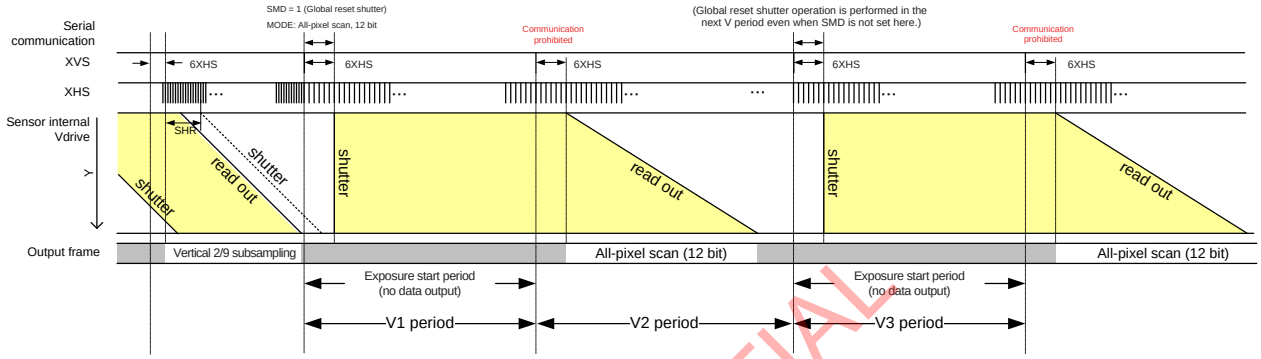
*1 Number of clocks in conversion of INCK = 72 MHz



Global Reset Shutter Normal Operation (Sub-LVDS)

Continuous Operation (Sub-LVDS)

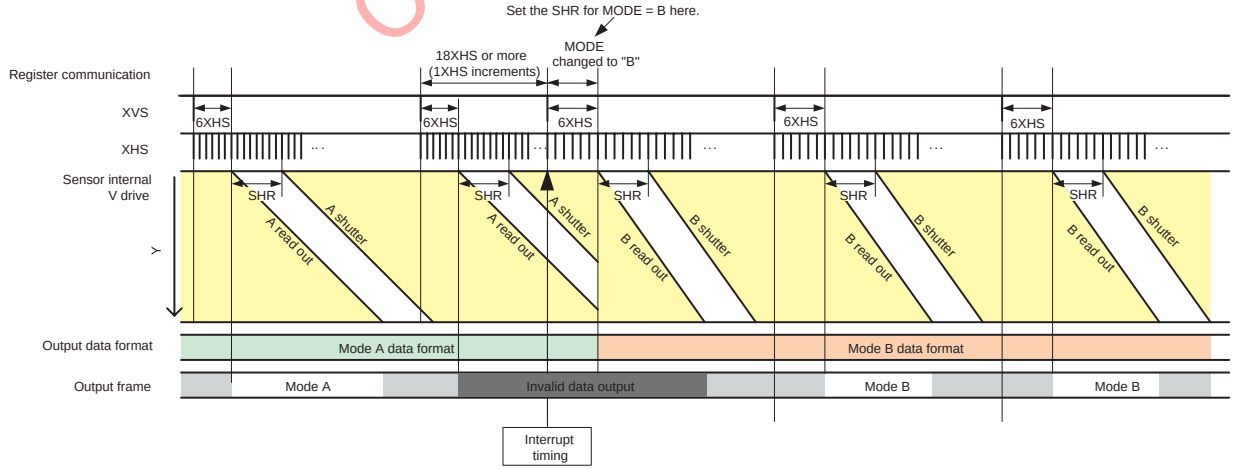
Operation when continuously performing global reset shutter + all-pixel scan (12 bits) is shown below.
V1 to V3 in the figure below are three continuous XVS periods. When the global reset shutter + all-pixel scan (12 bits) settings (SMD = 1, register setting for all-pixel scan mode (12 bits)) are made within the first 6XHS periods (recommended serial communication period) of the V1 period, integration starts simultaneously for all pixels at the end of the first 6XHS period of the V1 period, and the all-pixel scan (12 bits) data is output in the V2 period. The operation during V1 and V2 periods is then repeated each time XVS is input until the mode setting is changed next. Note that communication is also prohibited during the first 6XHS periods (recommended serial communication period) in the V2 period.
See the previous section for a description of the procedure when changing from continuous operation to a different readout mode.



Global Reset Shutter Continuous Operation (Sub-LVDS)

4-4. Interruptive Mode Change (Sub-LVDS)

The sensor mode can be changed using interrupts in all modes.
When changing the mode using an interrupt, the mode can be changed by inputting XVS in sync with XHS after 18XHS periods or more have elapsed from the start of the frame, and transmitting the mode setting register value within the communication period. In addition, the data output before the interrupt mode change is cut off at the timing of the interrupt mode change.

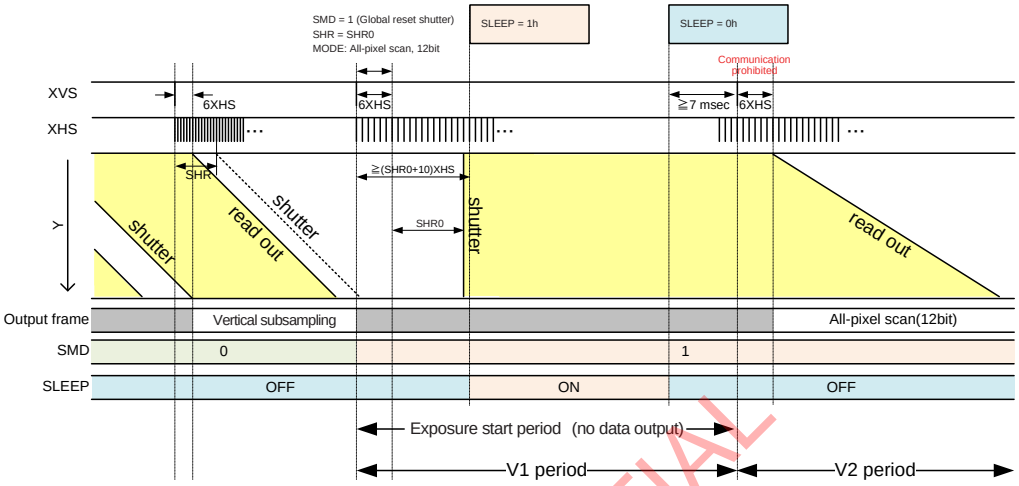


Interruptive Mode Change

4-5. Low Power Consumption Drive in Exposure Time (Sub-LVDS)

Low Power Consumption Drive in Exposure Time When Using Global Reset Shutter Operation (Sub-LVDS)

The sequence of low power consumption drive when exposing of global reset shutter operation is shown below.
To change to low power consumption drive, set the SLEEP register to 1h after (SHR setting value + 10) × XHS period or more in the frame of changing the register SMD from 0h to 1h.
And for readout, set SLEEP to 0h before 7 ms of readout frame in order to cancel low power consumption mode.

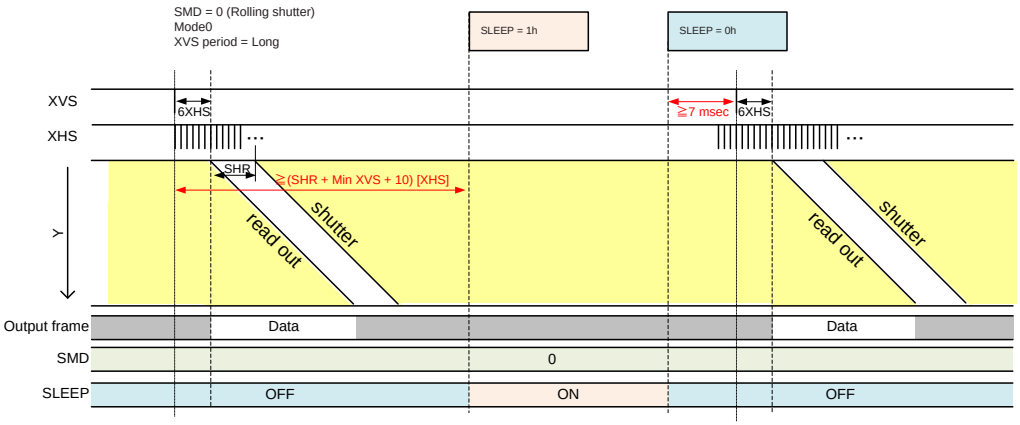


Low Power Consumption Drive in Exposure of Global Reset Shutter Operation Sequence (Sub-LVDS)

Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation (Sub-LVDS)

To extend the integration time, extending XVS period is available other than SVR register. SLEEP register can reduce power consumption during integration time when using long XVS period. To change to low power consumption drive, set SLEEP register to 1h after (SHR value + min XVS + 35) × XHS period or more in the frame of changing the register SMD from 0h to 1h. And for readout, set SLEEP to 0h before 7 ms of readout frame in order to cancel low power consumption mode.

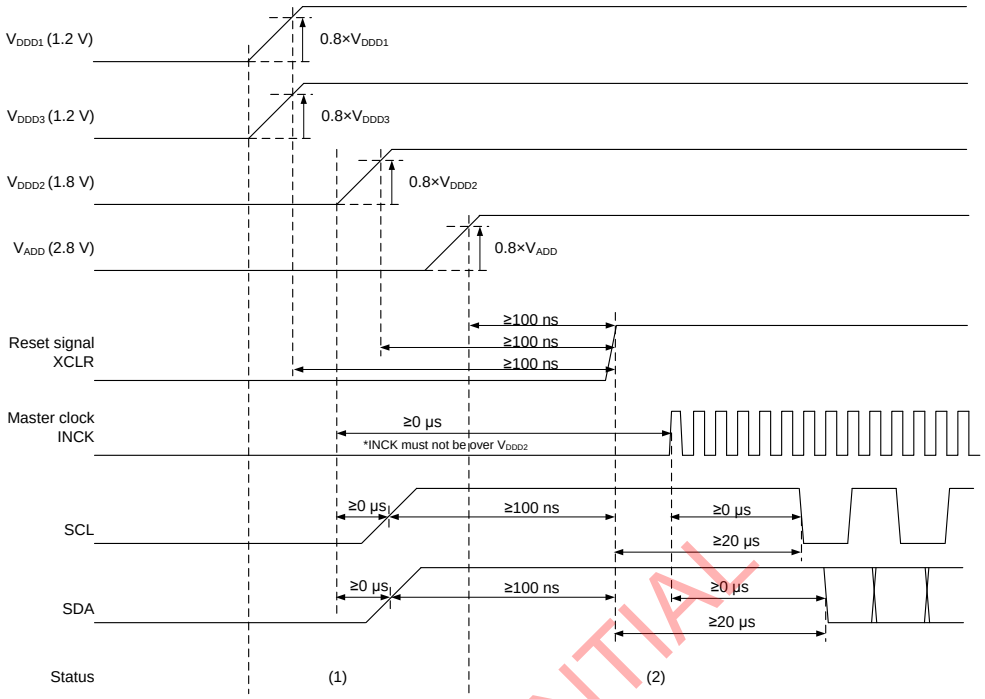
When using SVR ≥ 1h, this sequence is not necessary.



Low Power Consumption Drive in Integration Time When Using Rolling Shutter Operation (Sub-LVDS)

Power-on/off Sequence when using CSI-2

1. Power-on Sequence (CSI-2)

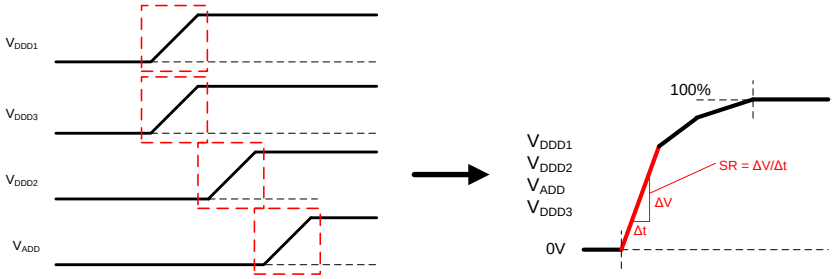


Power-on Sequence (CSI-2)

Period name	Remarks
(1) Power stabilization period	All input signals are set to Low level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}.
(2) Register communication period for standby cancel	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}. Then set XCLR to “H” and start the standby cancel sequence.

2. Slew Rate Limitation of Power-on Sequence (CSI-2)

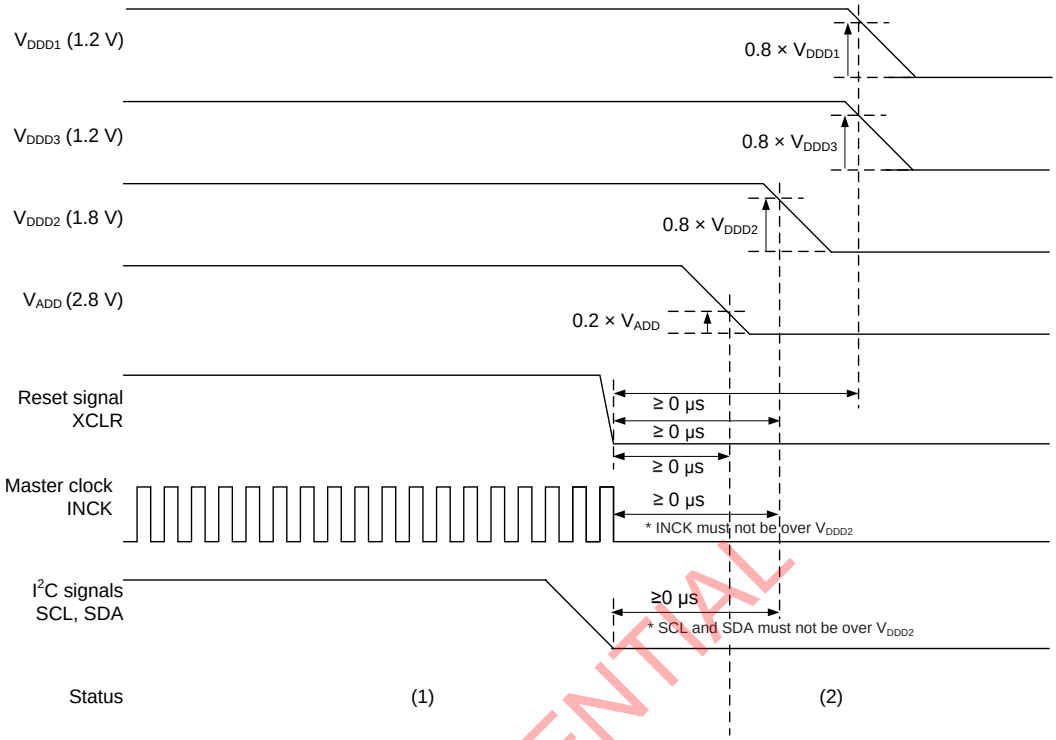
Conform to the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/us	
		V_{DDD2} (1.8 V)	—	25	mV/us	
		V_{DDD3} (1.2 V)	—	25	mV/us	
		V_{ADD} (2.8 V)	—	25	mV/us	

3. Power-off Sequence (CSI-2)

Make sure that all input signals are set to LOW level in the area of (2).



Power-off Sequence (CSI-2)

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off period	Turn the power supplies off after all input signals are set to "Low" level except SCL and SDA. Set SCL and SDA to "Low" level at the same time with turning off the power supply of V_{DDD2}. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}.

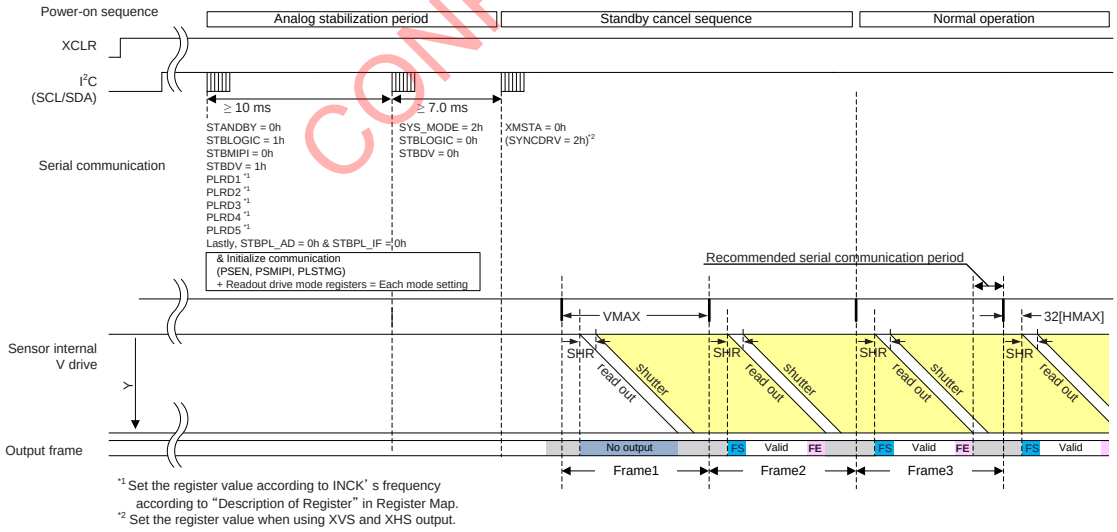
Standby Cancel Sequence when using CSI-2

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancels sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

1. After performing the power-on start-up sequence, make the following register setting.
   - Set address 3000h, bit [4:0] to “12h” (STANDBY register = 0h, STBLOGIC register = 1h, STBMIPI register = 0h, STBDV register = 1h).
   - Set the following registers to the appropriate value according to INCK’s frequency.
     Refer to “Description of Register” of “Register Map” on page TBD.
     Address 3120h, bit [7:0], Address 3121h, bit [7:0] (PLRD1 register).
     Address 3122h, bit [7:0] (PLRD2 register).
     Address 3129h, bit [7:0] (PLRD3 register).
     Address 312Ah, bit [7:0] (PLRD4 register).
     Address 312Dh, bit [7:0] (PLRD5 register).
     Lastly, set address 310Bh, bit [7:0] to “00h” (STBPL_IF register = 0h, STBPL_AD register = 0h).
   - Initialize communication
     Set all registers of PSMOVEN, PSMIPI1 to 4 and PLSTMG settings.
     See "Readout Drive Pulse Timing" on pages TBD. Register communication can be performed even when STANDBY is 1h and there is no restriction on the communication order.
     Set Readout drive mode registers
     Set the mode registers of the "Register Setting for Each Readout Drive Mode" on page TBD. Furthermore, set the required shutter and gain registers.

2. After the 1st stabilization period of 10 ms or more, make the following register setting.
   - Set address 3000h, bit [4:0] to “00h” (STANDBY register = 0h, STBLOGIC register = 0h, STBMIPI register = 0h, STBDV register = 0h).
   - Set address 303Eh, bit [1:0] to “02h” (SYS_MODE register = 2h)

3. After the 2nd stabilization period of 7.0ms or more,
   - Set address 30F4h, bit [0] to “0h” (XMSTA =0h).
   - Set address 3018h, bit [1:0] to “2h” (SYNCDRV =2h) (when using XHS and XVS output)

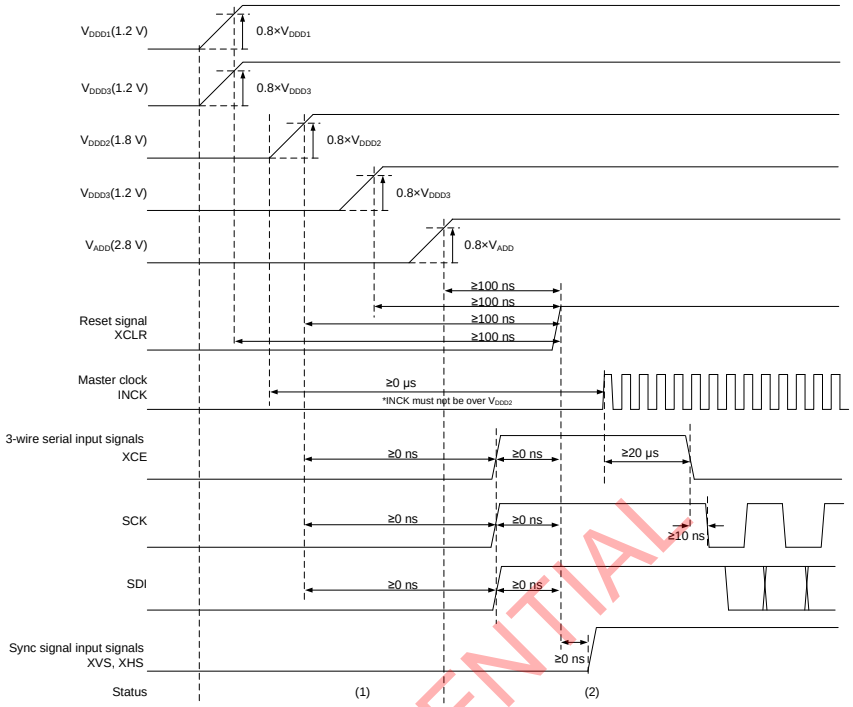


*1 Set the register value according to INCK’s frequency according to “Description of Register” in Register Map.
*2 Set the register value when using XVS and XHS output.

Power-on/off Sequence when using Sub-LVDS

1. Power-on Sequence (Sub-LVDS)

Make sure that both XVS and XHS must be set to LOW while XCLR is LOW.

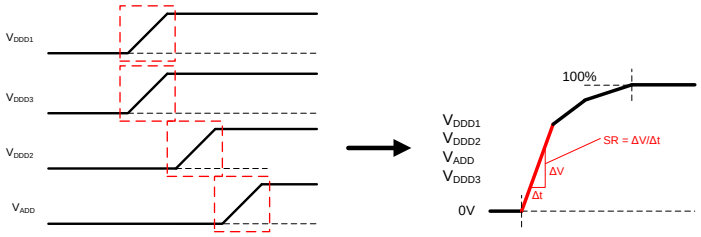


Power-on Sequence (Sub-LVDS)

Period name	Remarks
(1) Power stabilization time	All input signals are LOW level. There are no constraints of the power-on sequence with V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}.
(2) Standby cancel register communication	Wait 100 ns after the last power supply in V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}. Then set XCLR to “High” level and start the standby cancel sequence. XVS and XHS must be set to LOW while setting XCLR to LOW.

2. Slew Rate Limitation of Power-on Sequence (Sub-LVDS)

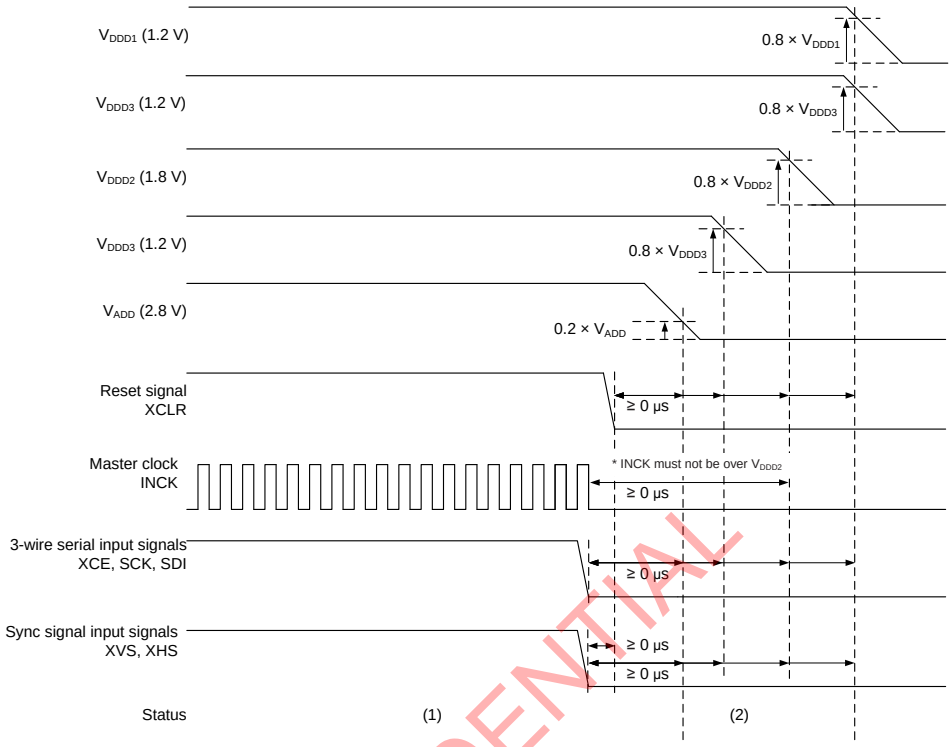
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	V_{DDD1} (1.2 V)	—	25	mV/µs	
		V_{DDD2} (1.8 V)	—	25	mV/µs	
		V_{DDD3} (1.2 V)	—	25	mV/µs	
		V_{ADD} (2.8 V)	—	25	mV/µs	

3. Power-off Sequence (Sub-LVDS)

Make sure that all input signals for the 3-wire serial interface and other signals are LOW in the period of (2) and both XVS and XHS must be set to LOW while setting XCLR to LOW.



Power-off Sequence (Sub-LVDS)

Period name	Remarks
(1) Pixel output period	Pixel signal output period
(2) Power-off time	Turn the power supplies off after LOW level is set to all input signals. There are no constraints of the power-off sequence with V_{ADD}, V_{DDD1}, V_{DDD2} and V_{DDD3}. XVS and XHS must be set to LOW while setting XCLR to LOW.

Standby Cancel Sequence (Sub-LVDS)

After the power-on start-up sequence is performed, this sensor is in standby mode. The standby cancel sequence is described below. Also perform this same sequence when canceling standby mode after shifting from normal operation to standby mode.

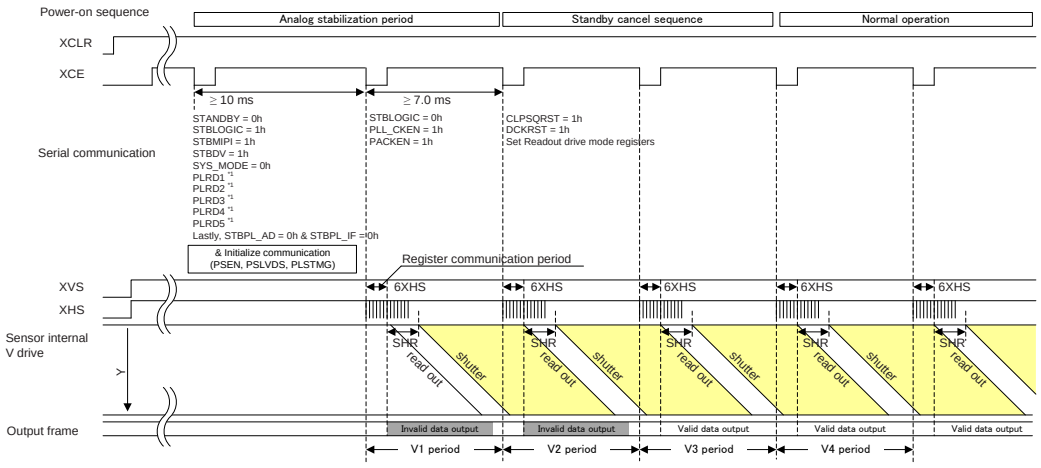
After performing the power-on start-up sequence, make the following register setting.

1. After performing the power-on start-up sequence, make the following register setting.
   - Set address 0000h, bit [4:0] to “1Ah” (STANDBY register = 0h, STBLOGIC register = 1h, STBMIPI register = 1h, STBDV register = 1h).
   - Set address 003Eh, bit [1:0] to “0h” (SYS_MODE register = 0h).
   - Set the following registers to the appropriate value according to INCK’s frequency.
     Refer to “Description of Register” of “Register Map” on page TBD.
     Address 0120h, bit [7:0], Address 3121h, bit [7:0] (PLRD1 register).
     Address 0122h, bit [7:0] (PLRD2 register).
     Address 0129h, bit [7:0] (PLRD3 register).
     Address 012Ah, bit [7:0] (PLRD4 register).
     Address 012Dh, bit [7:0] (PLRD5 register).
     Lastly, set address 010Bh, bit [7:0] to “00h” (STBPL_AD register = 0h, STBPL_IF register = 0h).
   - Initialize communication
     Set all registers of PSMOVEN, PSLVDS1 to 4 and PLSTMG settings in "Readout Drive Pulse Timing" on pages
     TBD. Register communication can be performed even when STANDBY is 1h and there is no restriction on the communication order. Vertical and horizontal sync signal, XVS and XHS, can be input during this communication.

2. After the 1st analog stabilization period of 10 ms or more,
   - Set address 00E6h, bit [7:0] to “01h” (PLL_CKEN register = 01h).
   - Set address 00E8h, bit [7:0] to “01h” (PACKEN register = 01h).
   - Set address 0000h, bit [4:0] to “18h” (STANDBY register = 0h, STBLOGIC register = 0h, STBMIPI register = 1h, STBDV register = 1h).

3. After the 2nd analog stabilization period of 7.0 ms or more, set the following registers during the register communication period of the next frame (the V2 period).
   - Set address 0001h, bit [4] to “1h” (CLPSQRST=1h) and set address 0009h, bit [0] to “1h” (DCKRST=1h)
   - Readout drive mode registers
     Set the mode registers of the "Register Setting for Each Readout Drive Mode" on pages TBD.
   - Furthermore, set the required shutter and gain registers.

In addition, when using the V3 period data after canceling standby mode, transmit the mode select register required for normal operation during the communication period of V2 period.



*1 Set the register value according to INCK’s frequency according to “Description of Register” in Register Map.

Spot Pixel Specifications

(V_{ADD} = 2.8 V, V_{DDD1} = 1.2 V, V_{DDD2} = 1.8 V, V_{DDD3} = 1.2 V, Tj = 60 ˚C, 29.97 frame/s, reference gain 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone						Measure-ment method	Remarks
		0	I	II	II'	OB	III		
Black pixels at high light	TBD % ≤ D	TBD				No evaluation criteria applied		1	
White pixels at high light	TBD % ≤ D					No evaluation criteria applied		1	
White pixels in the dark	TBD digit ≤ D < TBD digit	TBD					No evaluation criteria applied	2	1/30 s integration
	TBD digit ≤ D						No evaluation criteria applied		
FD white pixels	TBD digit ≤ D < TBD digit	TBD spots					No evaluation criteria applied	2	4 pixels occur per spot.
	TBD digit ≤ D						No evaluation criteria applied		
Black pixels at signal saturated	D ≤ TBD digit	0				No evaluation criteria applied		3	

Note) 1. D...Spot pixel level. Black pixels at signal saturated are prescribed at the signal output in spot pixel part.
2. Zone definition is illustrated in the figure below.
3. 1 digit ≈ TBD mV when 12 bits output.

Spot Pixel Zone Definition

TBD

Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
TBD mV or higher	TBD pcs
TBD mV or higher	TBD pcs
TBD mV or higher	TBD pcs
10.0 mV or higher	TBD pcs
24.0 mV or higher	TBD pcs
50.0 mV or higher	TBD pcs
72.0 mV or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

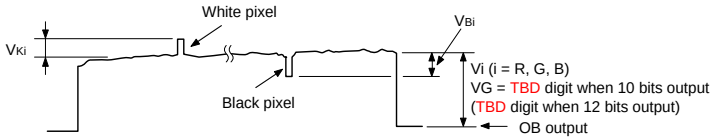
Material_No.03-0.0.8

Measurement Method for Spot Pixels

1. Black or white pixels at high light

After adjusting the luminous intensity so that the average value of the G channel signal output is TBD digit when 10 bits output (TBD digit when 12 bits output), measure the local dip point (black pixel at high light, V_{BR}, V_{BG} and V_{BB}) and peak point (white pixel at high light, V_{KR}, V_{KG} and V_{KB}) in each channel signal output. Substitute the values into the following formula.

Spot pixel level = (V_{Ki} (or) V_{Bi})/V_i × 100 [%] (i = R, G, B)



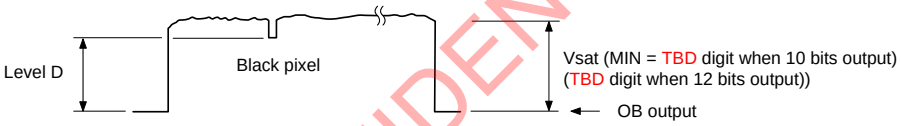
Signal output waveform of R/G/B channel (Black or White Pixels at High Light)

2. White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated

Set the device to operate in saturation and measure the local dip point in each of the R, G and B channels using the OB output with sensor as a reference.



Signal output waveform of R/G/B channel (Black Pixels at Signal Saturated)

Spot Pixel Pattern Specifications

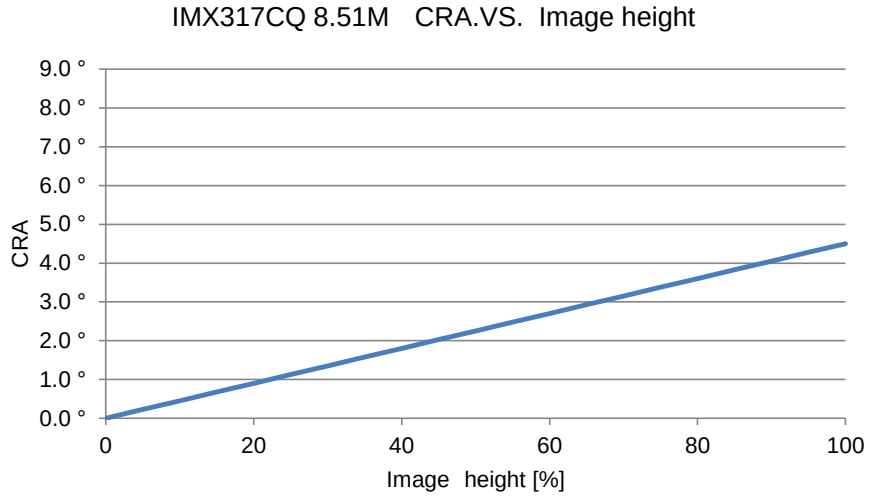
TBD

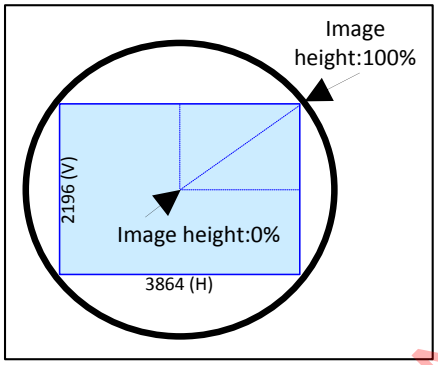
Stain Specifications

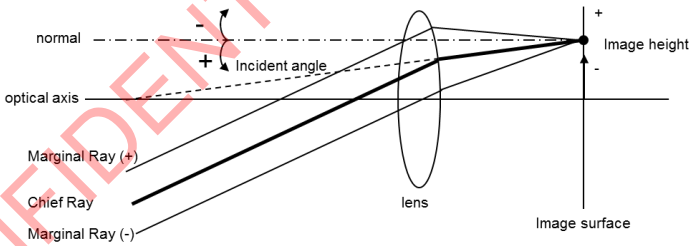
TBD

Relation between Image Height and target CRA

Tentative







Marking

TBD

Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

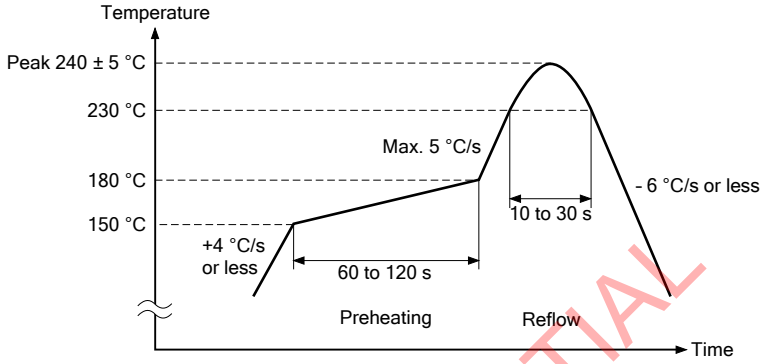
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 24 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

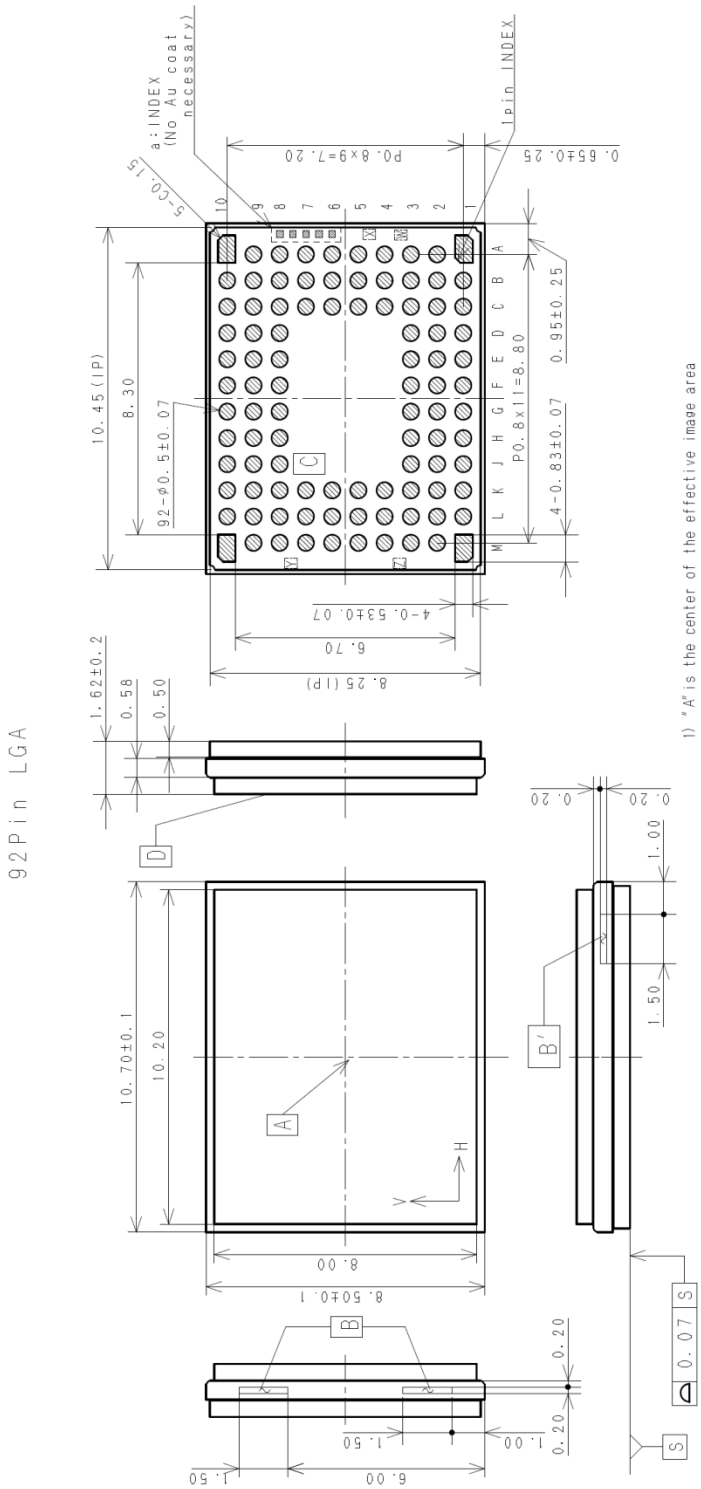
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

TENTATIVE



1) "A" is the center of the effective image area
2) The two points"B"of the package are the horizontal reference
   The point"B"of the package is the vertical reference
3) The bottom"C"of the package is the height reference
4) Base level"S" is a virtual flat surface calculated at three points(A10.M1.M10)
   of back side terminal
5) The center of the effective image area relative to" B" and" B' " is
   (H. V) = (5.257. 4.146) ±0.075 mm
6) The rotation angle of the effective image area relative to" H" and" V" is ±0.5°
7) The height from the bottom" C" to the effective image area is 0.72±0.1 mm
   The height from the top of cover glass" D" to the effective image area is 0.90±0.1 mm
8) The tilt of the effective image area relative to the bottom" C" is less than 0.05 mm
   The tilt of the effective image area relative to the bottom" D" of the cover glass
   is less than 0.05 mm
9) The thickness of the cover glass is 0.50 mm, and the refractive index is 1.5
10) As for standard for resin overflow in package outside,
    it shall be accepted up to outermost line tolerance of package.
11) One character of alphabet or number shall be placed from W to Z part.
    (Plating pretermission)
12) Up to 5 indexes are arranged in "a" part.

PACKAGE STRUCTURE	
PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT	***g
DRAWING NUMBER	TENTATIVE

List of Trademark Logos and Definition Statements

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.