1/2.6-inch 2.3 Mp CMOS Digital Image Sensor with Global Shutter

AR0234CS

ON Semiconductor®

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The AR0234CS is a 1/2.6−inch 2Mp CMOS digital image sensor with an active−pixel array of 1920 (H) x 1200 (V). It incorporates a new innovative global shutter pixel design optimized for accurate and fast capture of moving scenes at full resolution 120 frame per second. The sensor produces clear, low noise images in both low−light and bright scenes. It includes sophisticated camera functions such as auto exposure control, windowing, row skip mode, column−skip mode, pixel−binning and both video and single frame modes. It is programmable through a simple two−wire serial interface. The AR0234CS produces extraordinarily clear, sharp digital pictures with an industry leading Global Shutter Efficiency, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and industrial inspection.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/2.6−inch (6.8 mm)
Active Pixels	1920 (H) x 1200 (V) = 2.3 Mp
Pixel Size	3.0 μm
Color Filter Array	RGB or Monochrome
Chief Ray Angle	0° or 28°
Shutter Type	Global Shutter
Input Clock Range	6−54 MHz
Output Pixel Clock (Maximum)	90 MHz
Output Serial Parallel	 8−bit/10−bit MIPI, 1, 2, or 4−lane D−PHY 1.2, CSI−2 8−bit/10−Bit
Frame Rate Full resolution 720p	 120fps (4− lane MIPI running at 30 fps per MIPI lane), Default Max data rate 900 Mbps/lane 30 fps (Parallel) 120 fps (MIPI) 50 fps (Parallel)
Responsivity Monochrome Color	 55 Ke/lux*s TBD
SNRMAX	37 dB
Dynamic Range	70 dB
Supply Voltage I/O Digital Analog	 1.8 or 2.8 V 1.2 V 2.8 V
Operational Power Consumption	<420 mW
Operating Temperature	−40°C to + 85°C (Ambient) −40°C to +105°C (Junction)
Package Options	9.995 x 5.595 CSP

Features

- Superior Low−light and IR Performance
- HD Video (1080p120)
- 8−bit/10−bit MIPI, 1/2/4−lane MIPI or 8−bit/10−bit Parallel Data Interface
- Automatic Black Level Calibration (ABLC)
- On−chip Auto Exposure Control with Statistics Engine for Any 5x5 Programmable ROI
- Horizontal and Vertical Mirroring, Windowing and Pixel Binning
- On−chip Histogram Auto Exposure Control for Any Programmable ROI
- 5 x 5 Statistics Engine for Any Programmable ROI
- Flexible Control for Row and Column Skip Mode
- On−chip Slave or Trigger Mode for Synchronization
- Built in Strobe Control
- On−Chip Phase Lock Loop (PLL)
- On−Chip Lens Shading Correction

Applications

- Bar Code Scanner
- Gesture Recognition
- 3D Scanning
- Positional Tracking
- Iris Scanning
- Augmented Reality
- Virtual Reality
- Biometrics
- Machine Vision

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0234CSSM28SUKA0−CP	2.3MP 1/2.6”, Mono, 28 deg CRA	CSP Chip Tray with Protective Film
AR0234CSSM28SUKA0−CR	2.3MP 1/2.6”, Mono, 28 deg CRA	CSP Chip Tray without Protective Film
AR0234CSSM28SUKA0−CP1	2.3MP 1/2.6”, Mono, 28 deg CRA	CSP Chip Tray with Protective Film Low MOQ
AR0234CSSM28SUKA0−CR1	2.3MP 1/2.6”, Mono, 28 deg CRA	CSP Chip Tray without Protective Film Low MOQ
AR0234CS3M28SUD20−E	2.3MP 1/2.6”, Mono, 28 deg CRA	Bare Die, Engineering Samples
AR0234CSSM28SUKAH3−GEVB	2.3MP 1/2.6”, Mono, 28 deg CRA	Demo Headboard
AR0234CS3M00SUKA0−CP−E	2.3MP 1/2.6”, Mono, 0 deg CRA	CSP Chip Tray with Protective Film, Engineering Samples
AR0234CS3M00SUD20−E	2.3MP 1/2.6”, Mono, 0 deg CRA	Bare Die, Engineering Samples
AR0234CSSM00SUKAH3−GEVB	2.3MP 1/2.6”, Mono, 0 deg CRA	Demo Headboard
AR0234CS3C28SUKA0−CP−E	2.3MP 1/2.6”, RGB, 28 deg CRA	CSP Chip Tray with Protective Film, Engineering Samples
AR0234CS3C28SUD20−E	2.3MP 1/2.6”, RGB, 28 deg CRA	Bare Die, Engineering Samples
AR0234CSSC28SUKAH3−GEVB	2.3MP 1/2.6”, RGB, 28 deg CRA	Demo Headboard
AR0234CS3C00SUKA0−CP−E	2.3MP 1/2.6”, RGB, 0 deg CRA	CSP Chip Tray with Protective Film, Engineering Samples
AR0234CS3C00SUD20−E	2.3MP 1/2.6”, RGB, 0 deg CRA	Bare Die, Engineering Samples
AR0234CSSC00SUKAH3−GEVB	2.3MP 1/2.6”, RGB, 0 deg CRA	Demo Headboard

NOTE: Please check with an ON Semiconductor sales representative for availability of these parts.

GENERAL DESCRIPTION

The ON Semiconductor AR0234CS can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full−resolution image at 120 frames per second (fps). It outputs 8−bit or 10−bit raw data using parallel output ports or 10−bit or 8−bit using serial (MIPI) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

The AR0234CS includes additional features to allow application−specific tuning: windowing, adjustable auto−exposure control, auto black level correction, on−board temperature sensor, row−skip and column−skip modes and binning modes.

The sensor is designed to operate in a wide ambient temperature range (–40°C to +85°C ambient).

FUNCTIONAL OVERVIEW

The AR0234CS is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 54 MHz. The maximum output pixel rate is 90 Mp/s, corresponding to a clock rate of 90 MHz. Figure 1 shows a block diagram of the sensor.

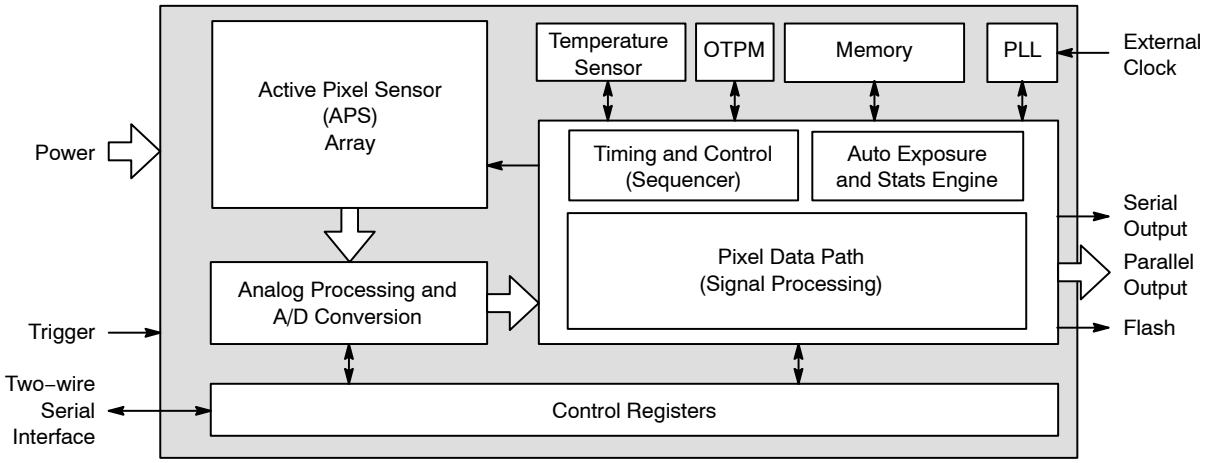


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.3 Mp Active−Pixel Sensor array. The AR0234CS features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All pixels simultaneously integrate light and store signal at the pixel. Once a row readout sequence has been initiated, each pixel's stored signal is then transfered through the analog signal chain (providing offset and gain) and then through each column analog to−digital converter (ADC). The output from the ADC is a 10−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 90 Mp/s, in parallel to frame and line synchronization signals.

FEATURES OVERVIEW

The AR0234CS Global Shutter sensor has a wide array of features to enhance functionality and to increase versatility. A summary of features follows.

- 3.0 μm Global Shutter Pixel
  To improve the low light performance and to capture the moving images accurately a large (3.0 μm) global shutter pixel is implemented for better image optimization.
- Operating Modes
  The AR0234CS works in master (video), Slave/ Trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In Slave/trigger mode, it accepts a trigger from external host to start exposure, then generates the exposure and readout timing. The external trigger signal allows for precise control of frame rate and register change updates. The exposure time is programmed through the two−wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- Frame Rate
  AR0234CS is capable of running up to 120 fps at full (1920 x 1200) resolution and 120 fps at 720p resolution for MIPI interface.
- Embedded Data and Statistics
  The AR0234CS has the capability to output image data and statistics embedded within the frame timing.
- Multi−Camera Synchronization
  The AR0234CS supports advanced line synchronization controls for multi−camera (stereo) support.
- Context Switching and Register Updates Context switching may be used to rapidly switch between two sets of register values.
- Gain
  A programmable analog gain of 1x to 16x applied globally to all color channels is available for along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Programmable analog gain for Parallel interface is limited to 8x.
- Automatic Exposure Control
  The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame.
- MIPI
  The AR0234CS Global Shutter image sensor supports one, two and four lanes of MIPI data. Compliant to MIPI standards:
  - MIPI Alliance Standard for CSI−2 version 1.2
  - MIPI Alliance Standard for D−PHY version 1.0
- PLL
  An on chip PLL provides reference clock flexibility and

supports spread spectrum sources for improved EMI performance.

- Reset
  The AR0234CS may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0234CS output pins may be tri−stated using a dedicated output enable pin.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.
- Silicon/OTPM Revision Information
  A revision register is provided to read out (via I^2C) silicon and OTPM revision information. This will be helpful to distinguish material if there are future OTPM or silicon revisions.
- Lens Shading Correction
  An on−chip lens shading correction algorithm is included
- Compression
  AR0234CS can optionally compress 10−bit data to 8−bit using DPCM compression.

ACTIVE ARRAY

The AR0234CS active pixel array is configured as 1920 columns by 1200 rows. The first active the pixel is top right corner of the active pixel array (see Figures 2 and 3 below).

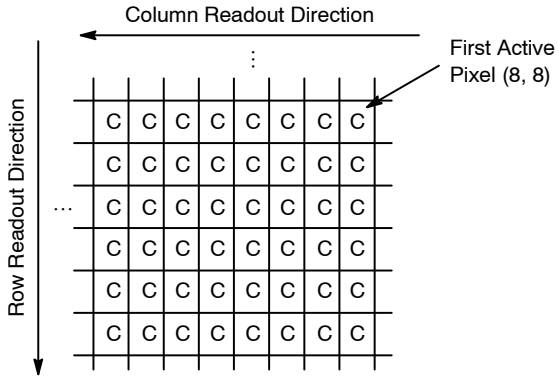


Figure 2. Pixel Mono Pattern Detail (Top Right Corner)

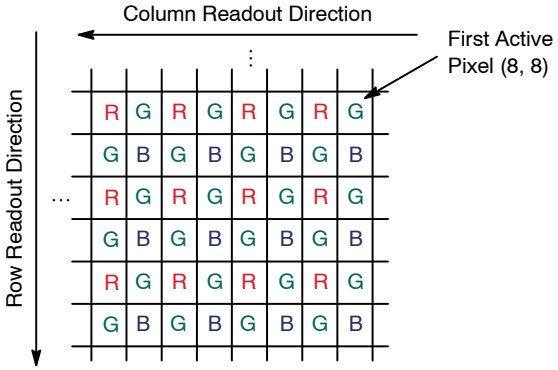
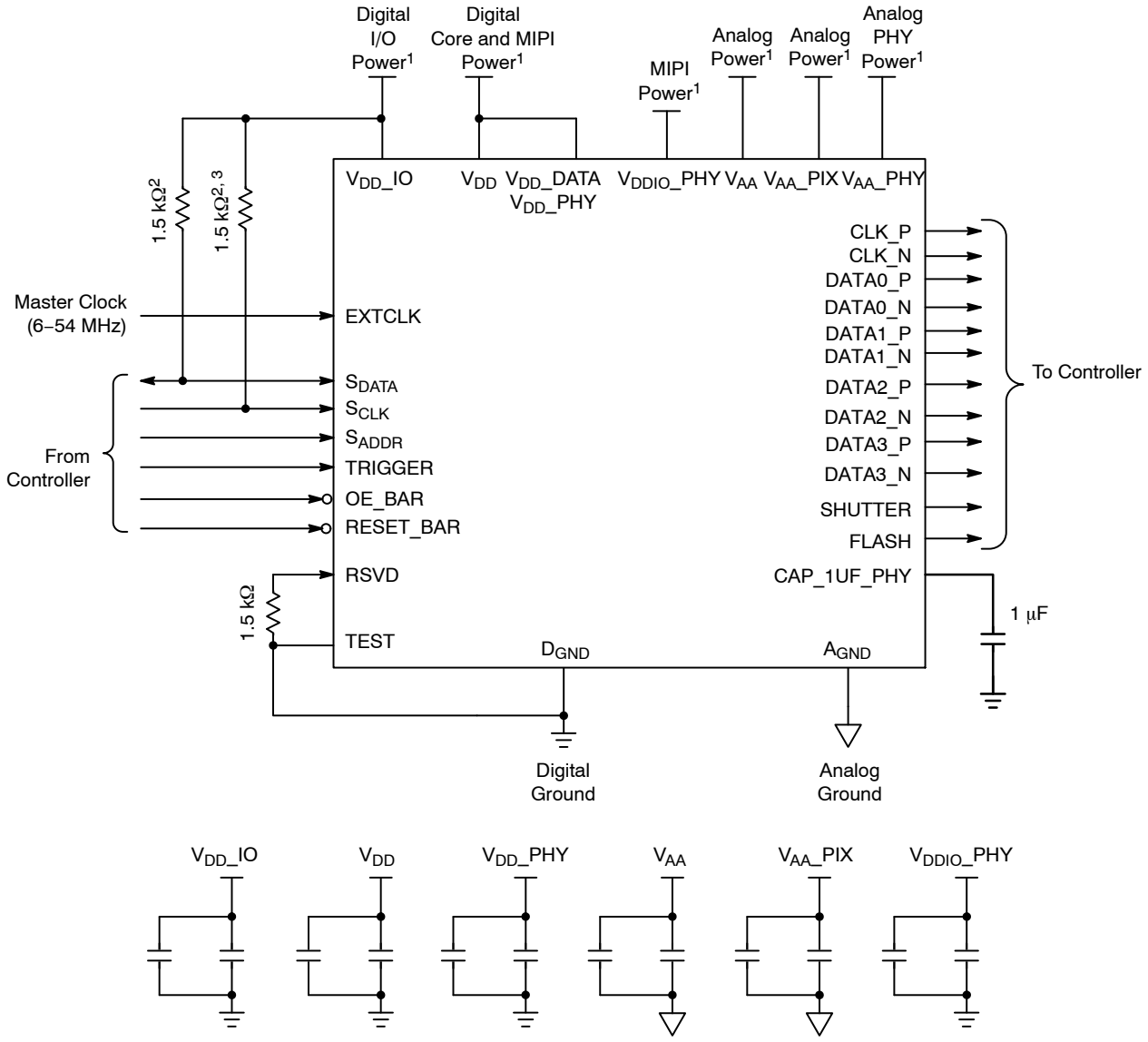


Figure 3. Pixel Color Pattern Detail (Top Right Corner)

CONFIGURATION AND PINOUT

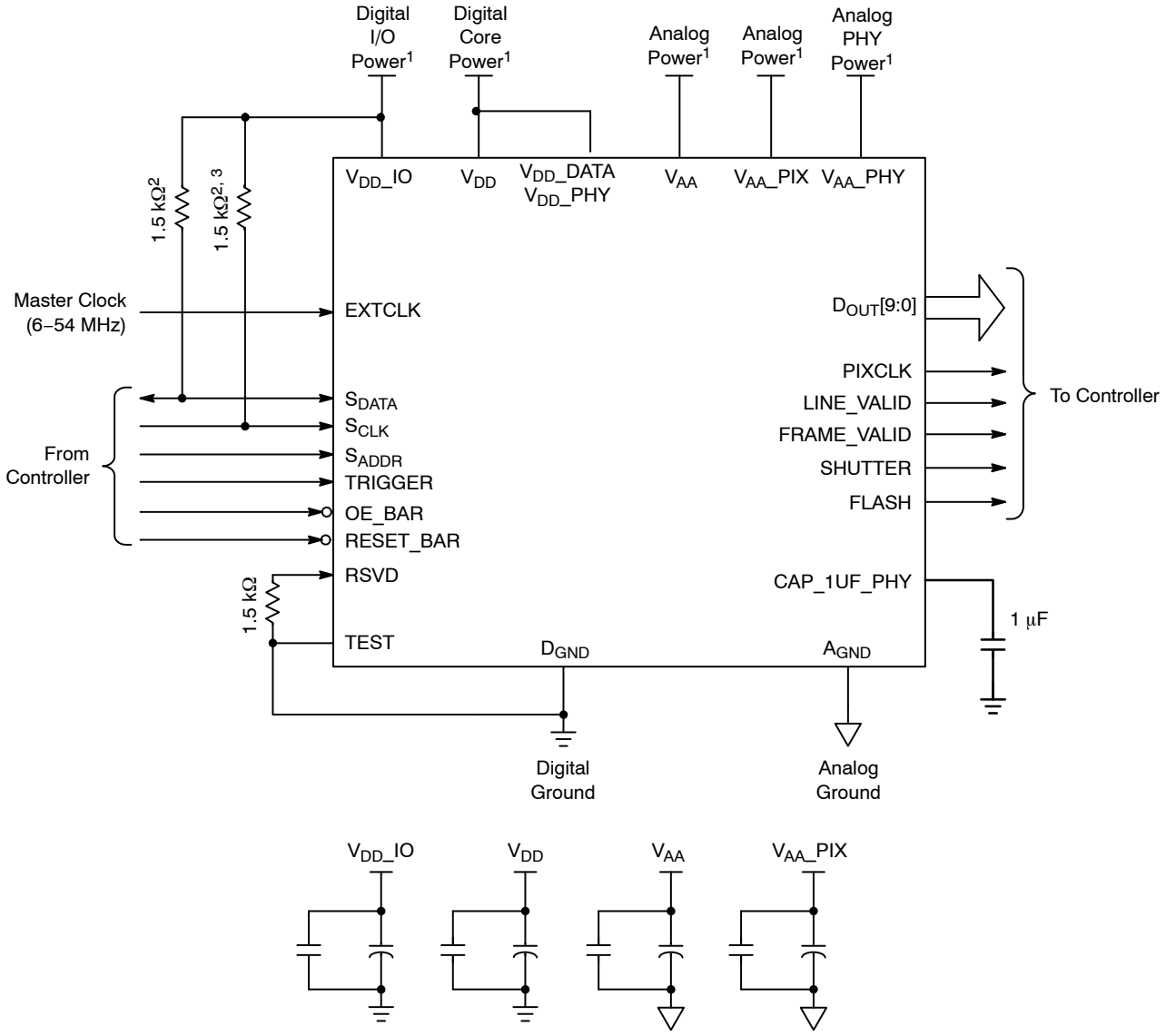
The figures and tables below show a typical configuration for the AR0234CS image sensor and show the package pinouts.



Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. This pull−up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. Analog and digital grounds need to be connected at a single point.
6. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0234CS demo headboard schematics for circuit recommendations.
7. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
8. It is recommended that VDD_PHY and VDD_DATA are tied to VDD (1.2 V).
9. It is recommended that VAA_PHY is connected to 2.8 V.
10. VDDIO_PHY should be connected to 1.8 V only.

Figure 4. Serial 4−lane MIPI Interface



Notes:

1. All power supplies must be adequately decoupled.
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3. This pull−up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
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6. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0234CS demo headboard schematics for circuit recommendations.
7. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
8. It is recommended that V_{DD}_PHY and V_{DD}_DATA are tied to V_{DD} (1.2 V).
9. It is recommended that VAA_PHY is connected to 2.8 V.
10. VDDIO_PHY should be connected to 1.8 V only.

Figure 5. Parallel Interface

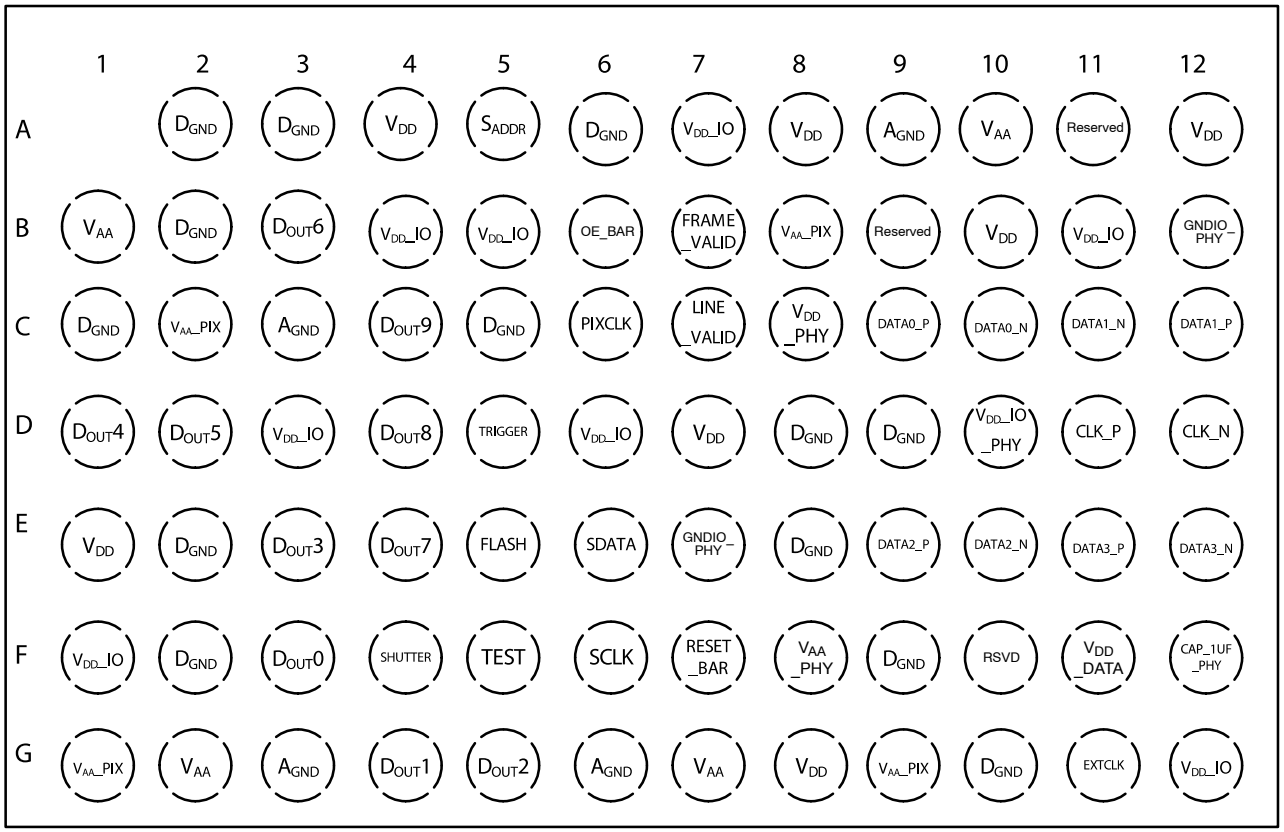


Figure 6. 9.995 x 5.595 mm 83−ball CSP Package (Top View)

Table 3. PIN DESCRIPTIONS − 83−BALL CSP PACKAGE

Name	CSP Ball	Type	Description
DATA0_N	C10	Output	MIPI serial data, lane 0, differential N
DATA0_P	C9	Output	MIPI serial data, lane 0, differential P
DATA1_N	C11	Output	MIPI serial data, lane 1, differential N
DATA1_P	C12	Output	MIPI serial data, lane 1, differential P
DATA2_N	E10	Output	MIPI serial data, lane 2, differential N
DATA2_P	E9	Output	MIPI serial data, lane 2, differential P
DATA3_N	E12	Output	MIPI serial data, lane 3, differential N
DATA3_P	E11	Output	MIPI serial data, lane 3, differential P
CLK_N	D12	Output	MIPI serial clock differential N
CLK_P	D11	Output	MIPI serial clock differential P
VAA	A10, B1, G2, G7	Power	Analog Power (2.8 V)
VAA_PHY	F8	Power	Analog PHY power supply. Analog power supply for the serial interface (2.8 V).
EXTCLK	G11	Input	External input clock
VDD_PHY	C8	Power	MIPI Power Supply (1.2 V)
VDDIO_PHY	D10	Power	I/O Power Supply (1.8 V)
DGND	A2 A3, A6, B2, C1, C5, D8, D9, E2, E8, F2, F9, G10	Power	Digital GND
GNDIO_PHY	B12, E7	Power	Connect to DGND.
VDD	A4, A8, A12, B10, D7, E1, G8	Power	Digital Power (1.2 V)

Table 3. PIN DESCRIPTIONS – 83−BALL CSP PACKAGE (continued)

Name	CSP Ball	Type	Description
V_{DD}_DATA	F11	Power	MIPI PHY Power (1.2 V)
AGND	A9, C3, G3, G6	Power	Analog GND
SADDR	A5	Input	Two−Wire Serial address select
SCLK	F6	Input	Two−Wire Serial clock input
SDATA	E6	I/O	Two−Wire Serial data I/O
VAA_PIX	B8, C2, G1, G9	Power	Pixel Power (2.8 V)
LINE_VALID	C7	Output	Asserted when DOUT line data is valid
FRAME_VALID	B7	Output	Asserted when DOUT frame data is valid
PIXCLK	C6	Output	Pixel clock out. DOUT is valid on rising edge of this clock
SHUTTER	F4	Output	Control of external mechanical shutter
FLASH	E5	Output	Control signal to drive external light sources
VDD_IO	A7, B4, B5, B11, D3, D6, F1, G12	Power	I/O supply power (1.8 V or 2.8 V)
DOUT7	E4	Output	Parallel pixel data output
DOUT8	D4	Output	Parallel pixel data output
DOUT9	C4	Output	Parallel pixel data output (MSB)
TEST	F5	Input	Manufacturing test enable pin (connect to DGND)
DOUT4	D1	Output	Parallel pixel data output
DOUT5	D2	Output	Parallel pixel data output
DOUT6	B3	Output	Parallel pixel data output
TRIGGER	D5	Input	Exposure synchronization input
OE_BAR	B6	Input	Output enable (active LOW). This pin is used for MIPI interface only.
DOUT0	F3	Output	Parallel pixel data output (LSB)
DOUT1	G4	Output	Parallel pixel data output
DOUT2	G5	Output	Parallel pixel data output
DOUT3	E3	Output	Parallel pixel data output
RSVD	F10	Input	Must be connected with 1.5 kΩ resistor between this pin and DGND.
RESET_BAR	F7	Input	Asynchronous reset (active LOW). All settings are restored to factory default
CAP_1UF_PHY	F12	Power	External bypass capacitor for MIPI Regulator
Reserved	A11, B9	N/A	Reserved (do not connect)

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0234CS.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD_IO} off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW − the interface protocol determines which device is allowed to drive S_{DATA} at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive S_{CLK} LOW; the AR0234CS uses S_{CLK} as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

- a (repeated) start condition
- a slave address/data direction byte
- an (a no) acknowledge bit
- a message byte
- a stop condition

The bus is idle when both S_{CLK} and S_{DATA} are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on S_{DATA} while S_{CLK} is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on S_{DATA} while S_{CLK} is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each S_{CLK} clock period. S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0234CS are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the S_{ADDR} input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the S_{CLK} clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases S_{DATA}. The receiver indicates an acknowledge bit by driving S_{DATA} LOW. As for data transfers, S_{DATA} can change when S_{CLK} is LOW and must be stable while S_{CLK} is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive S_{DATA} LOW during the S_{CLK} clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 7) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 7 shows how the internal register address maintained by the AR0234CS is loaded and incremented as the sequence proceeds.

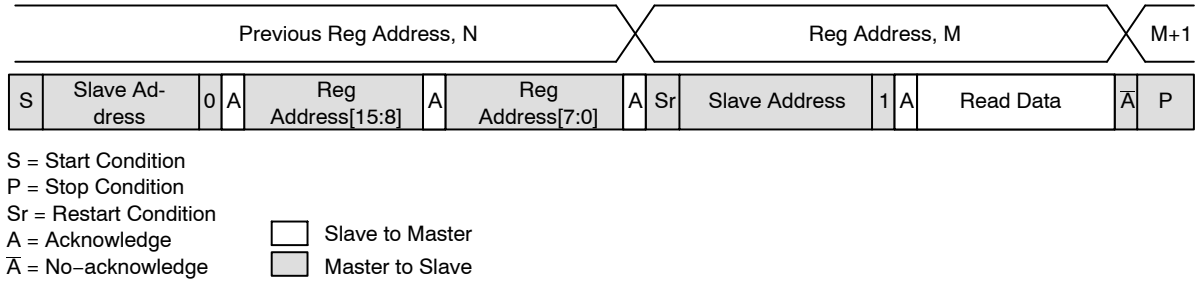


Figure 7. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 8) performs a read using the current value of the AR0234CS internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

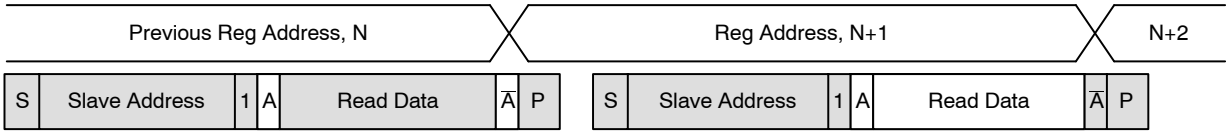


Figure 8. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 9) starts in the same way as the single READ from random location (Figure 7). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

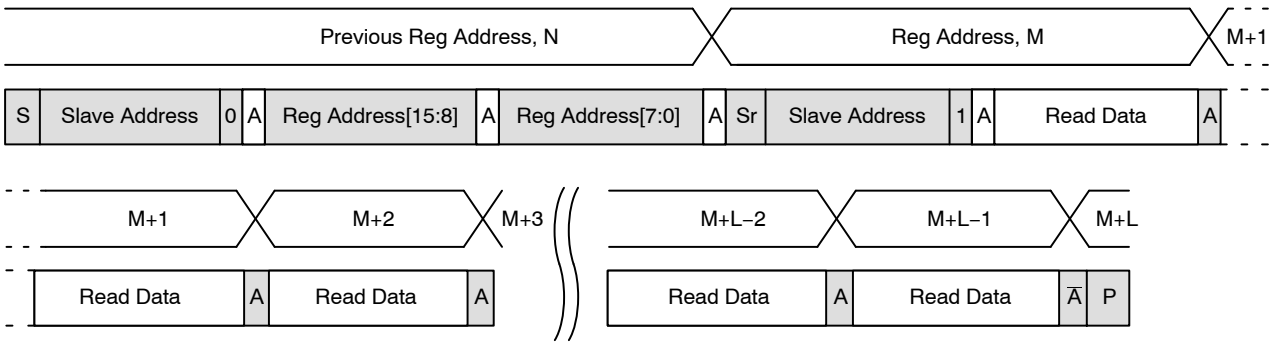


Figure 9. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 10) starts in the same way as the single READ from current location (Figure 8). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

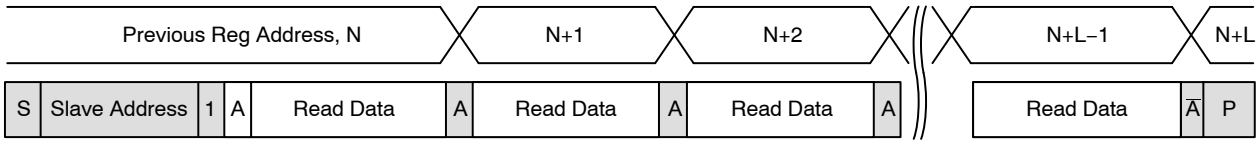


Figure 10. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 11) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

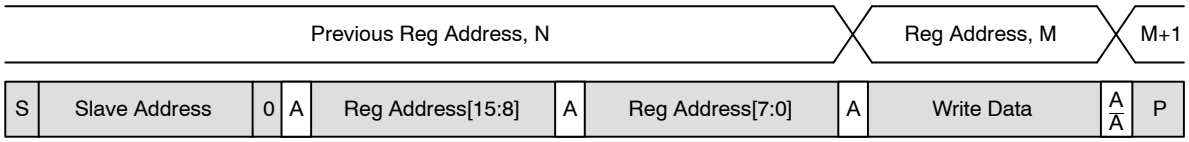


Figure 11. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 12) starts in the same way as the single WRITE to random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

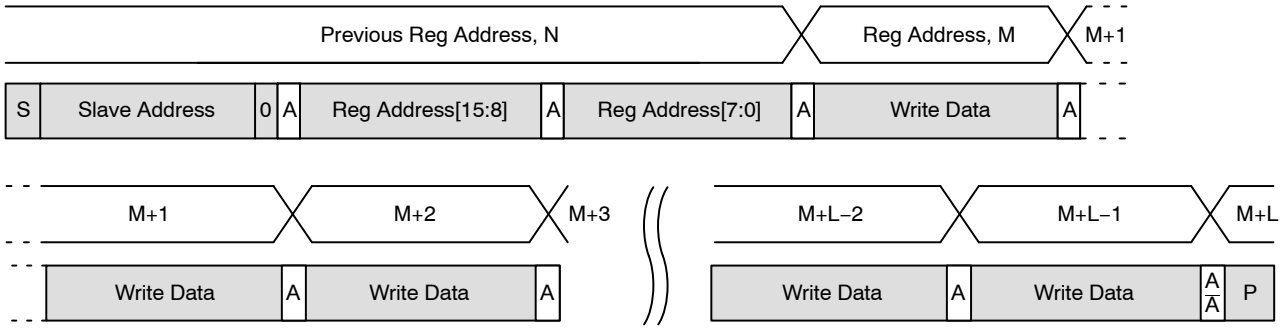


Figure 12. Sequential WRITE, Start at Random Location

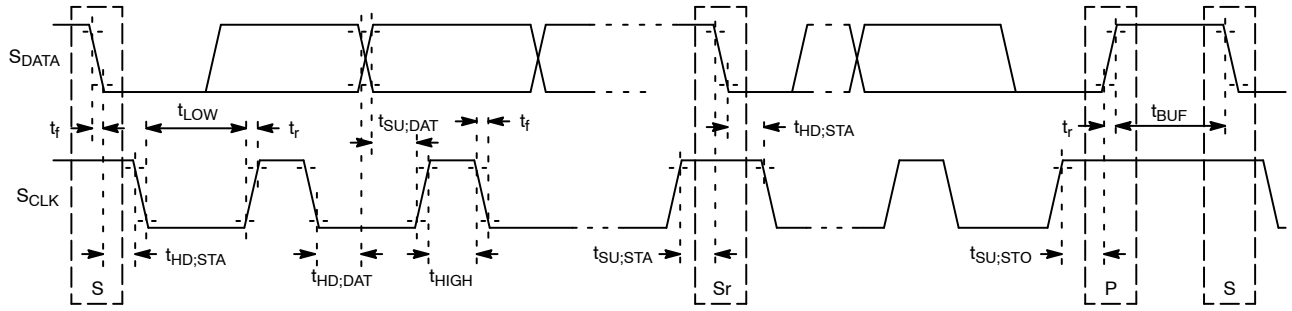
ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply to the following conditions:

V_{DD} = V_{DD}_PHY = V_{DD}_DATA = 1.2 V ±0.06;
V_{DD}_IO = V_{AA} = V_{AA}_PIX = 2.8 V ±0.3 V; V_{DDIO}_PHY = 1.8 V ± 0.1 V
T_A = −40°C to +85°C;
Output Load = 10 pF;
PIXCLK Frequency = 90 MHz;
MIPI off.

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 13 and Table 4.



NOTE: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 13. Two−Wire Serial Bus Timing Parameters

Table 4. TWO−WIRE SERIAL BUS CHARACTERISTICS
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.2 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PHY = 1.2 V; V_{DDIO}_PHY = 1.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) START Condition (After This Period, the First Clock Pulse is Generated)	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4.0	–	0.6	–	μs
Set−up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	μs
Data Set−up Time	$t_{SU;DAT}$	250	–	100 (Note 6)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1Cb (Note 7)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1Cb (Note 7)	300	ns
Set−up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive Load for each Bus Line	Cb	–	400	–	400	pF

Table 4. TWO−WIRE SERIAL BUS CHARACTERISTICS (continued)
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.2 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PHY = 1.2 V; V_{DDIO}_PHY = 1.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
Serial Interface Input Pin Capacitance	CIN_SI	−	3.3	−	3.3	pF
S_{DATA} Max Load Capacitance	CLOAD_SD	−	30	−	30	pF
S_{DATA} Pull−up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two−wire control is I^2C−compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD}_IO and V_{ILmax} = 0.1 V_{DD}_IO levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK. The two−wire standard specifies a minimum rise and fall time for Fast−Mode operation. This specification is not a timing requirement that is enforced on ON Semiconductor sensor's as a receiver, because our receivers are designed to work in mixed systems with std−mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two−wire slew−rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current−clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I^2C−bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0234CS launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[9:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 14 and Table 5 for I/O timing (AC) characteristics.

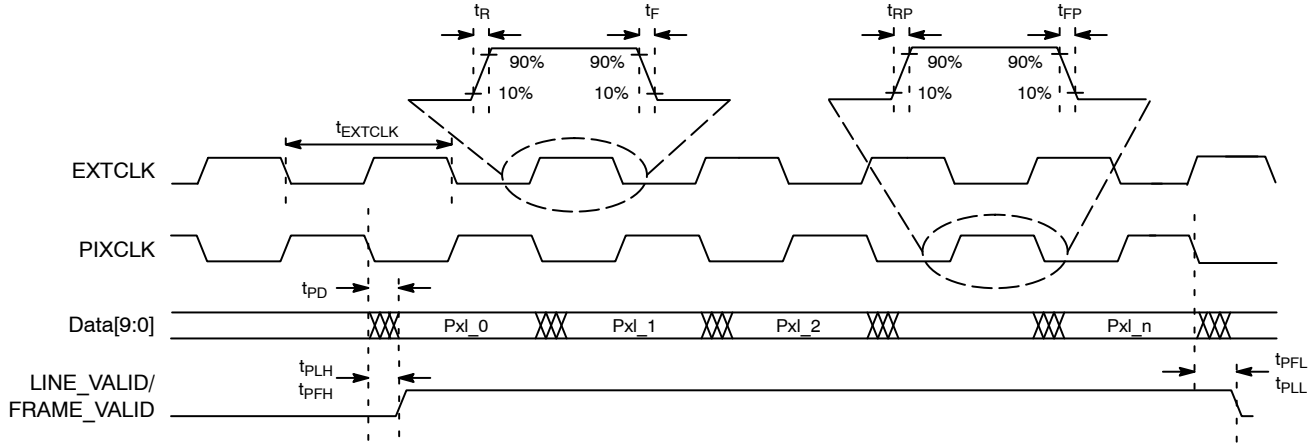


Figure 14. I/O Timing Diagram

Table 5. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (1.8 V V_{DD_IO}) (Note 8)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6	–	54	MHz
t_{EXTCLK}	Input Clock Period		18.5	–	166.7	ns
t_R	Input Clock Rise Time	PLL Enabled	–	3	–	ns
t_F	Input Clock Fall Time	PLL Enabled	–	3	–	ns
t_{JITTER}	Input Clock Jitter		–	–	600	ns
t_{cp}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4	9	–	106	ns
t_{RP}	PIXCLK Rise Time	PCLK Slew Rate = 6	2.1	–	4.2	ns
t_{FP}	PIXCLK Fall Time	PCLK Slew Rate = 6	1	–	2.7	ns
	PIXCLK Duty Cycle		30	–	55	%
f_{PIXCLK}	PIXCLK Frequency	PIXCLK Slew Rate = 6, Data Slew Rate = 7	6	–	90	MHz
t_{PD}	PIXCLK to Data Valid	PIXCLK Slew Rate = 6, Data Slew Rate = 7	2.5	–	3.6	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	2.5	–	3.0	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	2.2	–	3.0	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	0.5	–	1.2	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	0.2	–	0.7	ns
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

8. Minimum and maximum values are taken at 105°C ambient, 1.7 V and −40°C ambient, 1.9 V. All values are taken at the 50% transition point. The loading used is 10 pF.
9. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 6. I/O TIMING CHARACTERISTICS, PARALLEL OUTPUT (2.8 V V_{DD_IO}) (Note 10)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6	–	54	MHz
t_{EXTCLK}	Input Clock Period		18.5	–	166.7	ns
t_R	Input Clock Rise Time	PLL Enabled	–	3	–	ns
t_F	Input Clock Fall Time	PLL Enabled	–	3	–	ns
t_{JITTER}	Input Clock Jitter	Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4	–	–	600	ns
t_{cp}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled, PIXCLK Slew Rate = 4	4.3	–	105	ns
t_{RP}	PIXCLK Rise Time	PCLK Slew Rate = 6	0.9	–	2.3	ns
t_{FP}	PIXCLK Fall Time	PCLK slew rate = 6	0.5	–	1.5	ns
	PIXCLK Duty Cycle		40	–	55	%
f_{PIXCLK}	PIXCLK Frequency	PIXCLK Slew Rate = 6, Data Slew Rate = 7	6	–	90	MHz
t_{PD}	PIXCLK to Data Valid	PIXCLK Slew Rate = 6, Data Slew Rate = 7	2.2	–	3.1	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	1.7	–	2.4	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK Slew Rate = 6, Data Slew Rate = 7	1.7	–	2.3	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	0.8	–	1.1	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK Slew Rate = 6, Data Slew Rate = 7	0.4	–	0.9	ns
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

10. Minimum and maximum values are taken at 105°C ambient, 1.7 V and −40°C ambient, 1.9 V. All values are taken at the 50% transition point. The loading used is 10 pF.
11. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7. I/O RISE SLEW RATE (2.8 V V_{DD}_IO) (Note 12)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.39		0.91	V/ns
1	0.49		1.85	V/ns
2	0.54		2.14	V/ns
3	0.64		2.30	V/ns
4	0.80		2.45	V/ns
5	1.00		2.79	V/ns
6	1.13		3.06	V/ns
7	1.27		3.33	V/ns

12. Minimum and maximum values are taken at 105°C ambient, 2.5 V and −40°C junction, 3.1 V. The loading used is 10 pF.

Table 8. I/O FALL SLEW RATE (2.8 V V_{DD}_IO) (Note 13)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.37		2.66	V/ns
1	0.54		3.15	V/ns
2	0.67		3.52	V/ns
3	1.25		3.90	V/ns
4	1.55		4.03	V/ns
5	1.77		4.15	V/ns
6	1.94		4.21	V/ns
7	2.07		4.21	V/ns

13. Minimum and maximum values are taken at 105°C ambient, 1.7 V and −40°C ambient, 1.9 V. The loading used is 10 pF.

Table 9. I/O RISE SLEW RATE (1.8 V V_{DD}_IO) (Note 14)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.19		0.31	V/ns
1	0.22		0.33	V/ns
2	0.24		0.38	V/ns
3	0.27		0.64	V/ns
4	0.29		0.76	V/ns
5	0.32		0.85	V/ns
6	0.34		0.91	V/ns
7	0.37		0.97	V/ns

14. Minimum and maximum values are taken at 105°C ambient, 1.7 V and −40°C ambient, 1.9 V. The loading used is 10 pF.

Table 10. I/O FALL SLEW RATE (1.8 V V_{DD}_IO) (Note 15)

Parallel Slew (R0x306E[15:13])	Min	Typ	Max	Unit
0	0.17		0.32	V/ns
1	0.23		0.61	V/ns
2	0.29		1.13	V/ns
3	0.32		1.39	V/ns
4	0.37		1.55	V/ns
5	0.43		1.69	V/ns
6	0.50		1.80	V/ns
7	0.61		1.99	V/ns

15. Minimum and maximum values are taken at 105°C ambient, 1.7 V and −40°C ambient, 1.9 V. The loading used is 10 pF.

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 11, Table 12, Table 13, and Table 14.

Table 11. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Slew Rate	Unit
V_{DD}	Core Digital Voltage		1.14	1.2	1.26		V
V_{DD}_IO	I/O Digital Voltage		1.7/2.5	1.8/2.8	1.9/3.1		V
V_{DD}_IO_PHY	I/O Power Supply		1.7	1.8	1.9		V
V_{AA}	Analog Voltage		2.5	2.8	3.1		V
V_{AA}_PIX	Pixel Supply Voltage		2.5	2.8	3.1		V
V_{DD}_PHY	MIPI Supply Voltage		1.14	1.2	1.26		V
V_{DD}_DATA	MIPI Supply Voltage		1.14	1.2	1.26		V
V_{AA}_PHY	MIPI Supply Voltage		2.5	2.8	3.1		V
V_{IH}	Input HIGH Voltage		VDD_IO * 0.7	–	–		V
V_{IL}	Input LOW Voltage		–	–	VDD_IO * 0.3		V
I_{IN}	Input Leakage Current	No Pull-up Resistor; VIN = VDD_IO or DGND		–	20		uA
V_{OH}	Output HIGH Voltage		VDD_IO * 0.7 (1.8/2.8)	–	–	0	V
V_{OH}	Output HIGH Voltage		VDD_IO * 0.7 (1.8/2.8)	–	–	7	V
V_{OL}	Output LOW Voltage		–	–	0.4 (1.8 V/2.8 V)	0	V
V_{OL}	Output LOW Voltage	VDD_IO = 2.8 V	–	–	0.4 (1.8 V/2.8 V)	7	V
I_{OH}	Output HIGH Current	At Specified VOH	–	–	3 (1.8 V/2.8 V)	0	mA
I_{OH}	Output HIGH Current	At Specified VOH		–	7 (1.8 V) 12(2.8 V)	7	mA
I_{OL}	Output LOW Current	At Specified VOL	–	–	2 (1.8 V) 3(2.8 V)	0	mA
I_{OL}	Output LOW Current	At Specified VOL	–	–	7 (1.8 V) 9(2.8 V)	7	mA

CAUTION: Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 12. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{SUPPLY}	Power Supply Voltage (All Supplies)	–0.3	4.5	V
I_{SUPPLY}	Total Power Supply Current	–	400	mA
I_{GND}	Total Ground Current	–	400	mA
V_{IN}	DC Input Voltage	–0.3	V_{DD}_IO + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{DD}_IO + 0.3	V
T_{STG}	Storage Temperature (Note 16)	–40	+125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

16. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13. OPERATING CURRENT CONSUMPTION FOR PARALLEL OUTPUT

(V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{AA}_PHY = 2.8 V; V_{DD} = V_{DD}_PHY = V_{DD}_DATA = 1.2 V; V_{DDIO}_PHY = 1.8 V; PLL Enabled and PIXCLK = 90 MHz; T_A = 25°C; C_{LOAD} = 10 pF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDD_PHY + IDD_DATA + IDD	Digital Operating Current	Parallel, Streaming, Full Resolution 30 fps	–	52	105	mA
IDD_IO	I/O Digital Operating Current	Parallel, Streaming, Full Resolution 30 fps	–	40	112	mA
IDDIO_PHY	I/O PHY Digital Operating Current	Parallel, Streaming, Full Resolution 30 fps	–	0	1	mA
IAA_PHY + IAA	Analog Operating Current	Parallel, Streaming, Full Resolution 30 fps	–	50	90	mA
IAA_PIX	Pixel Supply Current	Parallel, Streaming, Full Resolution 30 fps	–	5	13	mA

17. Values in Table 13 are subject to change.
18. Maximum values for V_{DD}_IO parallel are dependent on the specific load being applied in the final design. Typical values are based on a load of 20 pF.
19. The following supply rails can be connected together.
    1. V_{DD}, V_{DD}−PHY and V_{DD}_DATA
    2. VDD_IO and VDDIO_PHY if 1.8 VDC each
    3. V_{AA}, V_{AA}_PHY and V_{AA}_PIX

Table 14. OPERATING CURRENT CONSUMPTION FOR MIPI OUTPUT

(V_{AA} = V_{AA}_PIX = V_{DD}_IO = V_{AA}_PHY = 2.8 V; V_{DD} = V_{DD}_PHY = V_{DD}_DATA = 1.2 V; V_{DDIO}_PHY = 1.8 V; PLL Enabled and PIXCLK = 90 MHz; T_A = 25°C; C_{LOAD} = 10 pF)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDD_PHY + IDD_DATA + IDD	Digital Operating Current	MIPI, Streaming, Full Resolution 120 fps	–	155	250	mA
IDD_IO	I/O Digital Operating Current	MIPI, Streaming, Full Resolution 120 fps	–	0.2	1	mA
IDDIO_PHY	I/O PHY Digital Operating Current	MIPI, Streaming, Full Resolution 120 fps	–	10	12	mA
IAA_PHY + IAA	Analog Operating Current	MIPI, Streaming, Full Resolution 120 fps	–	55	102	mA
IAA_PIX	Pixel Supply Current	MIPI, Streaming, Full Resolution 120 fps	–	5	13	mA

20. Values in Table 14 are subject to change.
21. The following supply rails can be connected together.
    1. V_{DD}, V_{DD}−PHY and V_{DD}_DATA
    2. VDD_IO and VDDIO_PHY if 1.8 VDC each
    3. V_{AA}, V_{AA}_PHY and V_{AA}_PIX

Table 15. STANDBY CURRENT CONSUMPTION

(Analog = V_{AA} + V_{AA}_PIX + V_{AA}_PHY; Digital = V_{DD} + V_{DD}_IO + V_{DD}_PHY + V_{DDIO}_PHY + V_{DD}_DATA; T_A = 25°C)

Definition	Condition	Min	Typ	MAX	Unit
Soft Standby (Clock Off, Driven Low)	Analog, 2.8 V	–	5	35	μA
	Digital, 1.2 V/1.8 V/2.8 V	–	250	4000	μA
Soft Standby (Clock On, EXTCLK = 27 MHz)	Analog, 2.8 V	–	5	35	μA
	Digital, 1.2 V/1.8 V/2.8 V	–	5000	14000	μA
nRESET Low (Clk off)	Analog, 2.8 V	–	5	35	μA
	Digital, 1.2 V/1.8 V/2.8 V	–	250	4000	μA
nRESET Low	Analog, 2.8V	–	5	35	μA
	Digital, 1.2 V/1.8 V/2.8 V	–	250	4000	μA

22. Values in Table 15 are subject to change.

MIPI Electrical Specifications

The ON Semiconductor AR0234CS sensor supports four lanes of MIPI data.

Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.2
- MIPI Alliance Standard for D−PHY version 1.0

MIPI AC and DC Electrical Characteristics

Table 16. MIPI HIGH−SPEED TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	HS transmit differential voltage	140	–	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	–	250	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential−1 or Differential−0	–	–	14	mV
$\Delta V_{CMTX}(1,0)$	V_{CMTX} mismatch when output is Differential−1 or Differential−0	–	–	5	mV
V_{OHHS}	HS output HIGH voltage	–	–	360	mV
Z_{OS}	Single−ended output impedance	40	–	62.5	Ω
ΔZ_{OS}	Single−ended output impedance mismatch	–	–	10	%

Table 17. MIPI HIGH−SPEED TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate	–	–	768	Mb/s
t_{rise}	20–80% rise time	150	–	160	ps
t_{fall}	20–80% fall time	150	–	160	ps

Table 18. MIPI LOW−POWER TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Thevenin output low level	–	–	50	mV
V_{OH}	Thevenin output high level	1.1	1.15	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110	–	–	

Table 19. MIPI LOW−POWER TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_{rise}	15–85% rise time	–	–	25	ns
t_{fall}	15–85% fall time	–	–	25	ns
Slew	Slew rate (C_{LOAD} 5–20 pf)	–	–	250	mV/ns
Slew	Slew rate (C_{LOAD} 20–70 pf)	–	–	150	mV/ns

POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the AR0234 is shown in Figure 15. The available power supplies (V_{AA}/V_{AA}_PIX/V_{AA}_PHY, V_{DD}IO, V_{DD}IO_PHY, V_{DD}/V_{DD}_PHY, and V_{DD}_DATA) must have the separation specified below.

1. Turn on V_{AA}/V_{AA}_PIX/V_{AA}_PHY power supply.
2. After 100 µs, turn on V_{DD}IO power supply.
3. After 100 µs, turn on V_{DD}IO_PHY(1.8 V) power supply.
4. After 100 µs, turn on V_{DD}/V_{DD}_PHY power supply
5. After 100 µs, turn on V_{DD}_DATA power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET_N for at least 1 ms. The parallel interface will be tri-stated during this time.
8. Wait for ~160000 EXTCLKs for internal initialization into soft standby where M3ROM and full OTPM upload would be complete.
9. Set streaming mode (mode_select/stream (R0x301A[2]) = 1) and the internal PLL would be enabled (not locked yet).
10. Wait for 1 ms for PLL lock to complete, Part will then go into streaming mode.

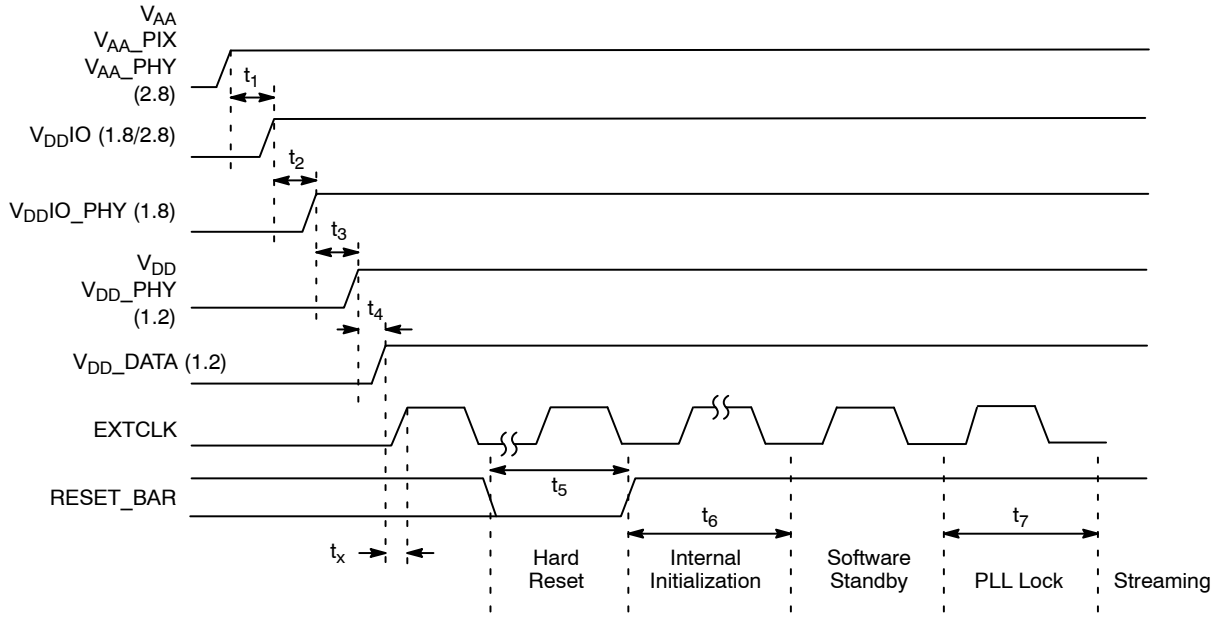


Figure 15. Power-up Sequence

Table 20. POWER-UP SEQUENCE

SN	Definition	Symbol	Min	Typ	Max	Unit
1	V_{AA}/V_{AA}_PIX/V_{AA}_PHY to V_{DD}IO	t_1	0	100	–	µs
2	V_{DD}IO to V_{DD}IO_PHY	t_2	0	100	–	µs
3	V_{DD}IO_PHY to V_{DD}/V_{DD}_PHY	t_3	0	100	–	µs
4	V_{DD}/V_{DD}_PHY to V_{DD}_DATA	t_4	0	100	–	µs
5	Xtal Settle Time (Component Dependent)	t_x	–	30 ms	–	ms
6	Hard Reset	t_5	1	–	–	ms
7	Internal Initialization	t_6	160000	–	–	EXTCLK
8	PLL Lock Time	t_7	1	–	–	ms

23. V_{DD} and V_{DD}_DATA can be tied together (t_4 becomes '0' in this case).
24. V_{AA}/V_{AA}PIX/V_{AA}_PHY can be tied together.

Power Down Sequence

The recommended power-down sequence for the AR0234 is shown in Figure 16. The available power supplies (V_{AA}/V_{AA}_PIX/V_{AA}_PHY, V_{DD}IO, V_{DD}IO_PHY, V_{DD}/V_{DD}_PHY, and V_{DD}_DATA) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0.
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V_{DD}_DATA.
4. Turn off V_{DD}/V_{DD}_PHY.
5. Turn off V_{DD}IO_PHY.
6. Turn off V_{DD}IO.
7. Turn off V_{AA}/V_{AA}_PIX/V_{AA}_PHY.

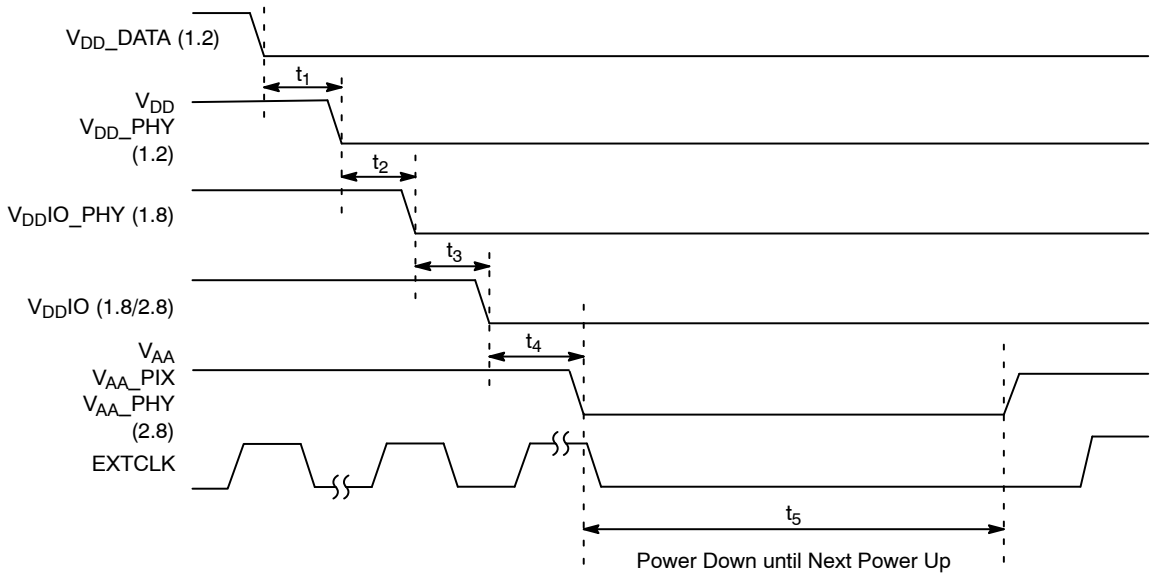


Figure 16. Power-down Sequence

Table 21. POWER-DOWN SEQUENCE

SN	Definition	Symbol	Min	Typ	Max	Unit
1	V_{DD}_DATA to V_{DD}/V_{DD}_PHY	t_1	0	–	–	
2	V_{DD}/V_{DD}_PHY to V_{DD}IO_PHY	t_2	0	–	–	
3	V_{DD}IO_PHY to V_{DD}IO	t_3	0	–	–	
4	V_{DD}IO to V_{AA}/V_{AA}_PIX/V_{AA}_PHY	t_4	0	–	–	
5	PwrDn until Next Pwrup Time	t_5	100	–	–	ms

25. V_{DD} and V_{DD}_DATA can be tied together.
26. V_{AA}/V_{AA}PIX/V_{AA}_PHY can be tied together.

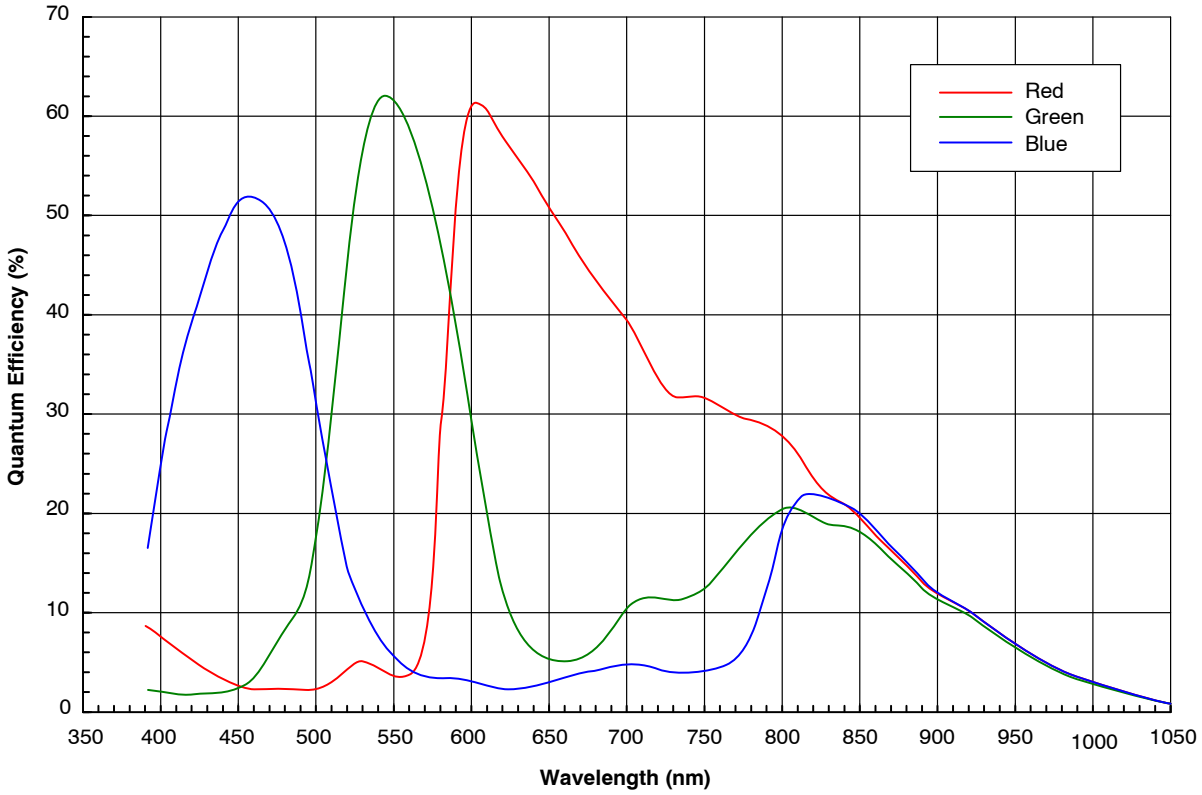


Figure 17. Quantum Efficiency – Color Sensor (Typical)

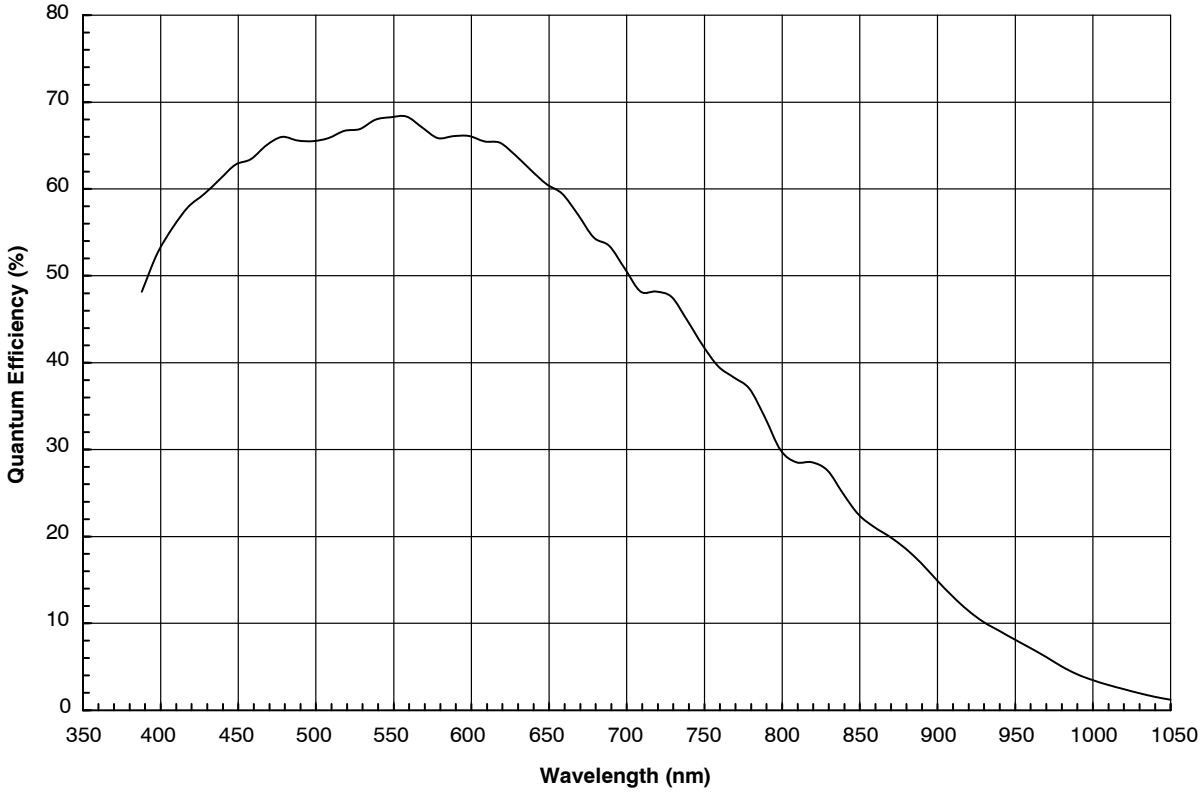


Figure 18. Quantum Efficiency – Monochrome Sensor (Typical)

CRA vs. Image Height Plot

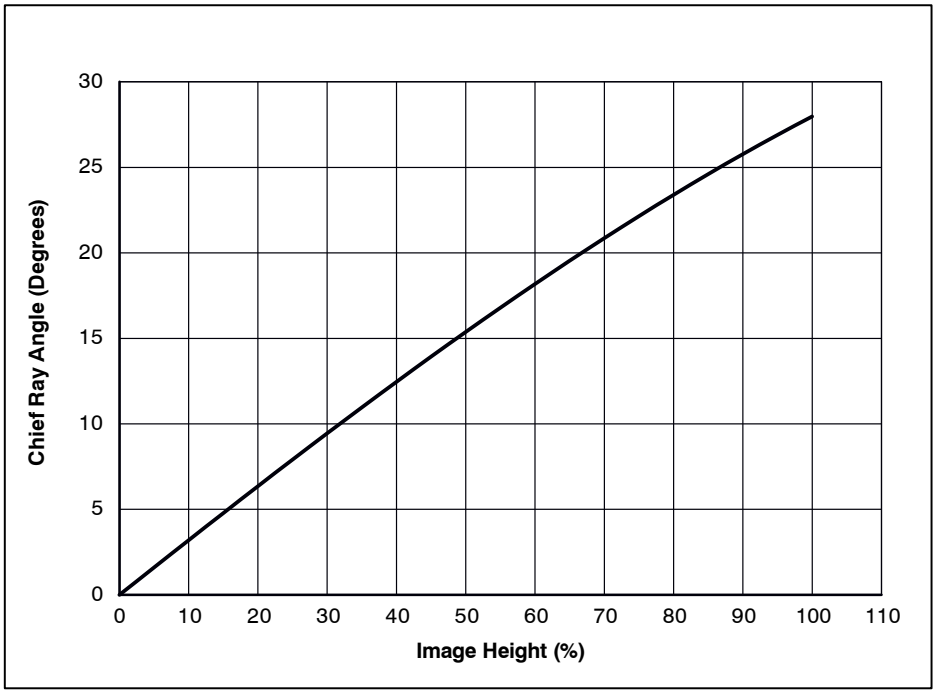


Figure 19. Chief Ray Angle – 28°

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.170	1.61
10	0.340	3.20
15	0.509	4.79
20	0.679	6.36
25	0.849	7.91
30	1.019	9.45
35	1.189	10.97
40	1.358	12.46
45	1.528	13.93
50	1.698	15.38
55	1.868	16.79
60	2.038	18.18
65	2.208	19.54
70	2.377	20.86
75	2.547	22.15
80	2.717	23.39
85	2.887	24.60
90	3.057	25.77
95	3.226	26.90
100	3.396	27.97

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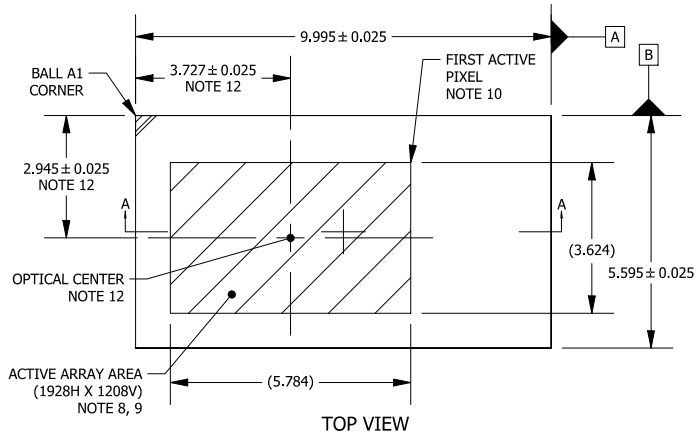
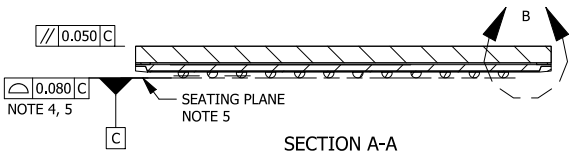


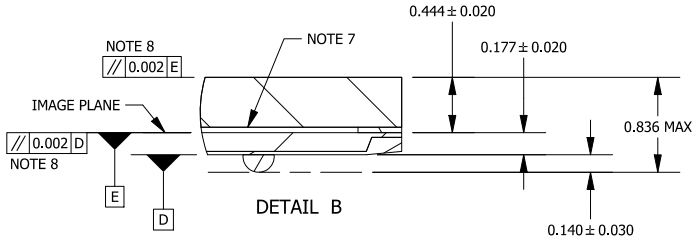
TOP VIEW

NOTES:

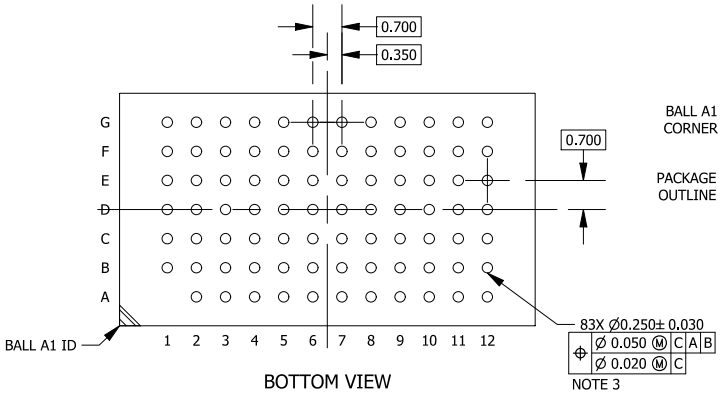
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52.
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.044 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.1°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. PACKAGE CENTER (X, Y) = (0.000, 0.000).
12. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-1.271, -0.148).



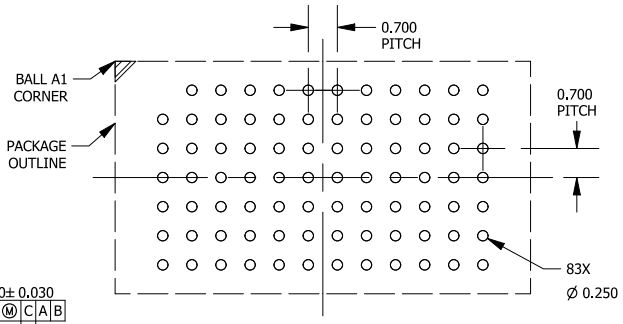
SECTION A-A



DETAIL B



BOTTOM VIEW



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